

FIG. 1

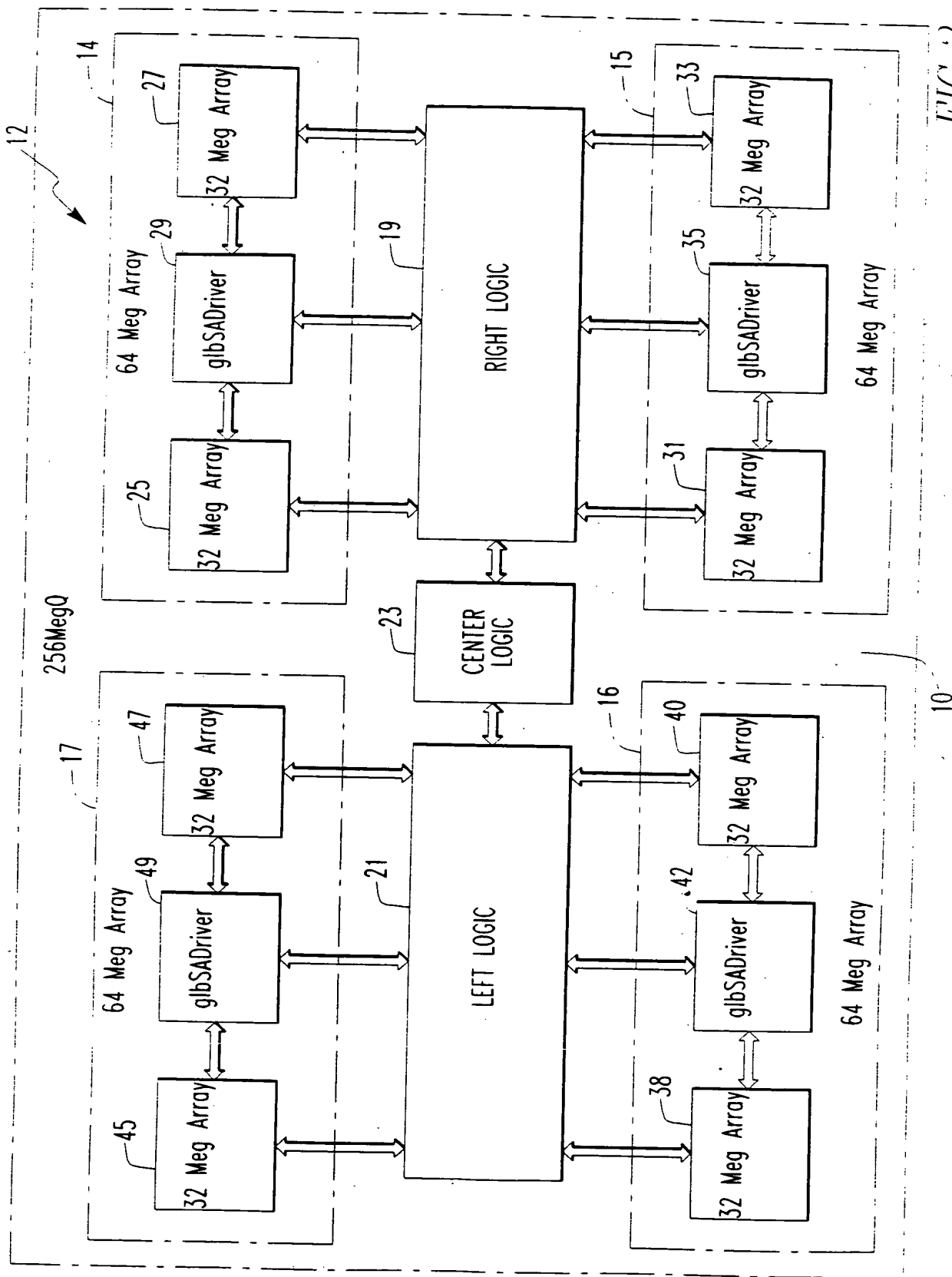
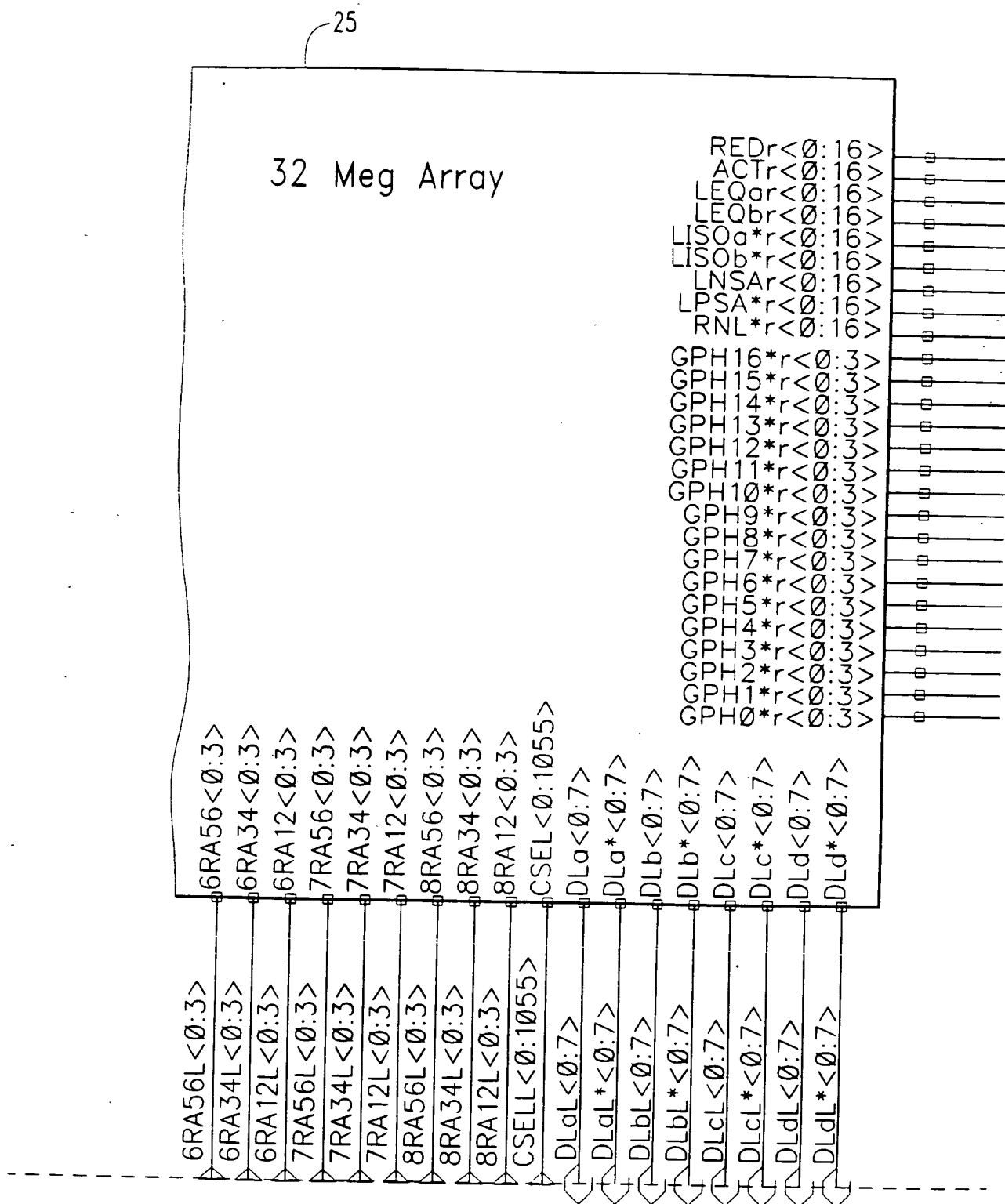
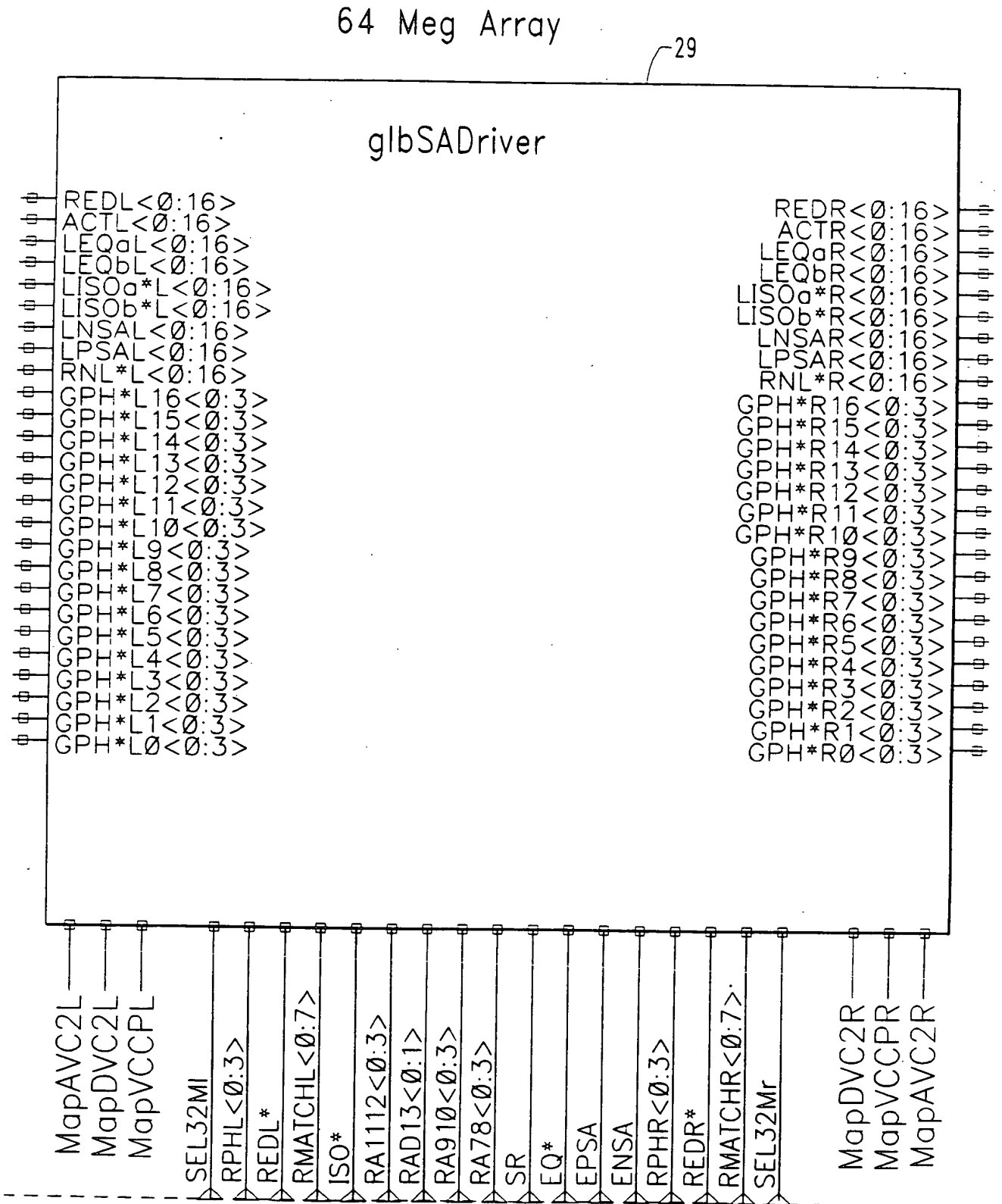


FIG. 2

[illegible]





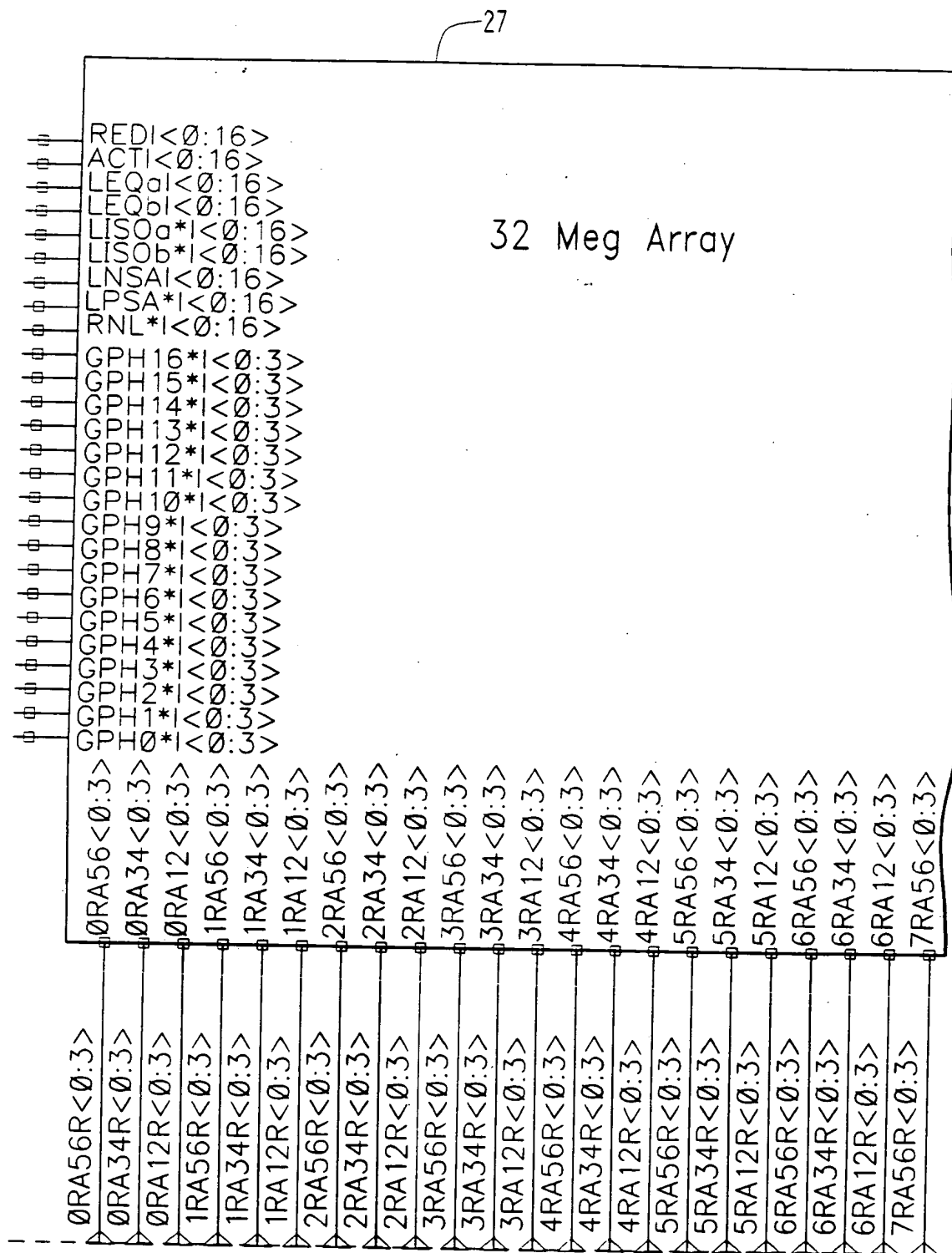
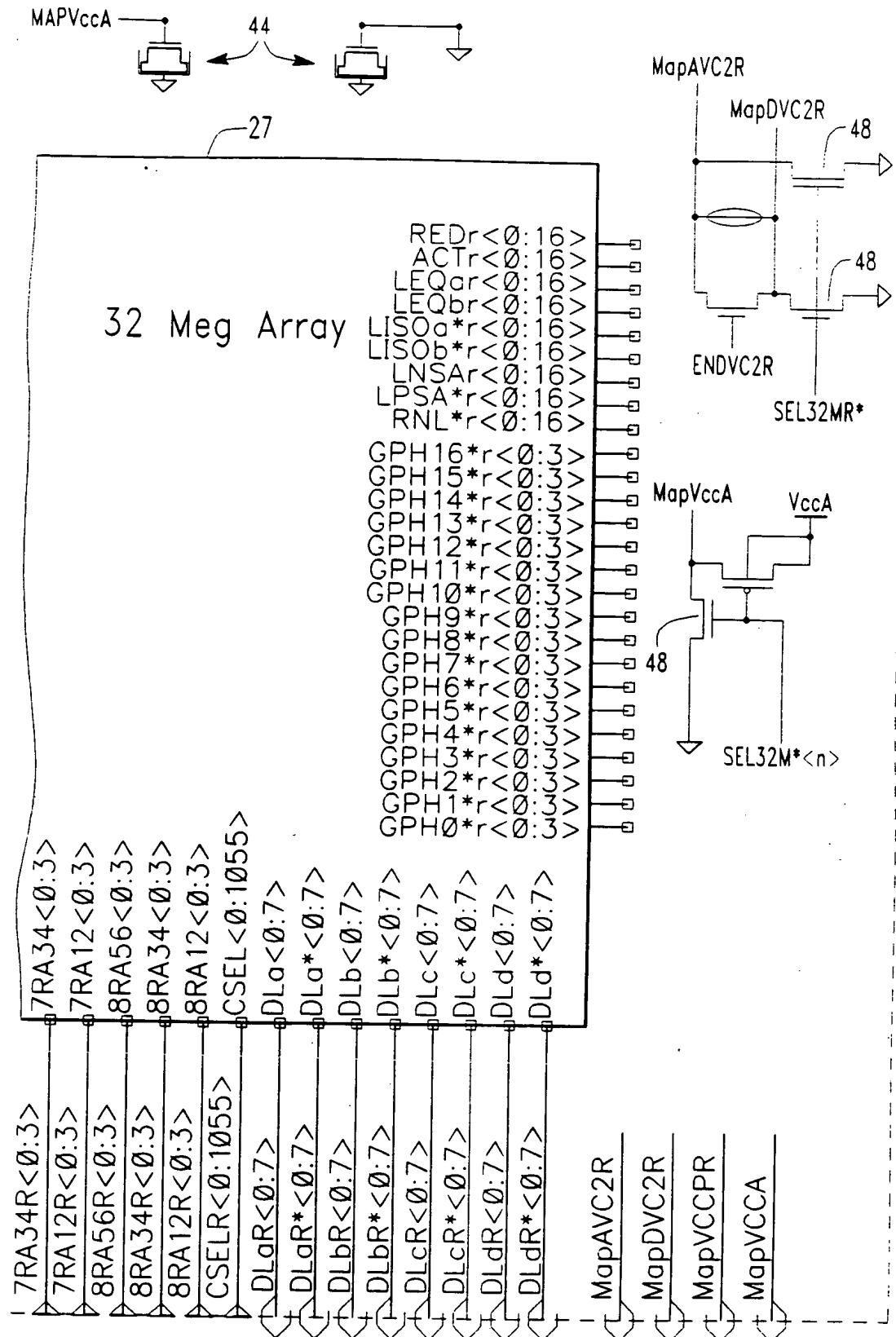
[illegible]

FIG. 3E

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32MEG ARRAY

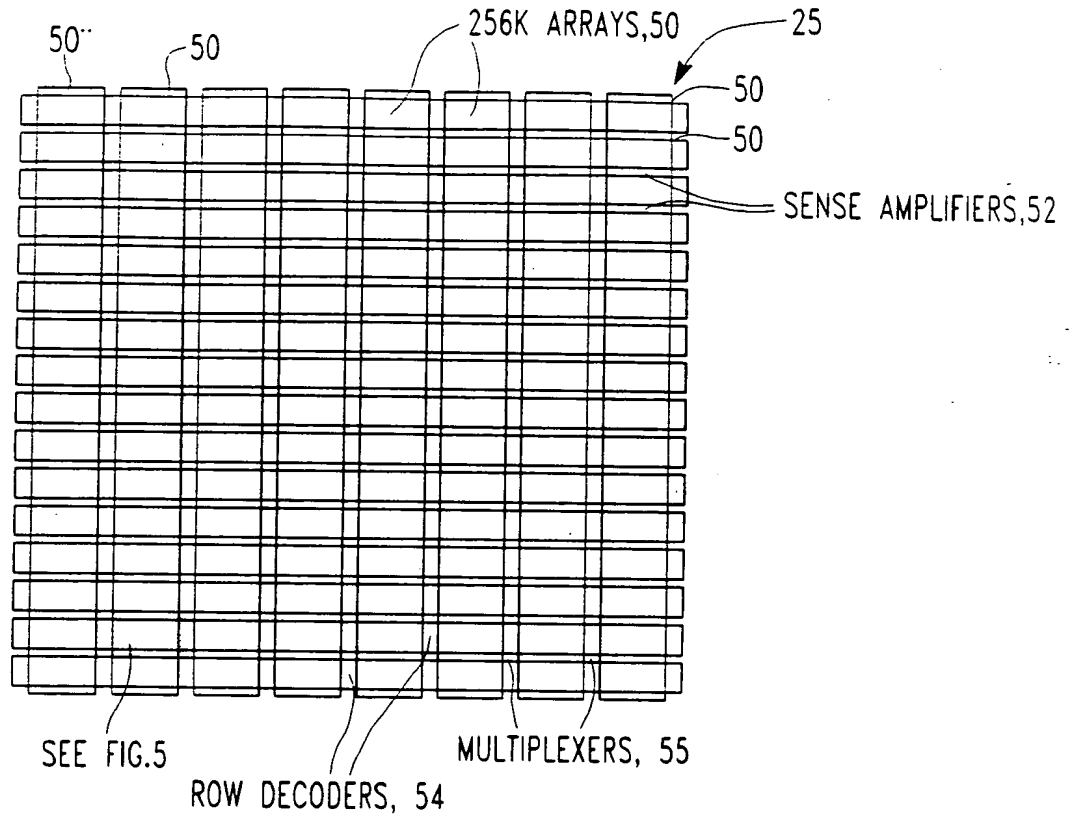


FIG. 4

TOP SECRET 5624E660

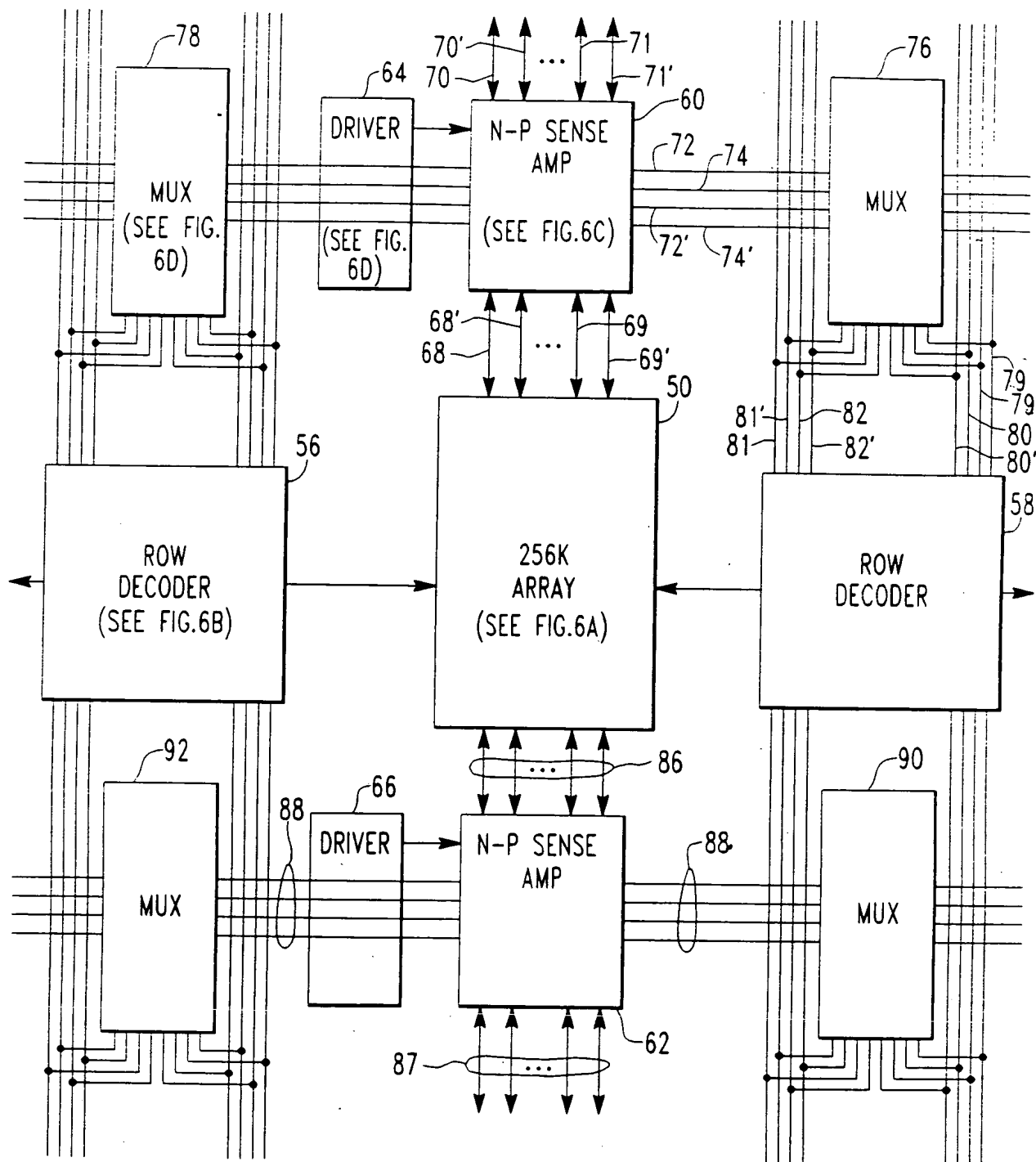


FIG. 5

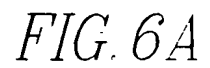
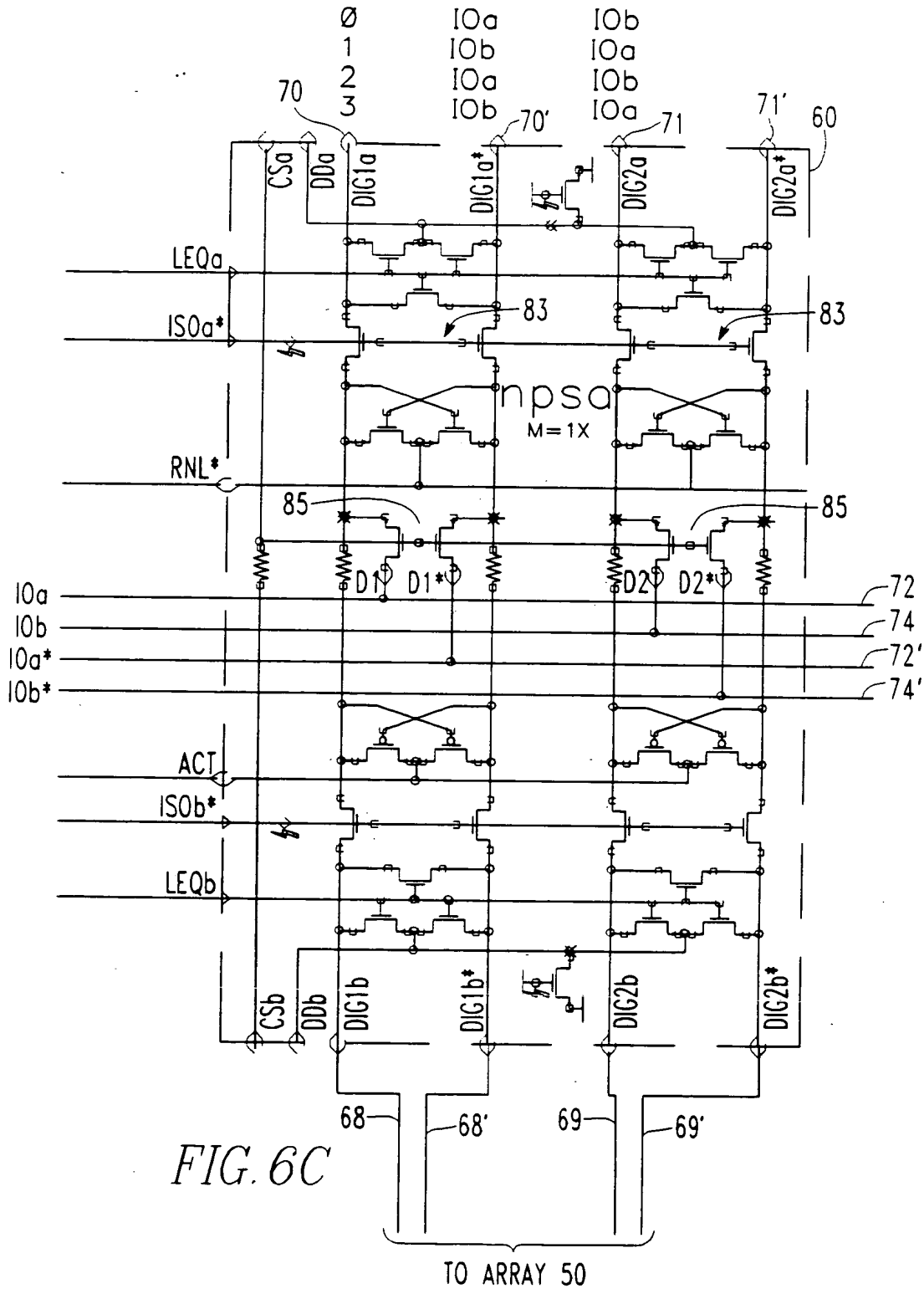
[illegible]

FIG. 6A

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Connections of odd/even
columns to IOa and IOb
alternates with odd/even
column select lines:
CA01* D1(even) D2(odd)



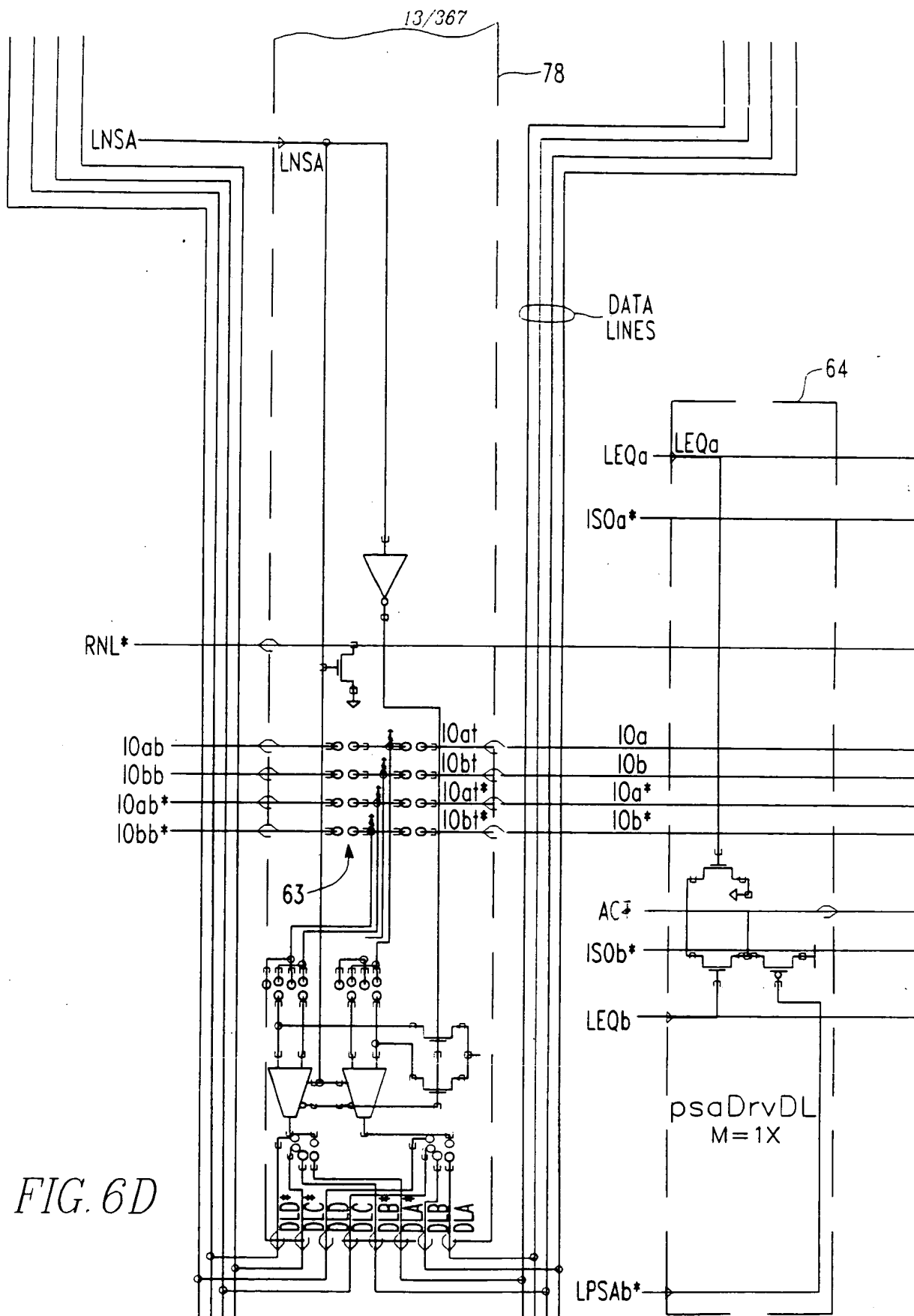
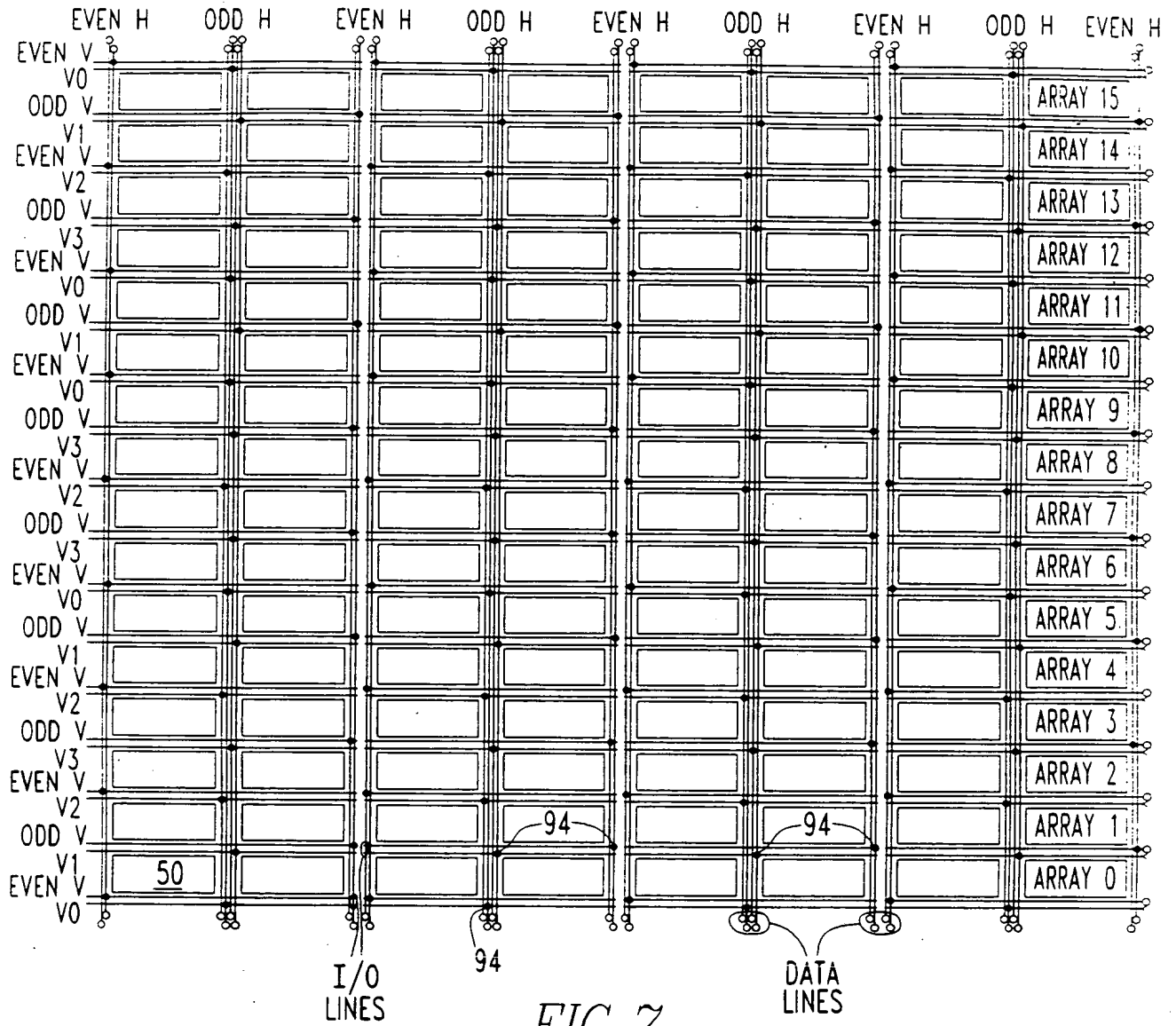


FIG. 6D

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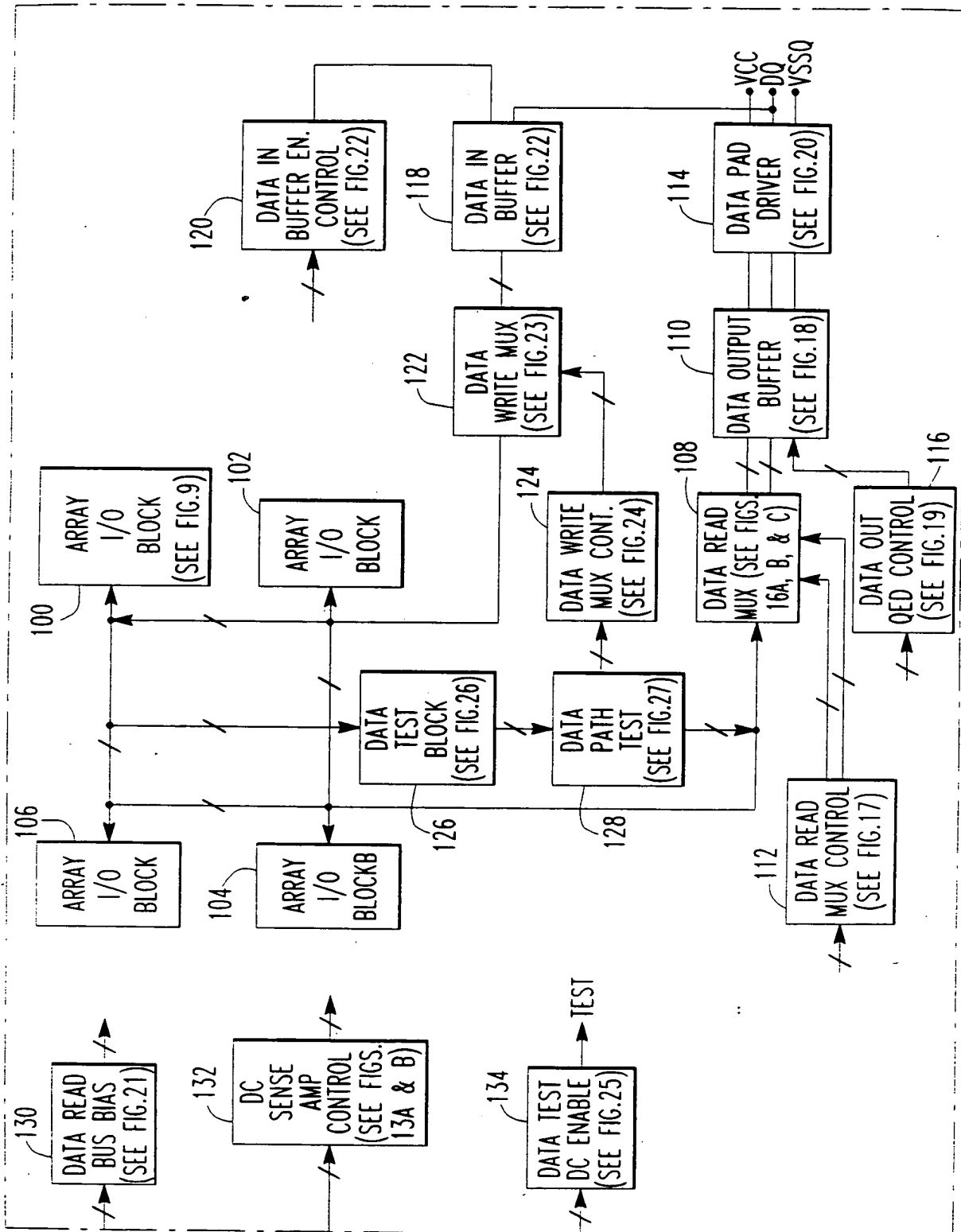


FIG. 8

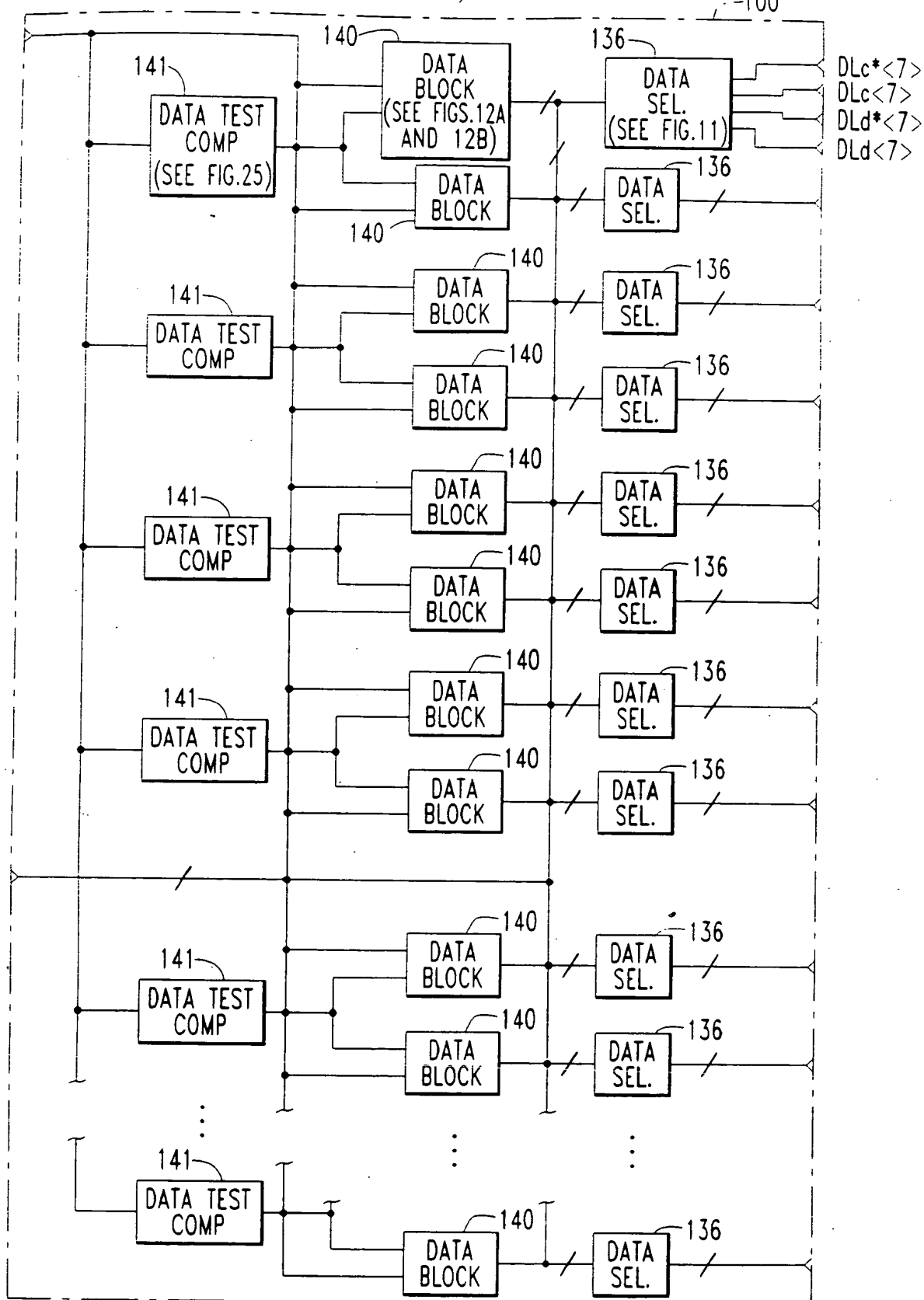


FIG. 9

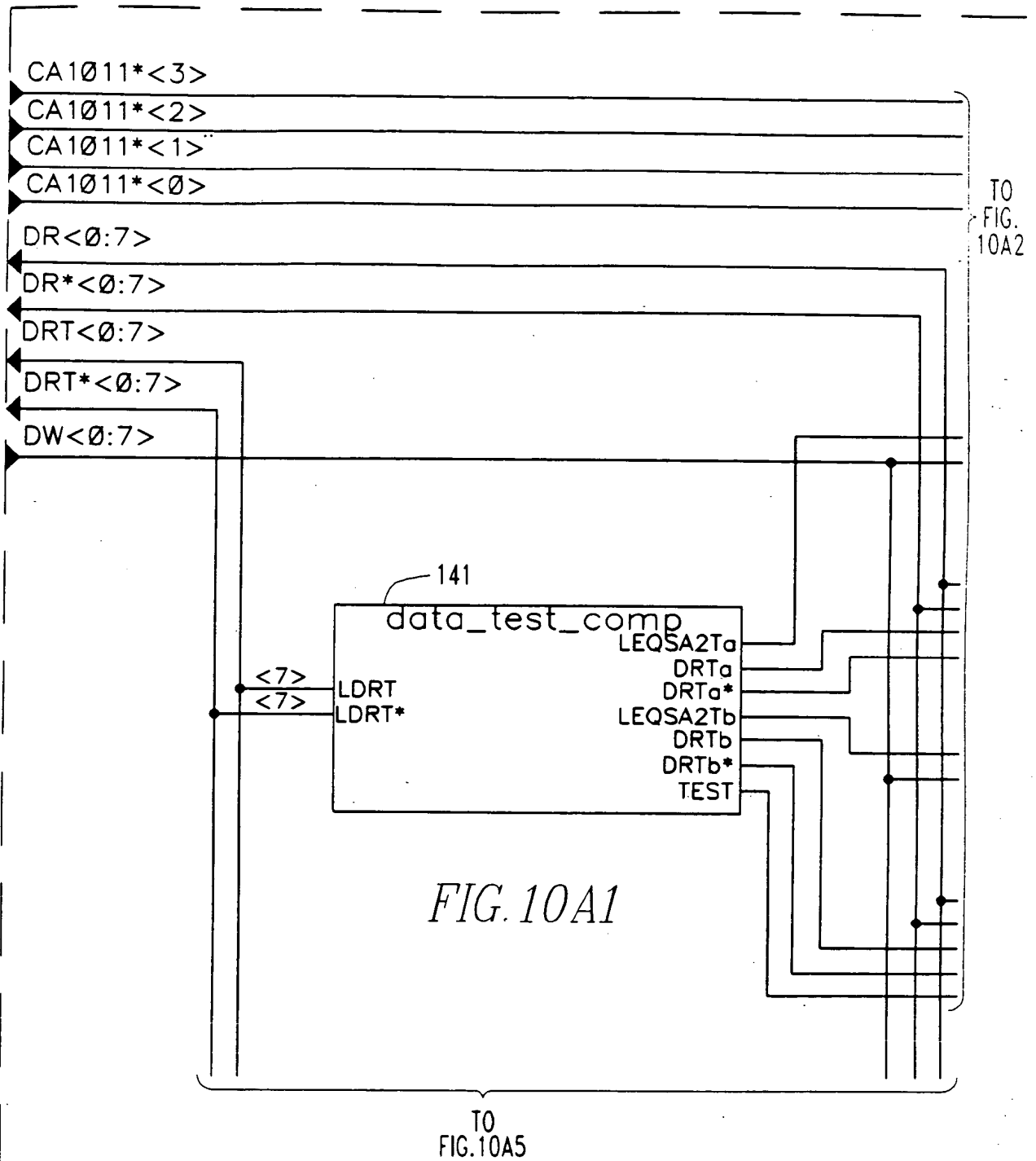
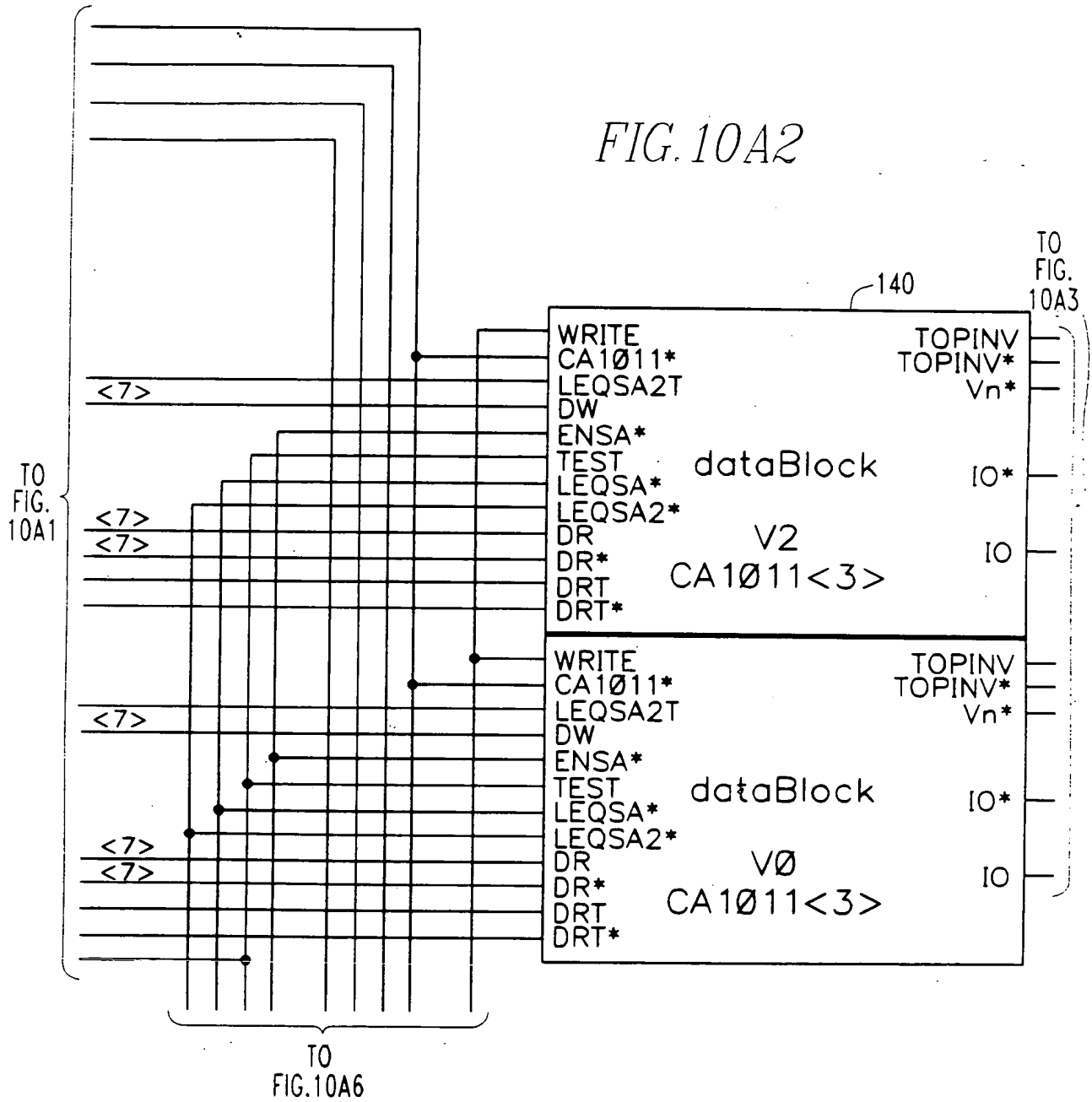
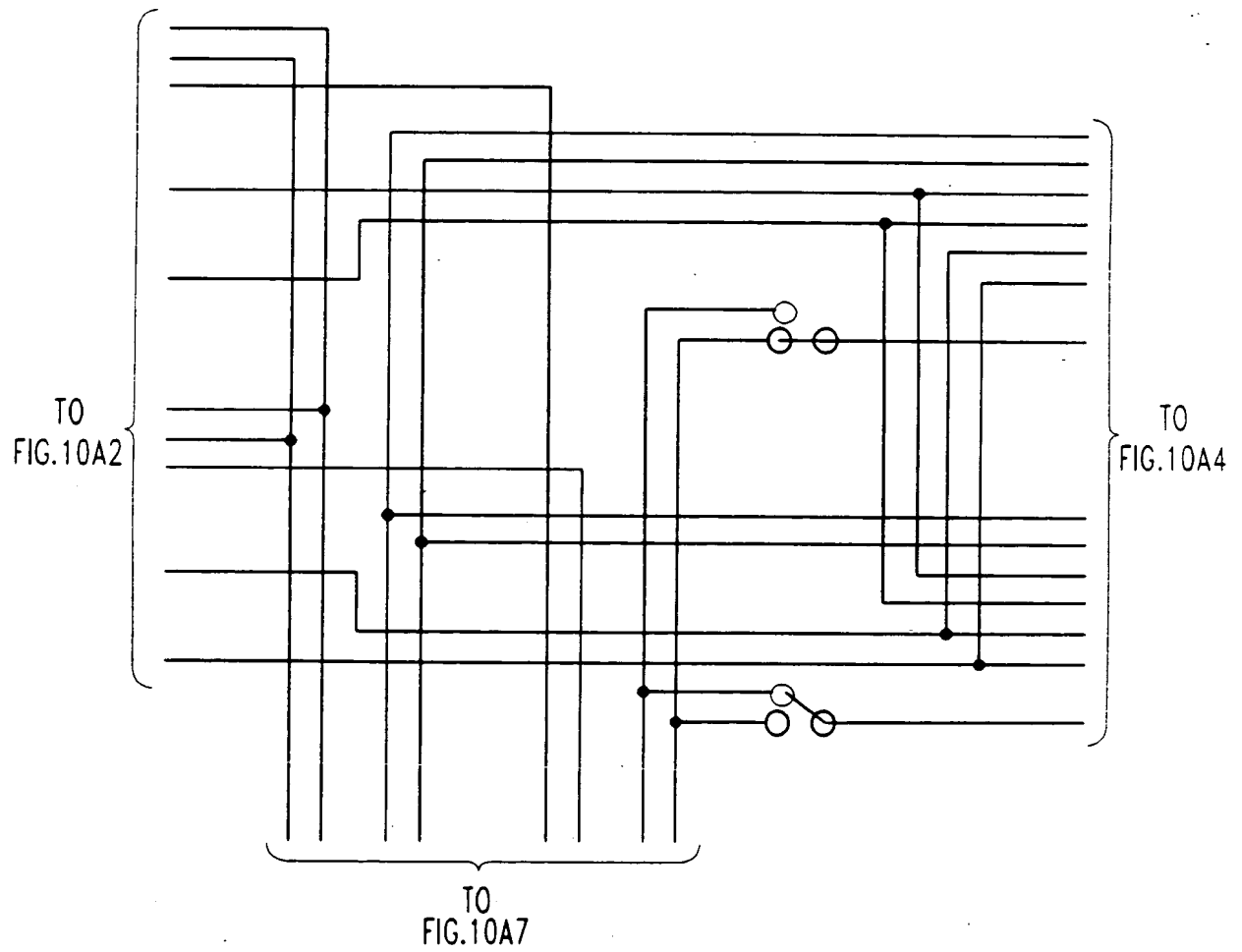


FIG. 10A2



[illegible]

arrayIOBlock

100

FIG. 10A4

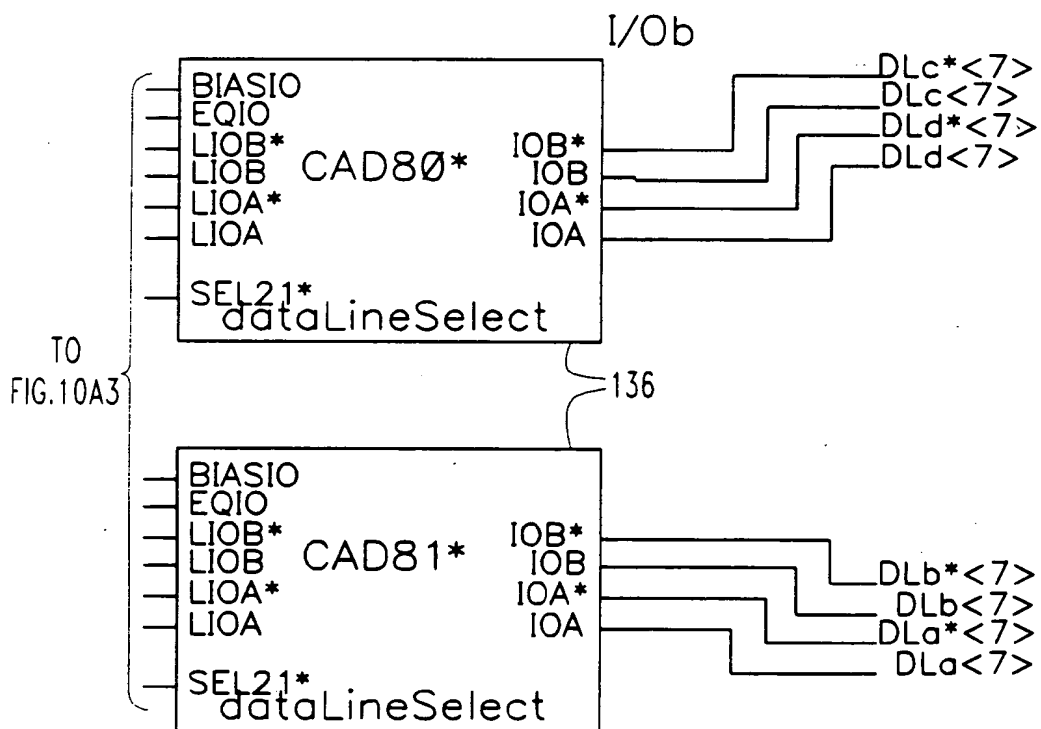


FIG. 10A5

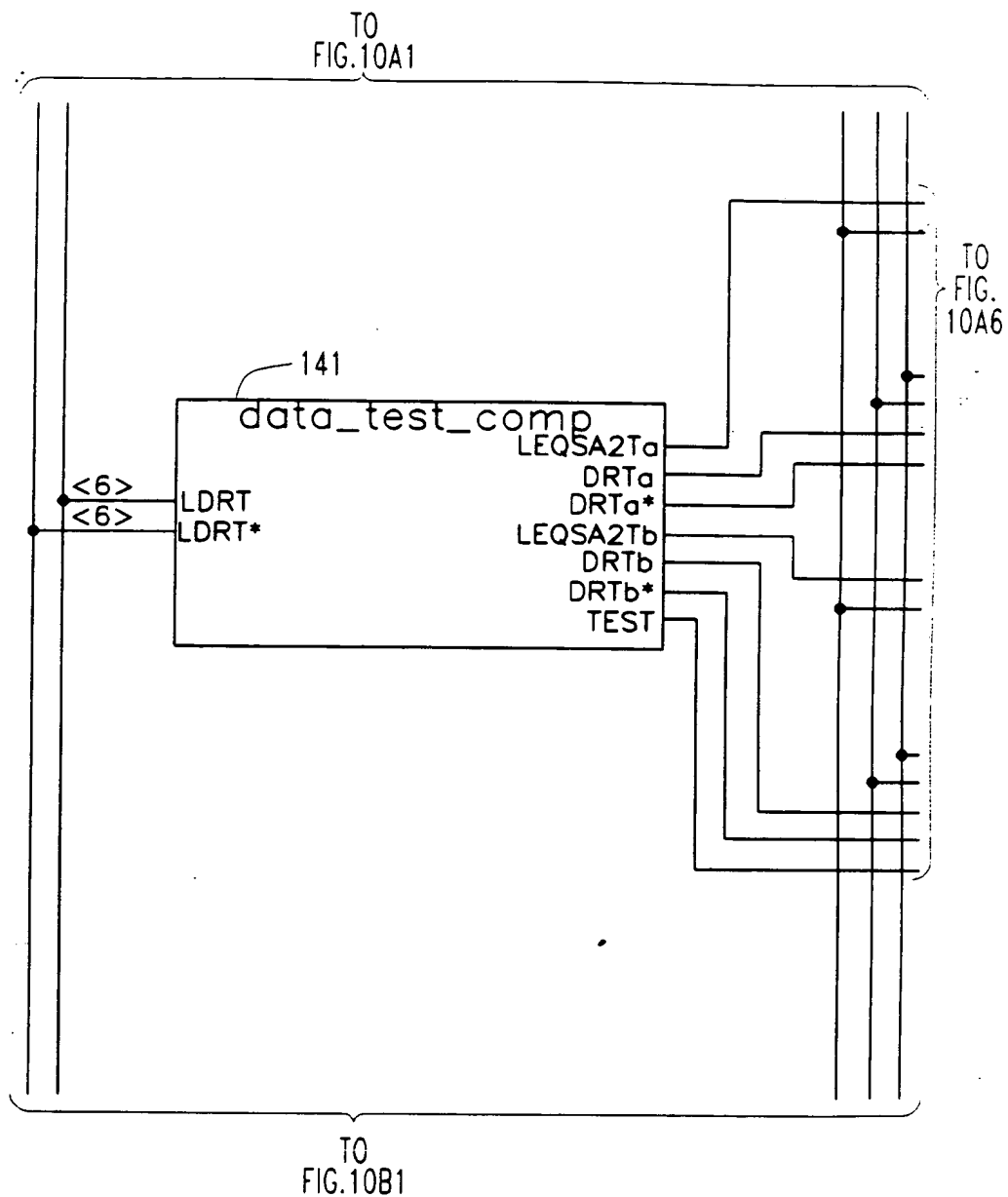


FIG. 10A5

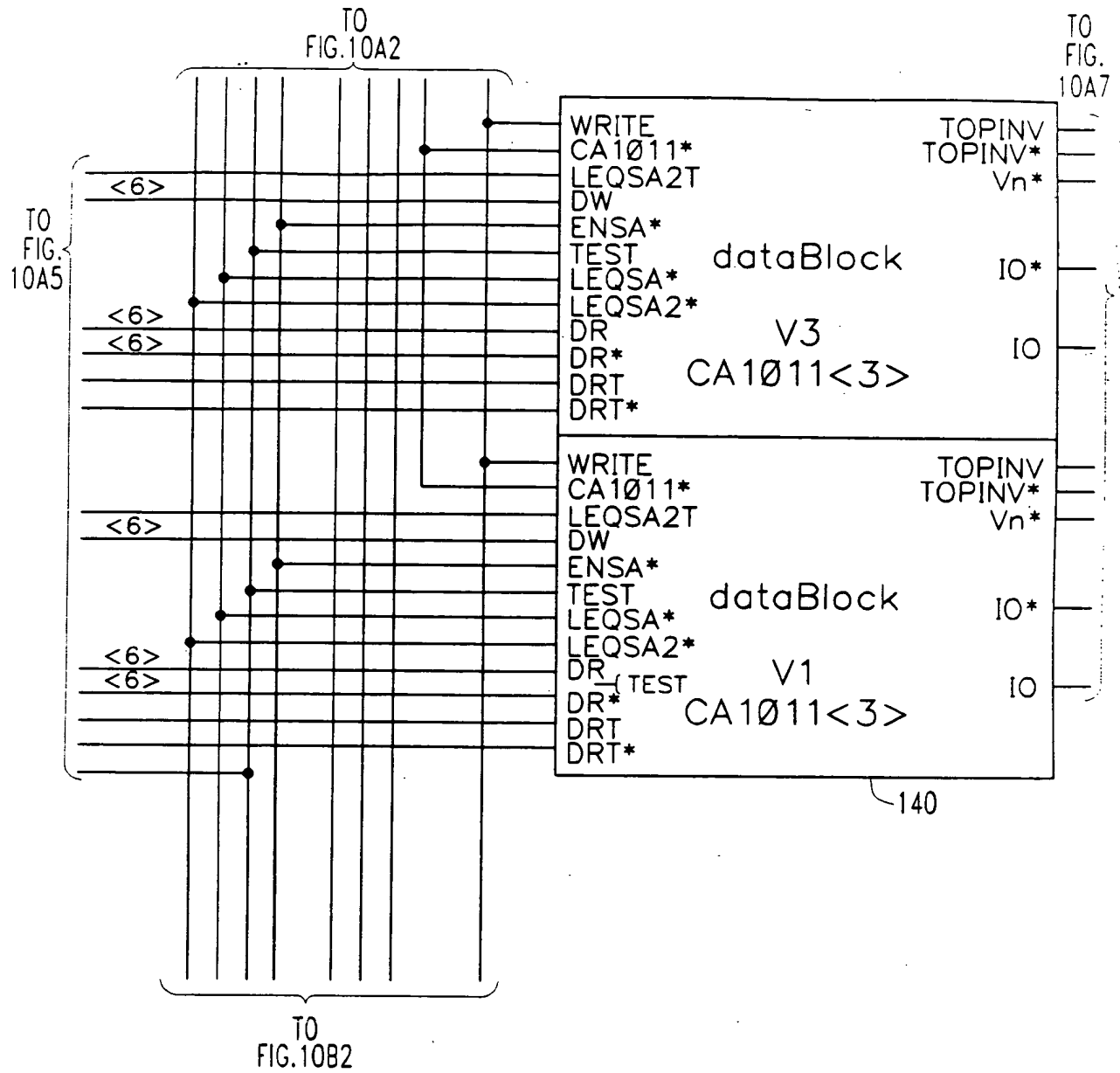


FIG. 10A6

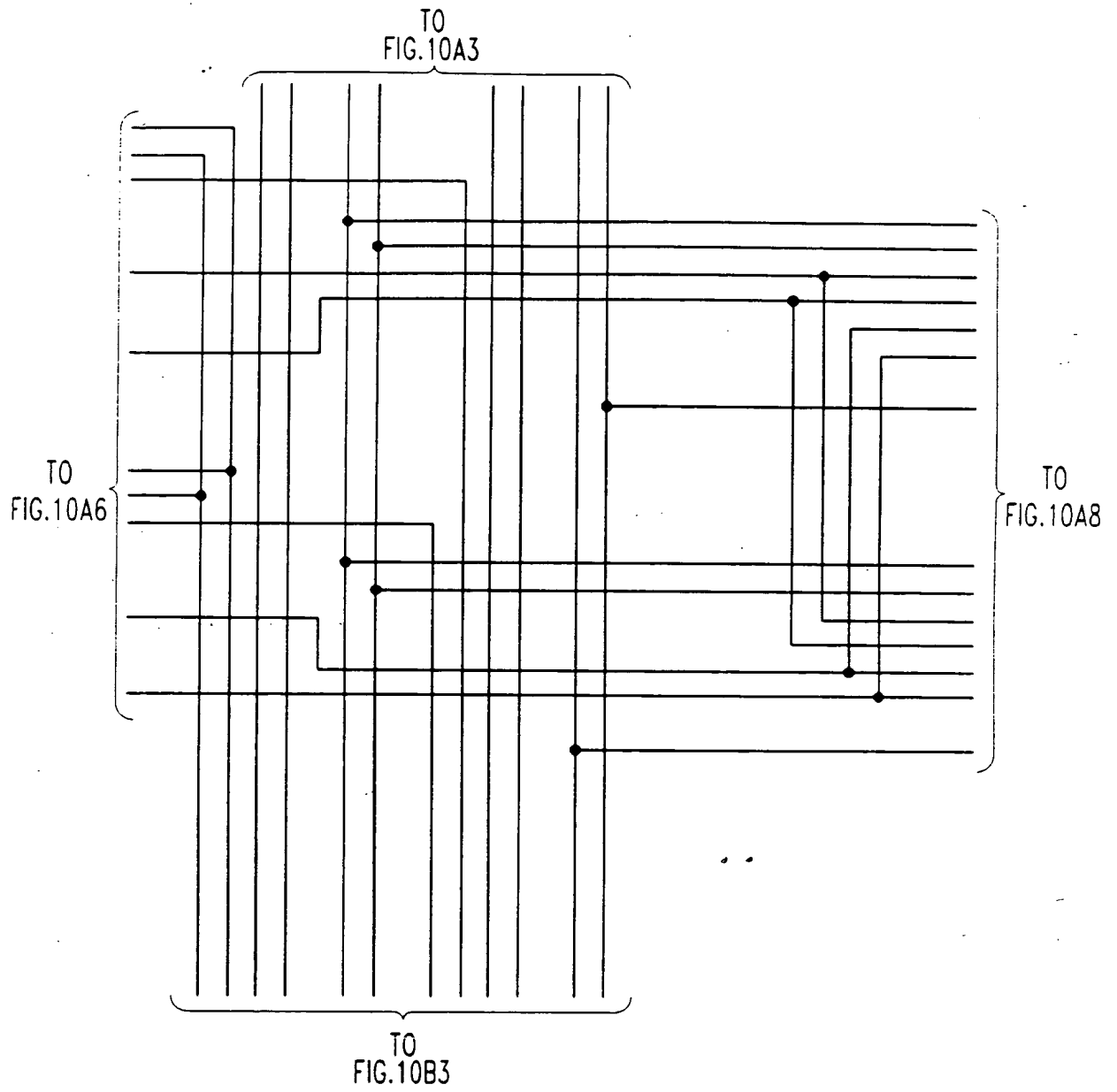


FIG. 10A7

FIG. 10A7

I/Oa

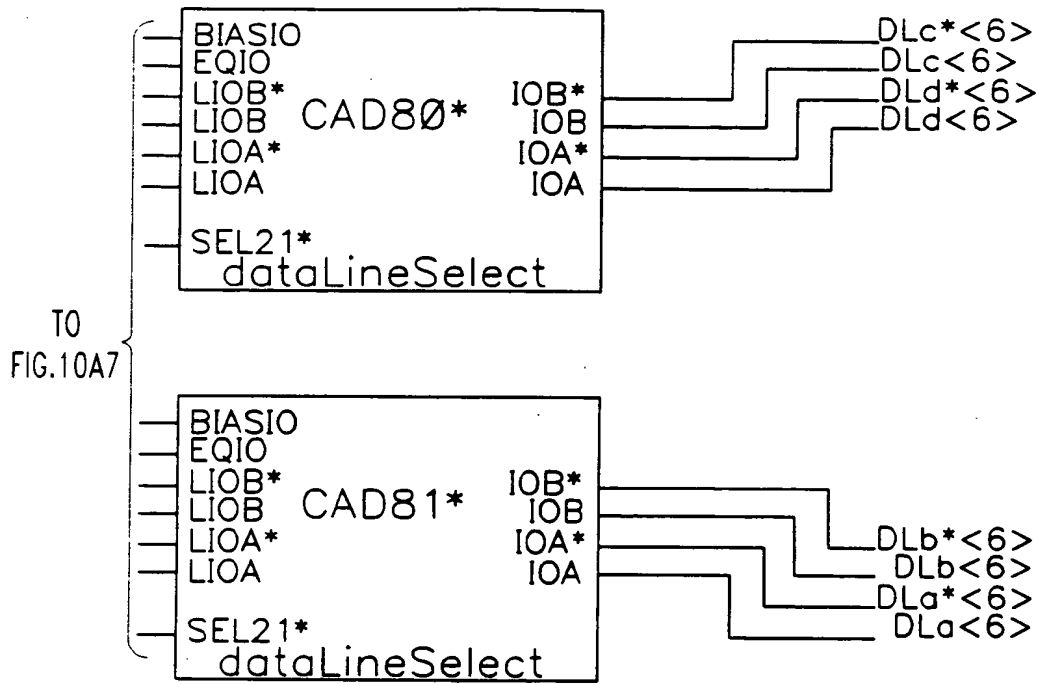


FIG.10A8

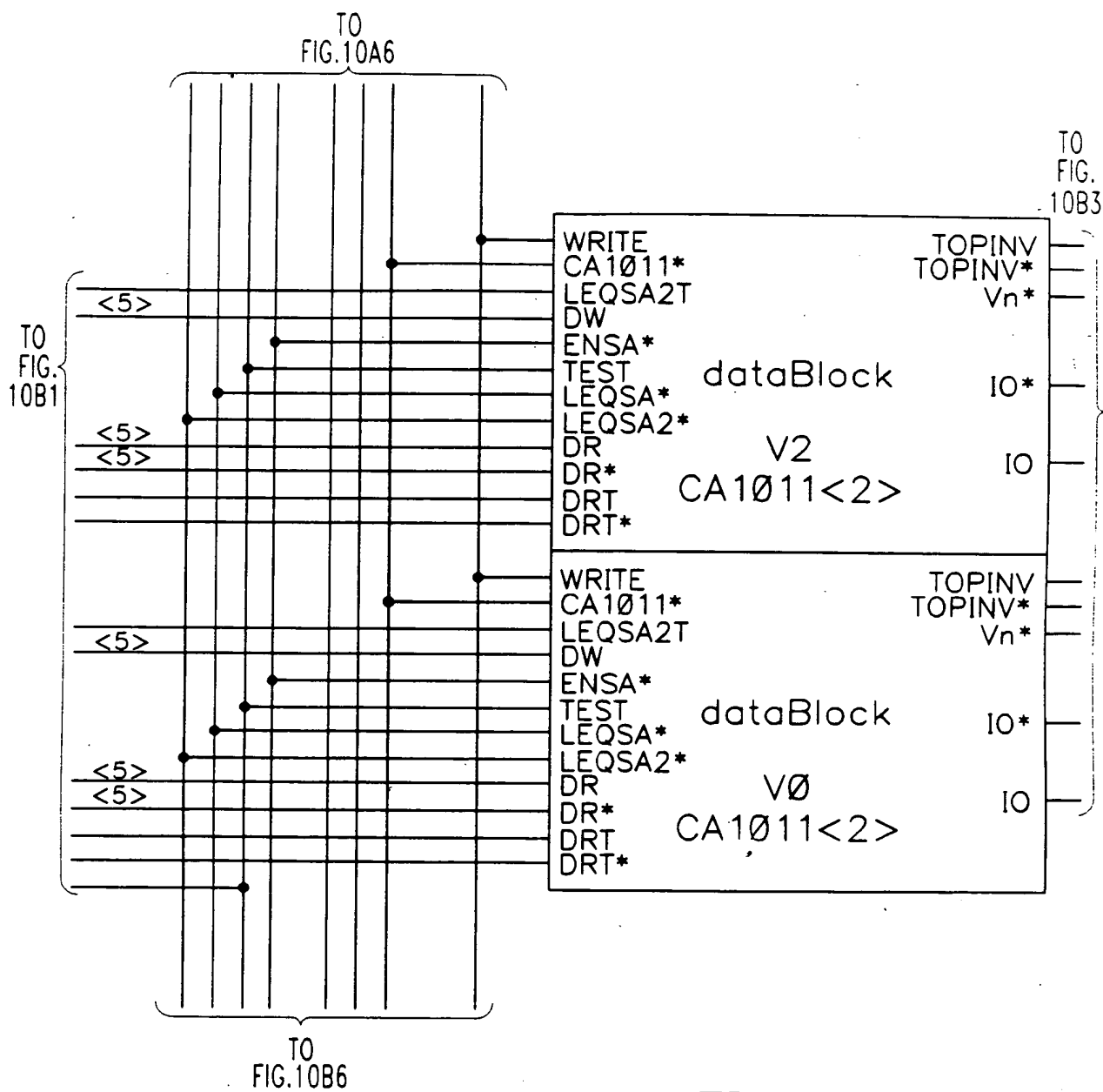


FIG. 10B2

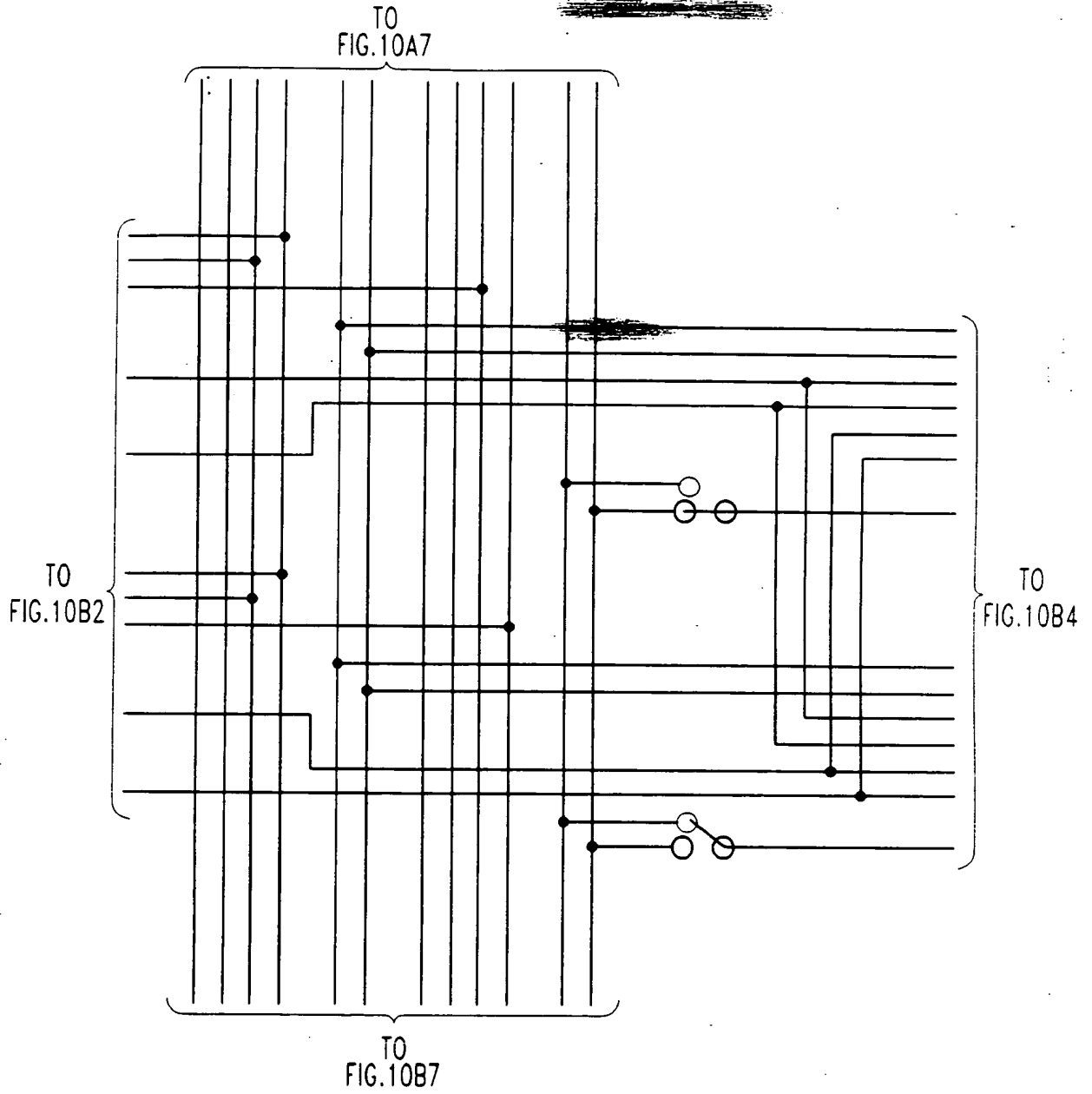


FIG. 10B3

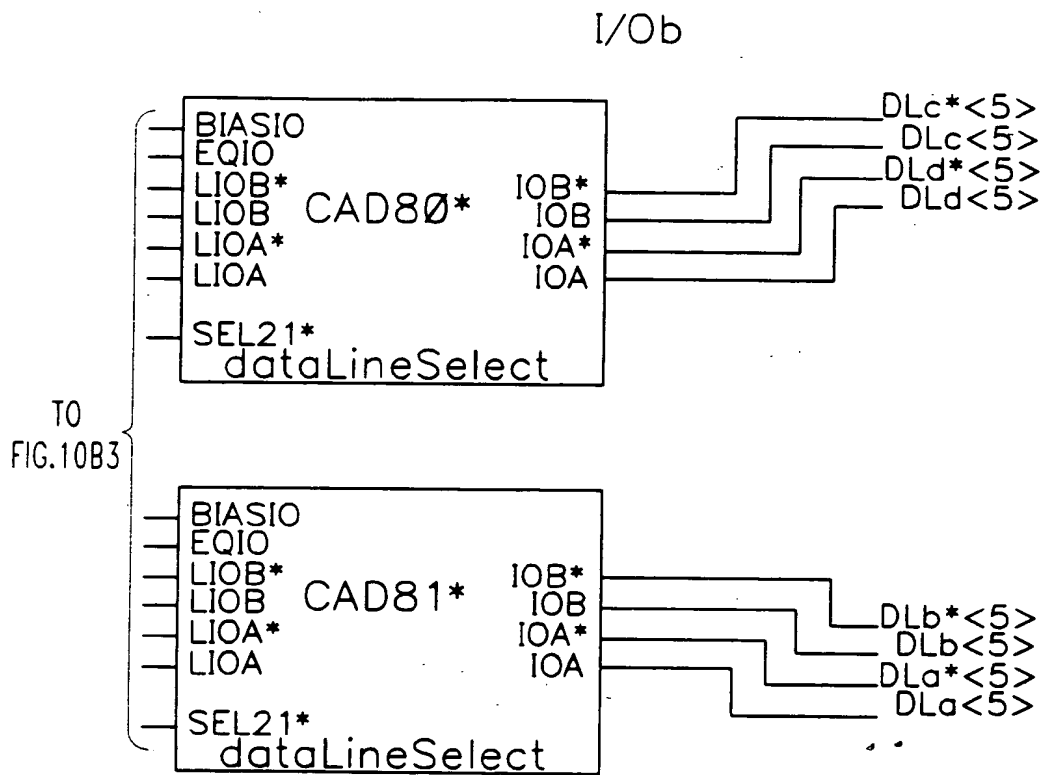


FIG. 10B4

FIG. 10B5

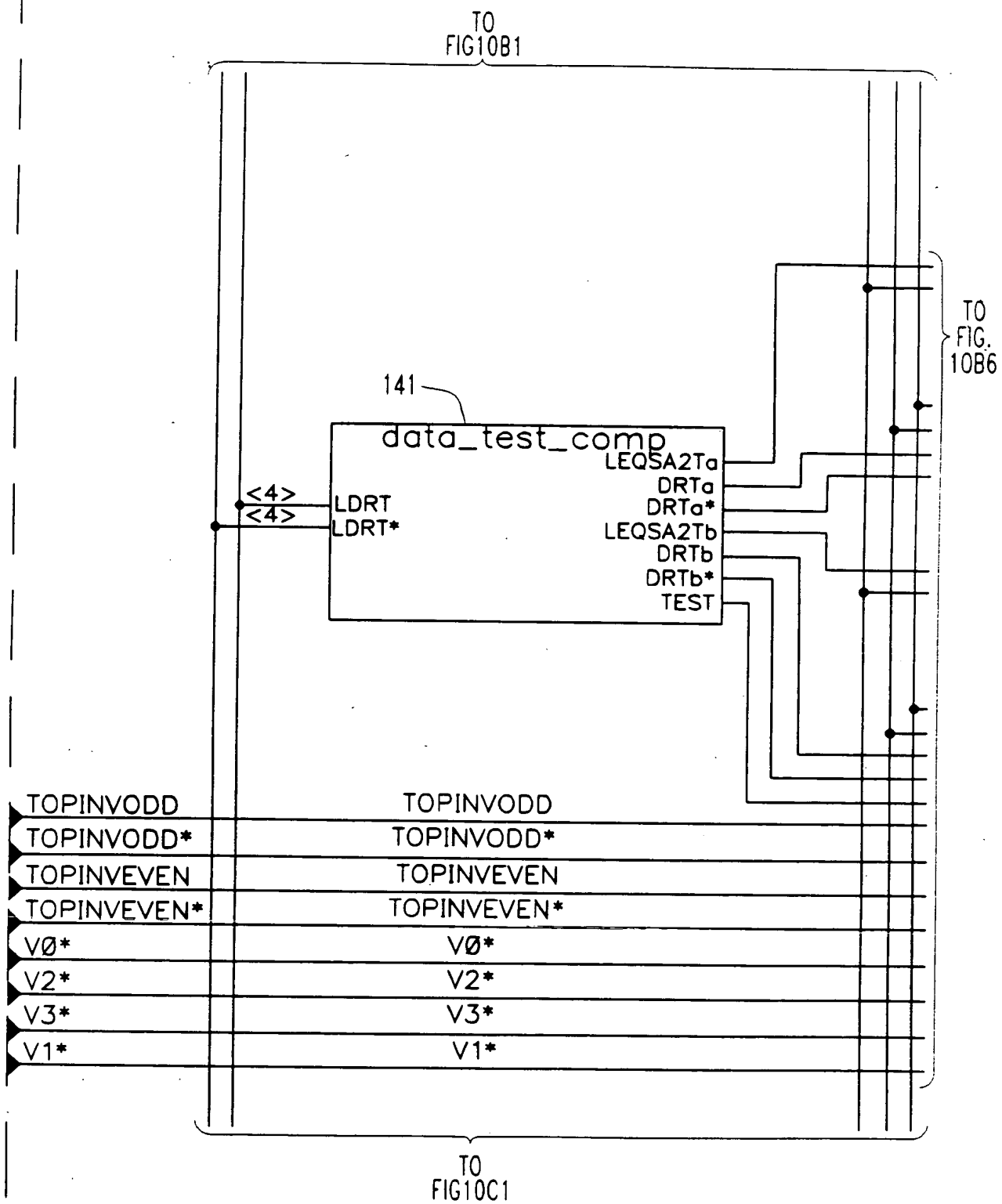


FIG. 10B6

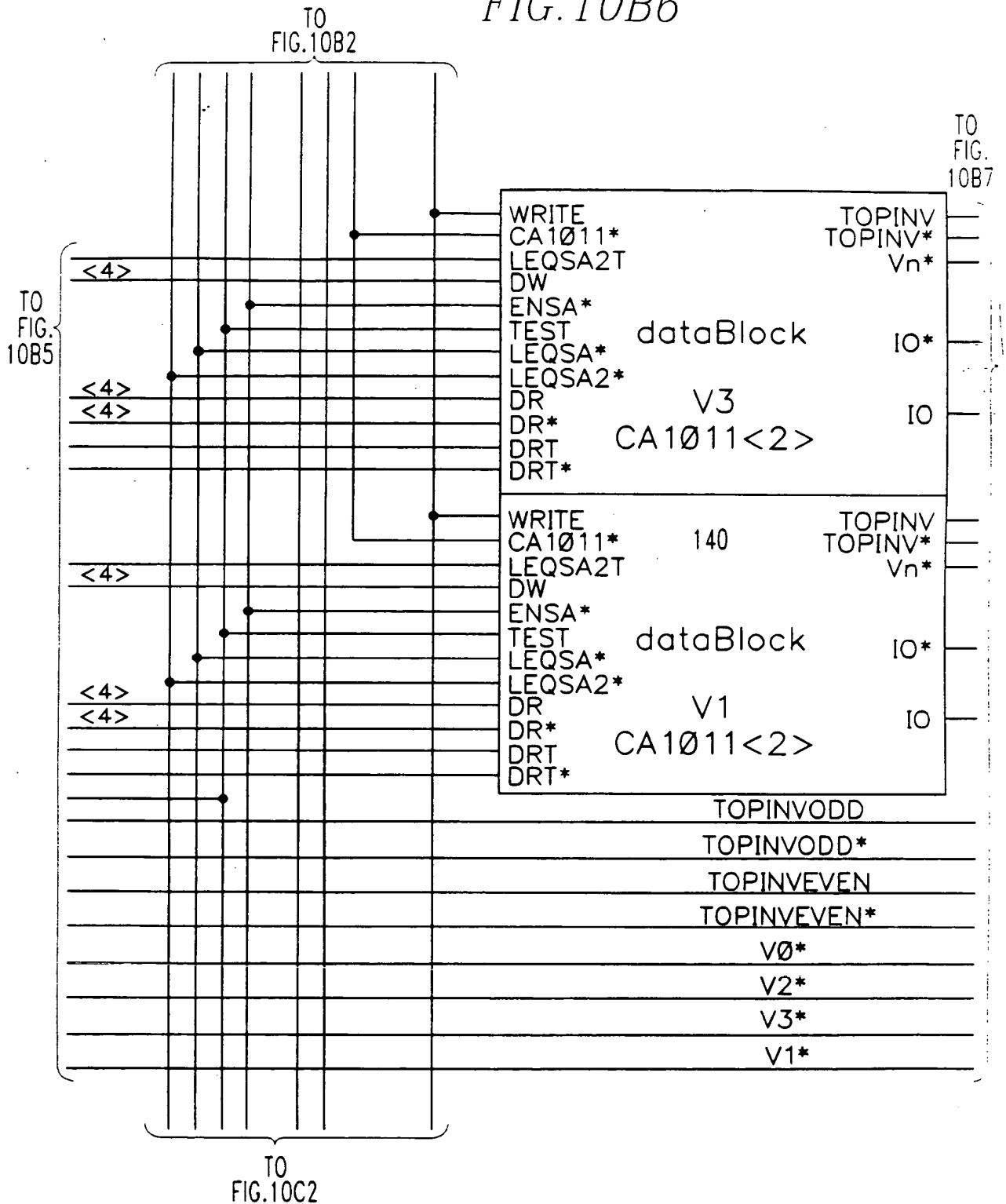
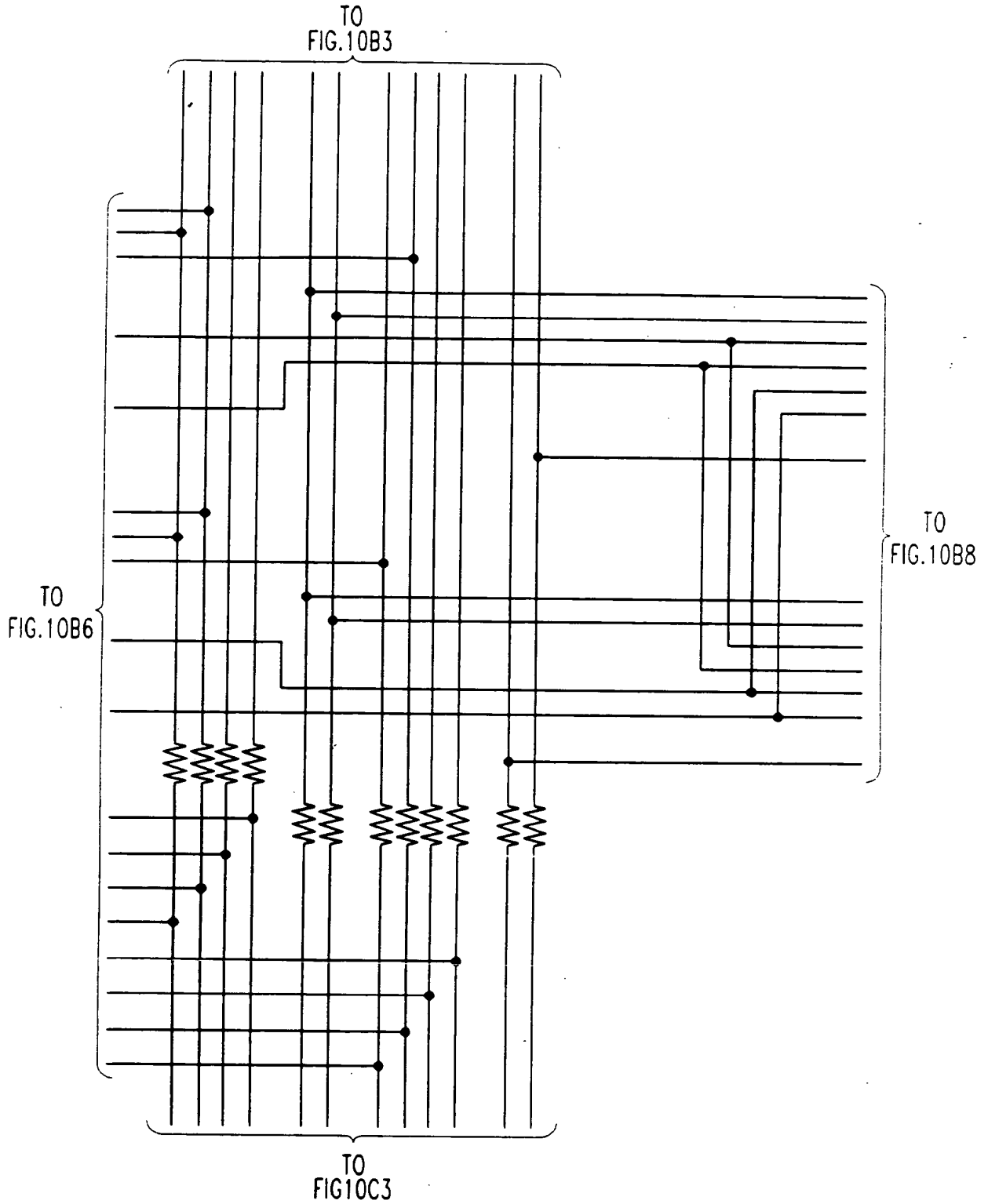
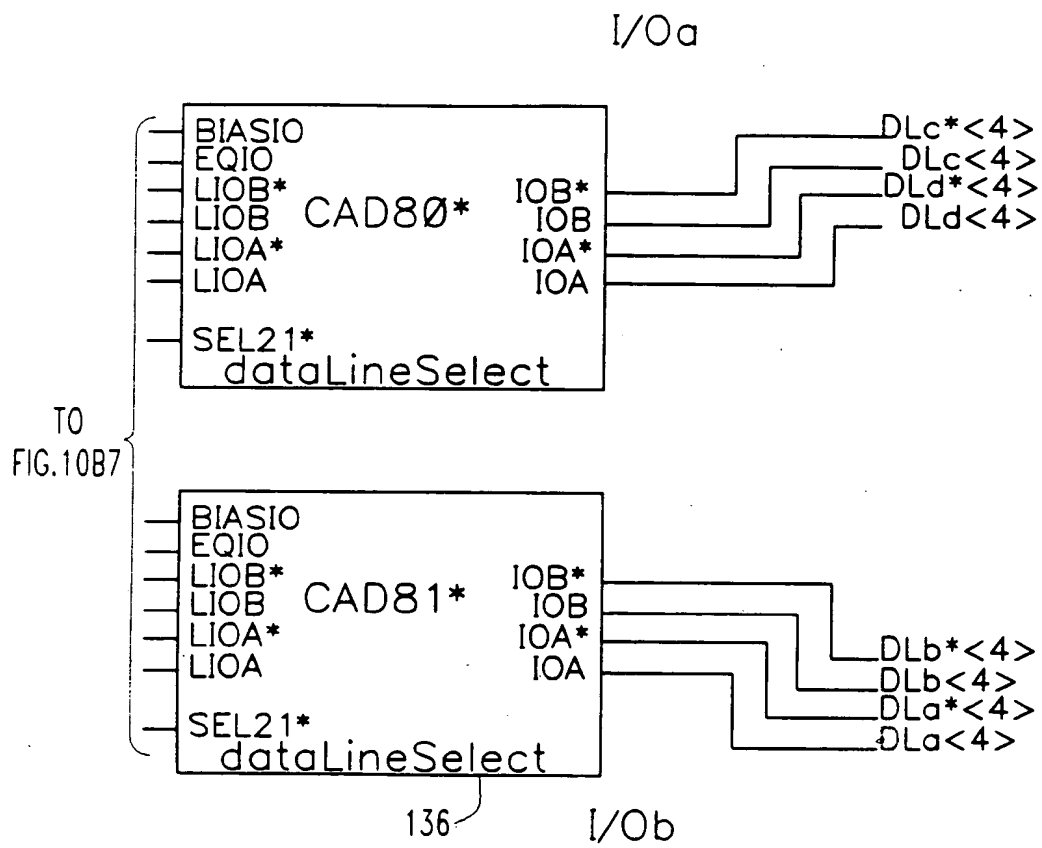


FIG. 10B7

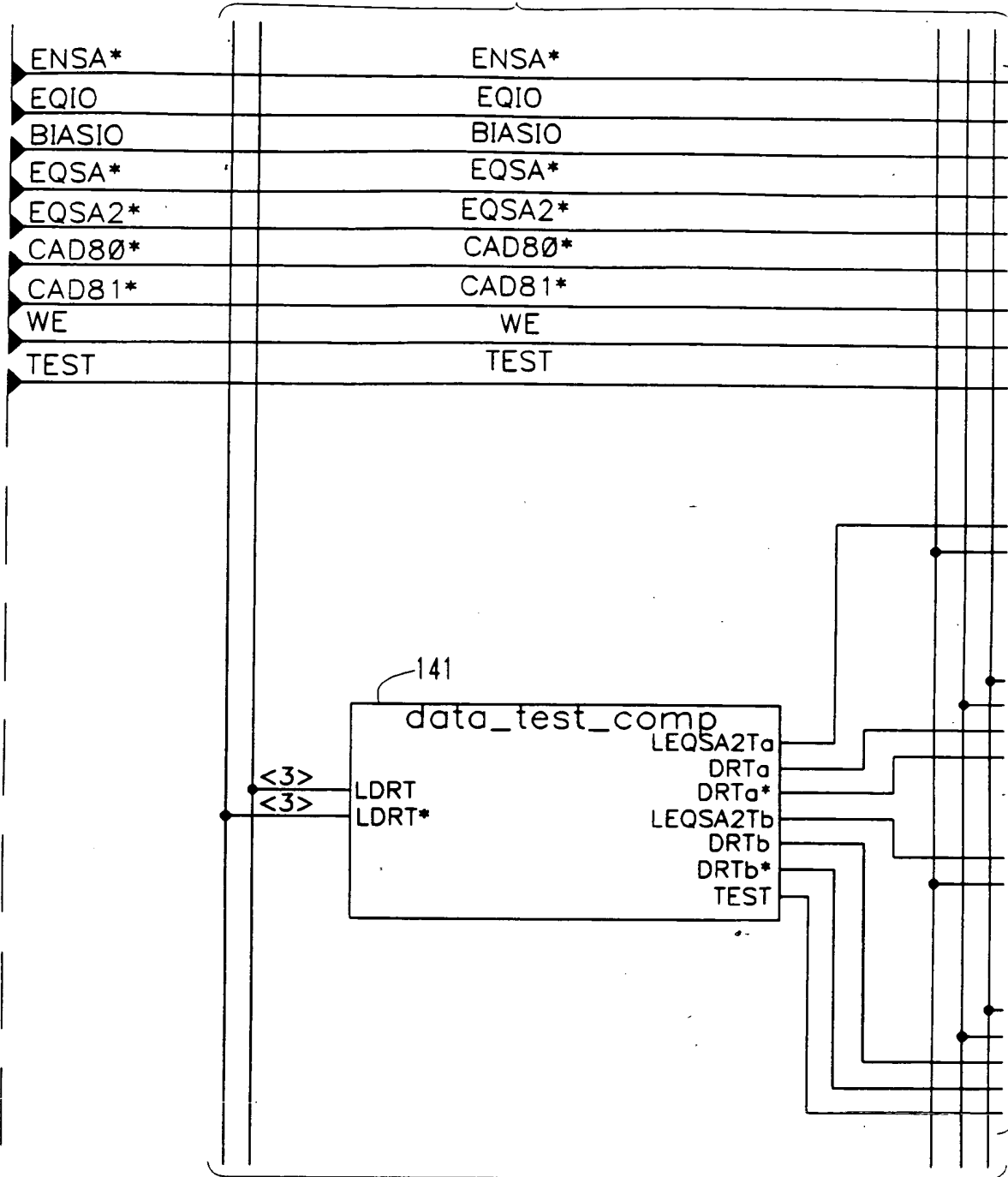


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FIG. 10B8



TO
FIG.
10C2



TO
FIG.10C5

FIG. 10C1

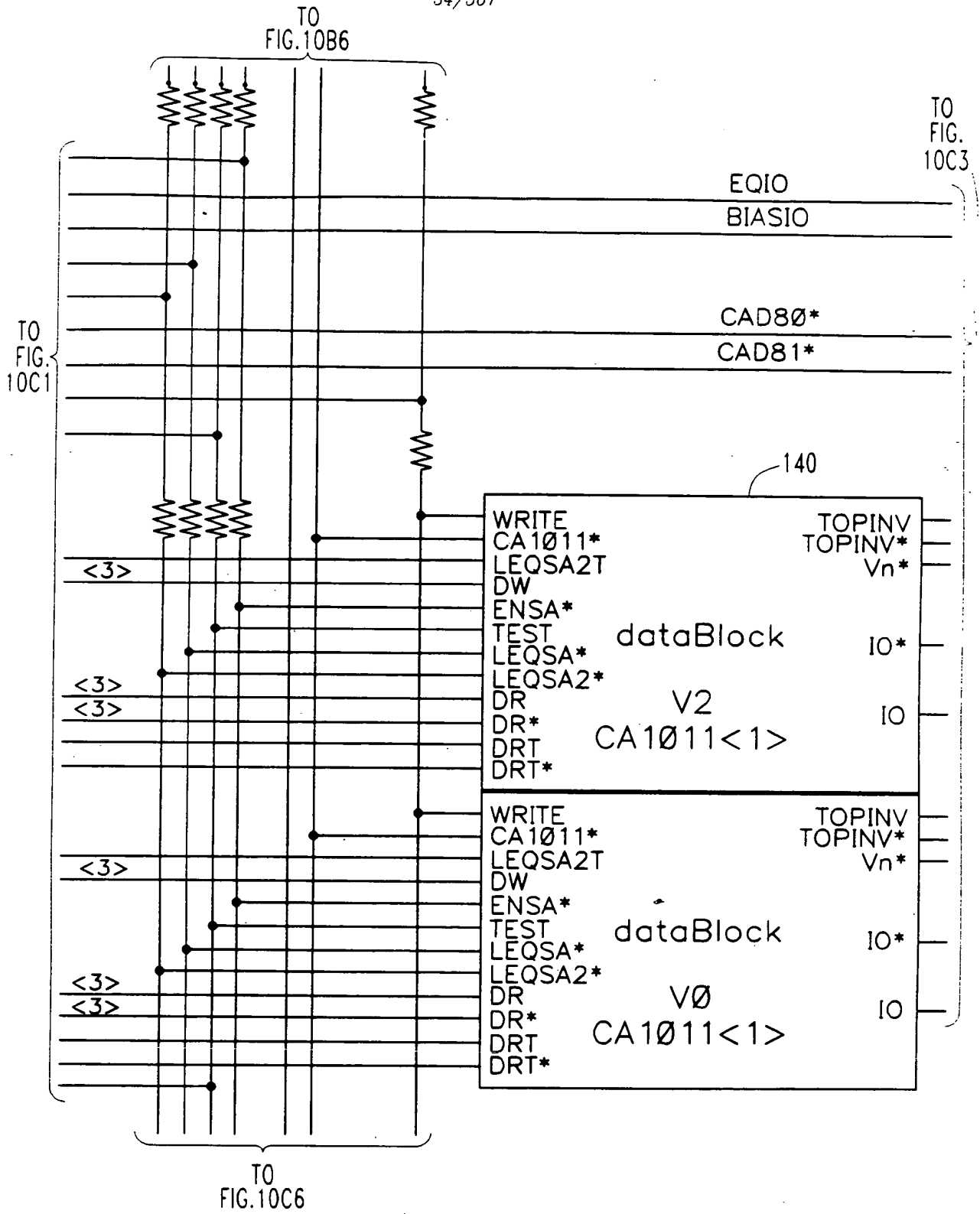


FIG. 10C2

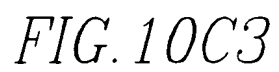
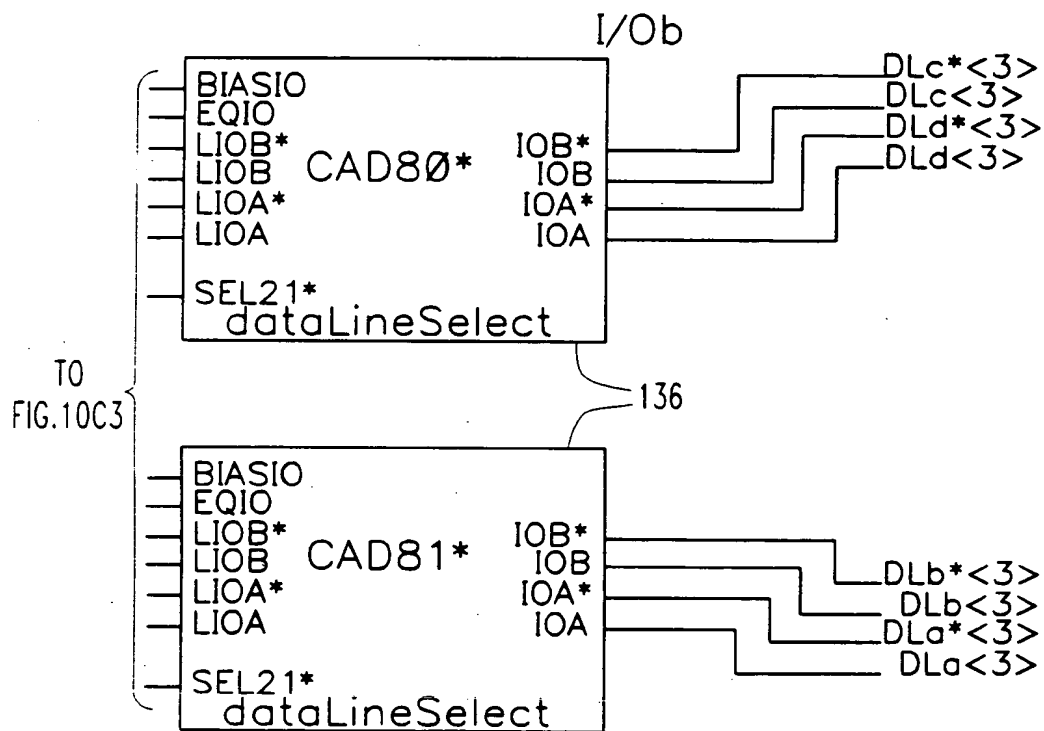


FIG. 10C4



003475-08201

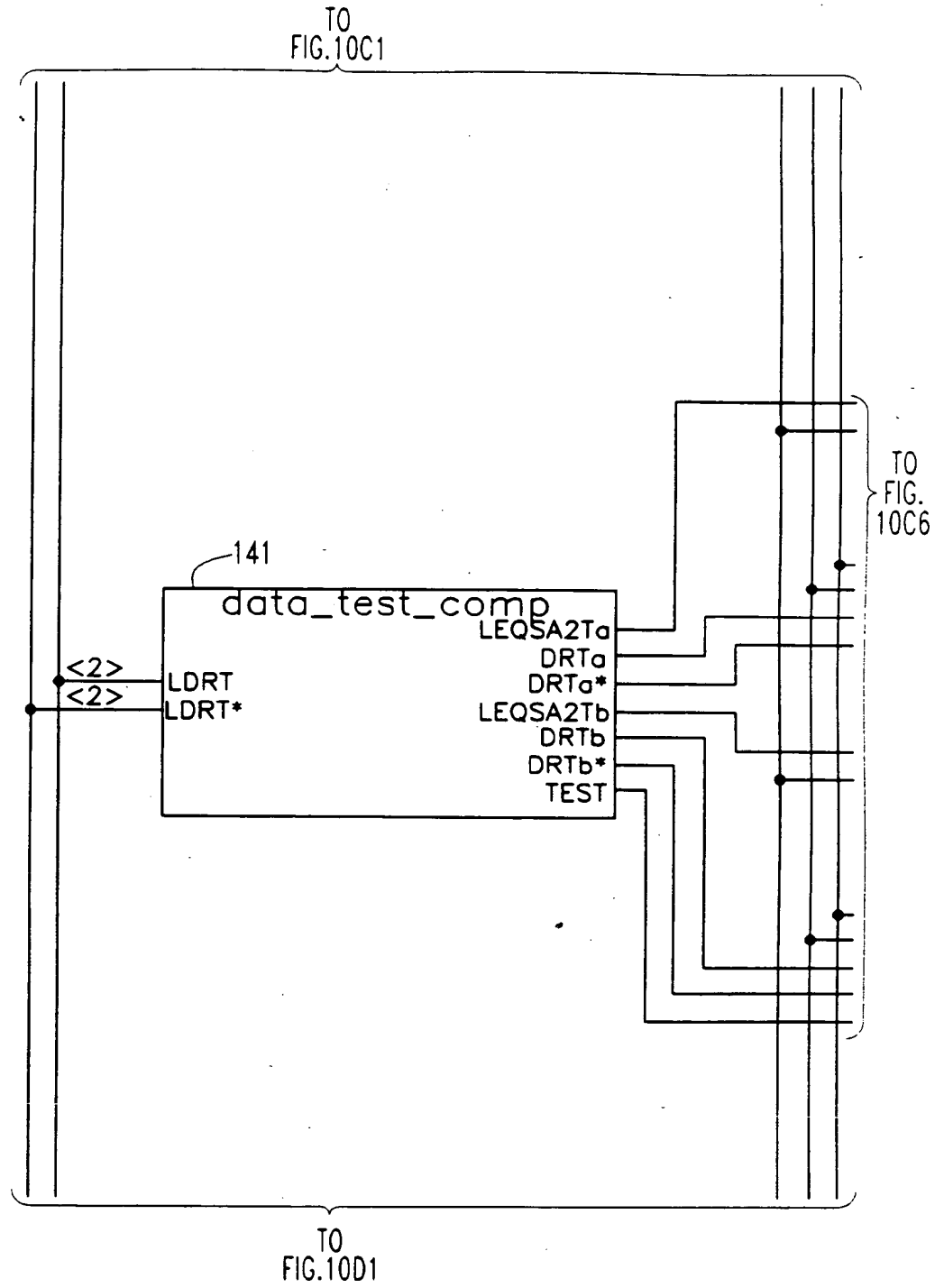


FIG. 10C5

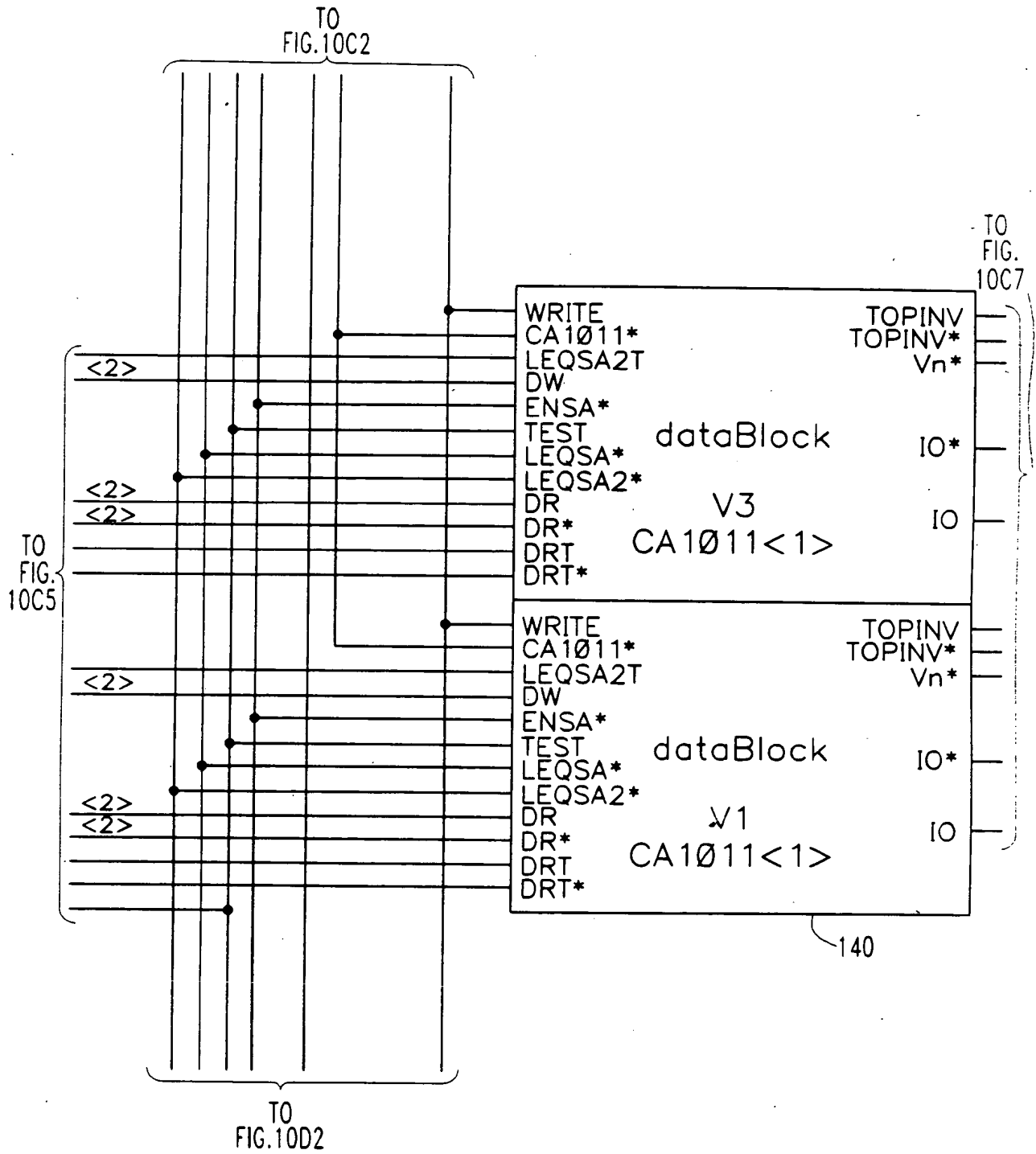


FIG. 10C6

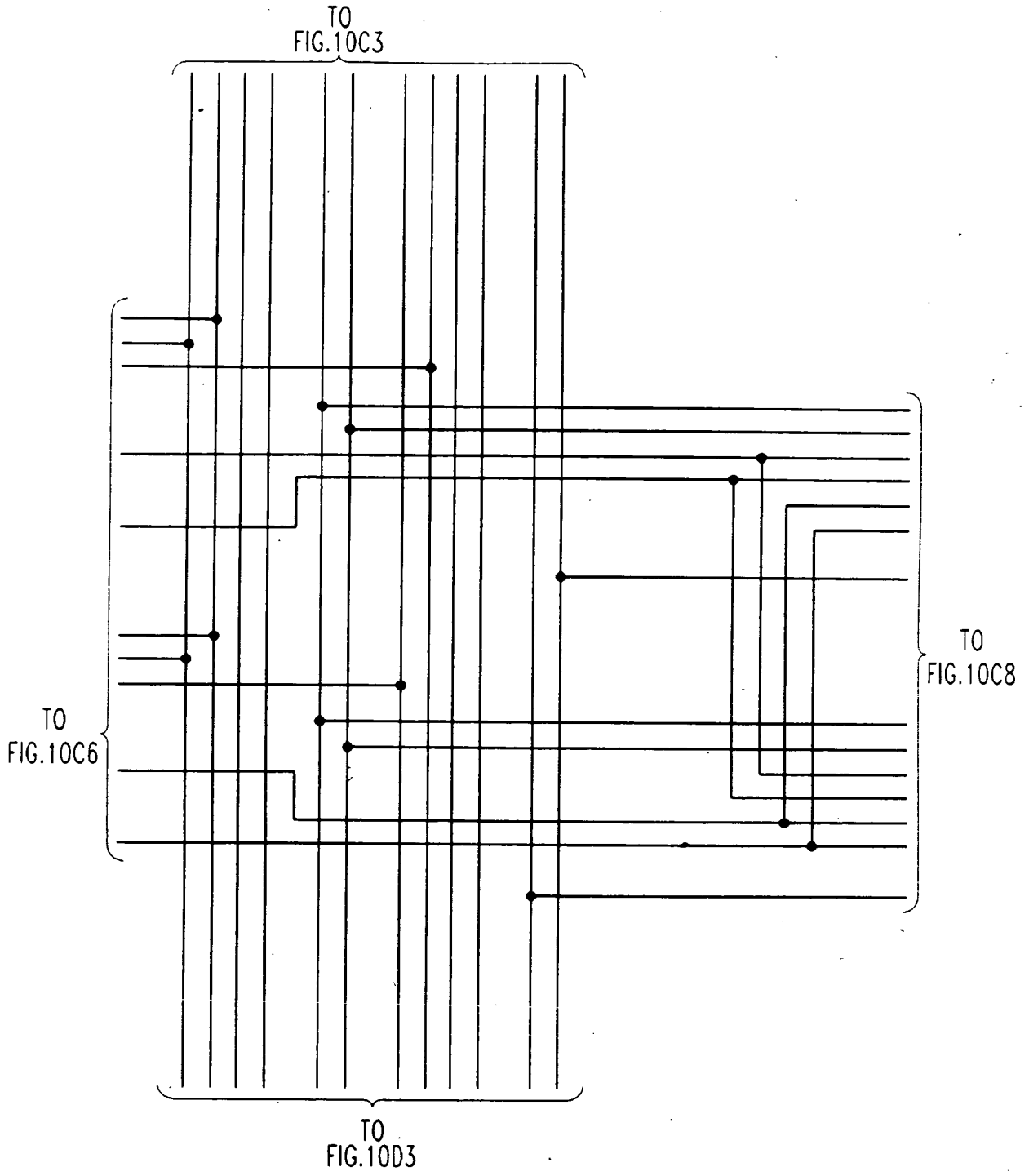


FIG. 10C7

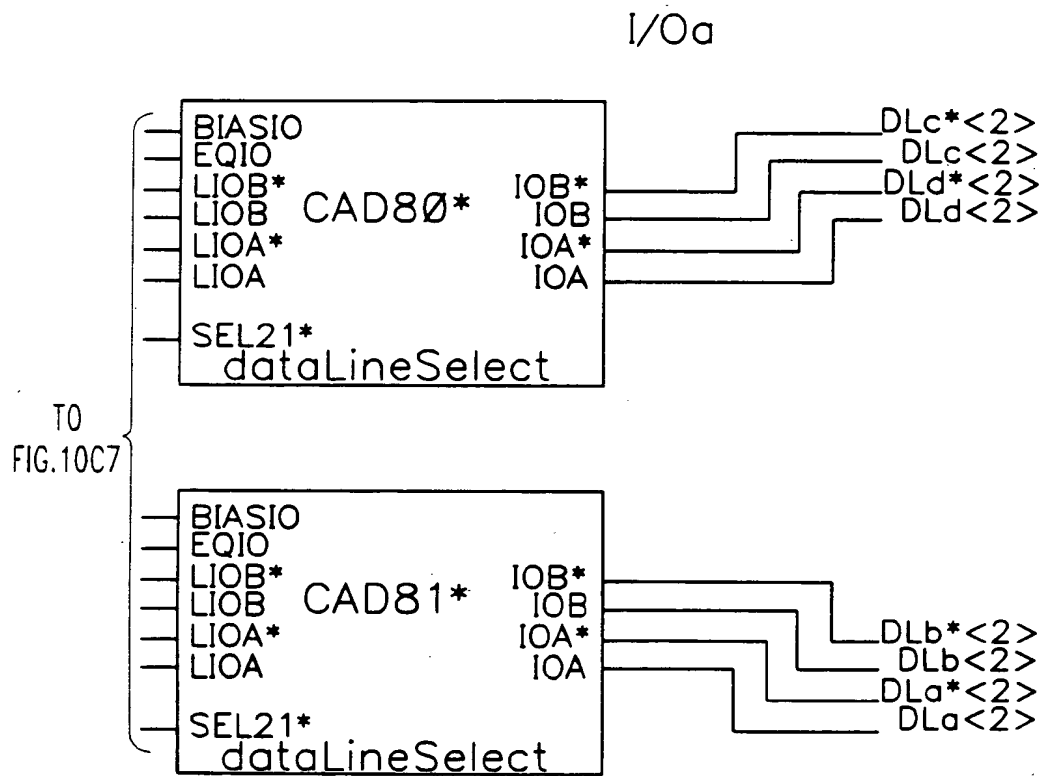


FIG. 10C8

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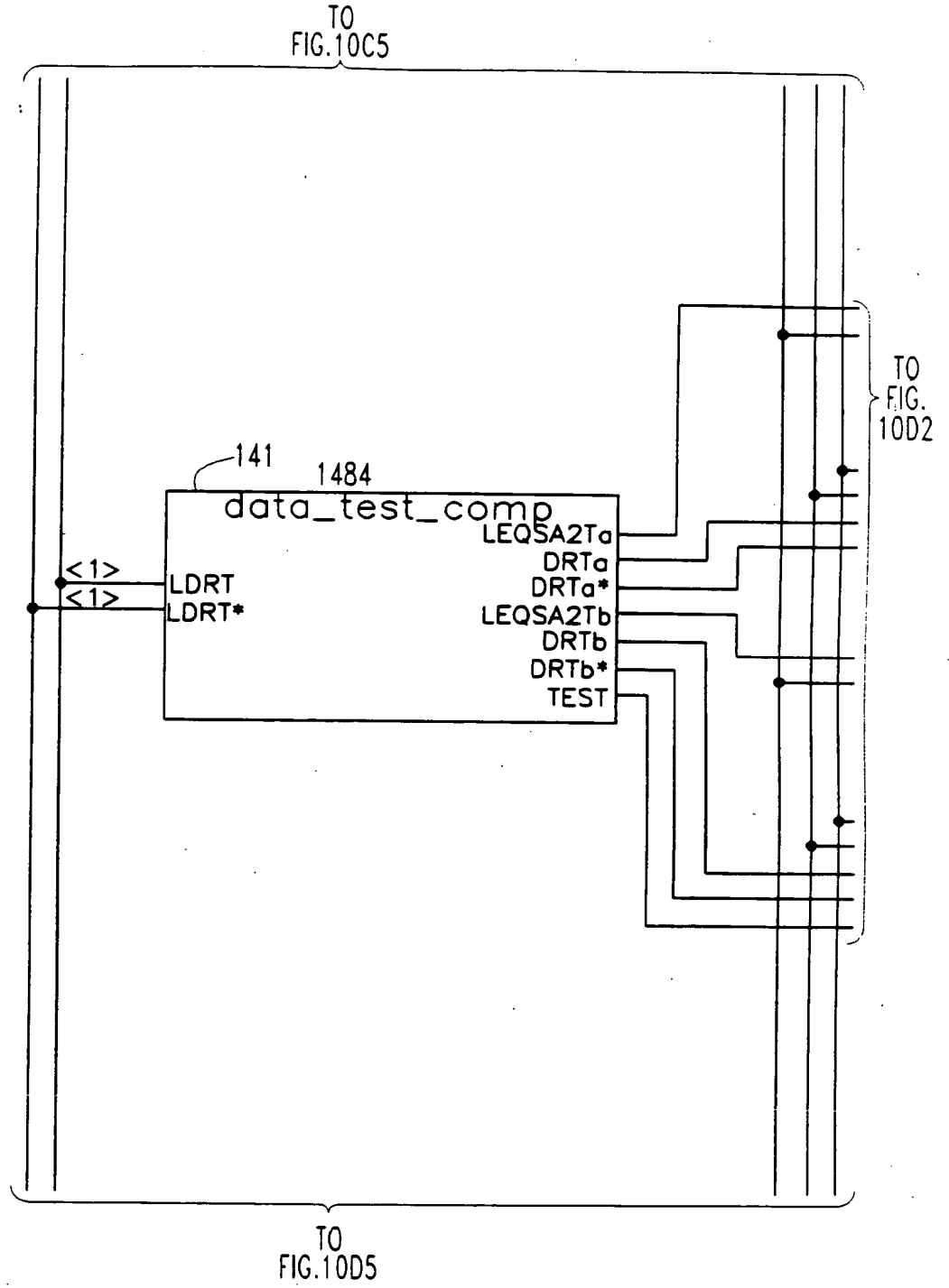
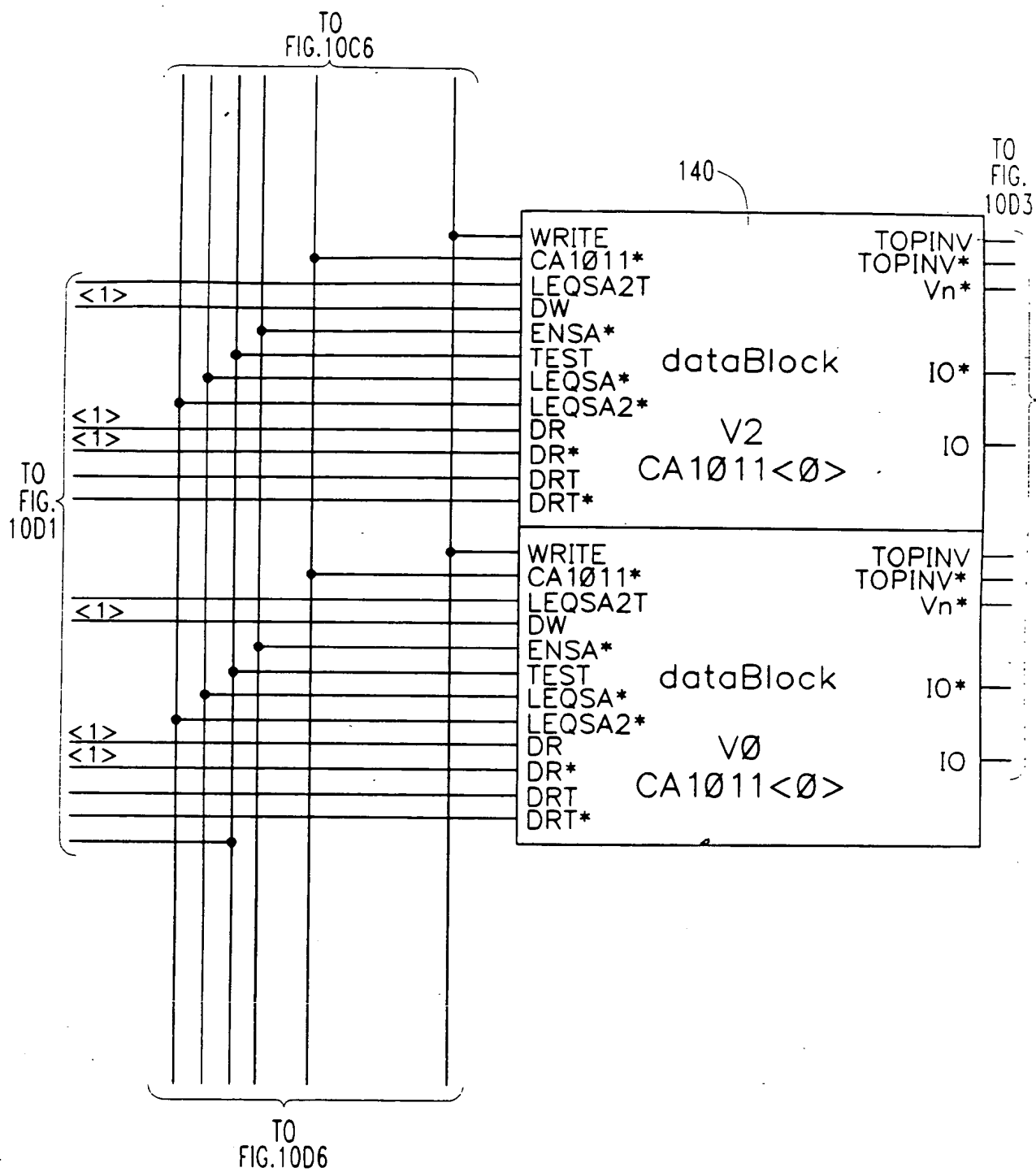


FIG. 10D1



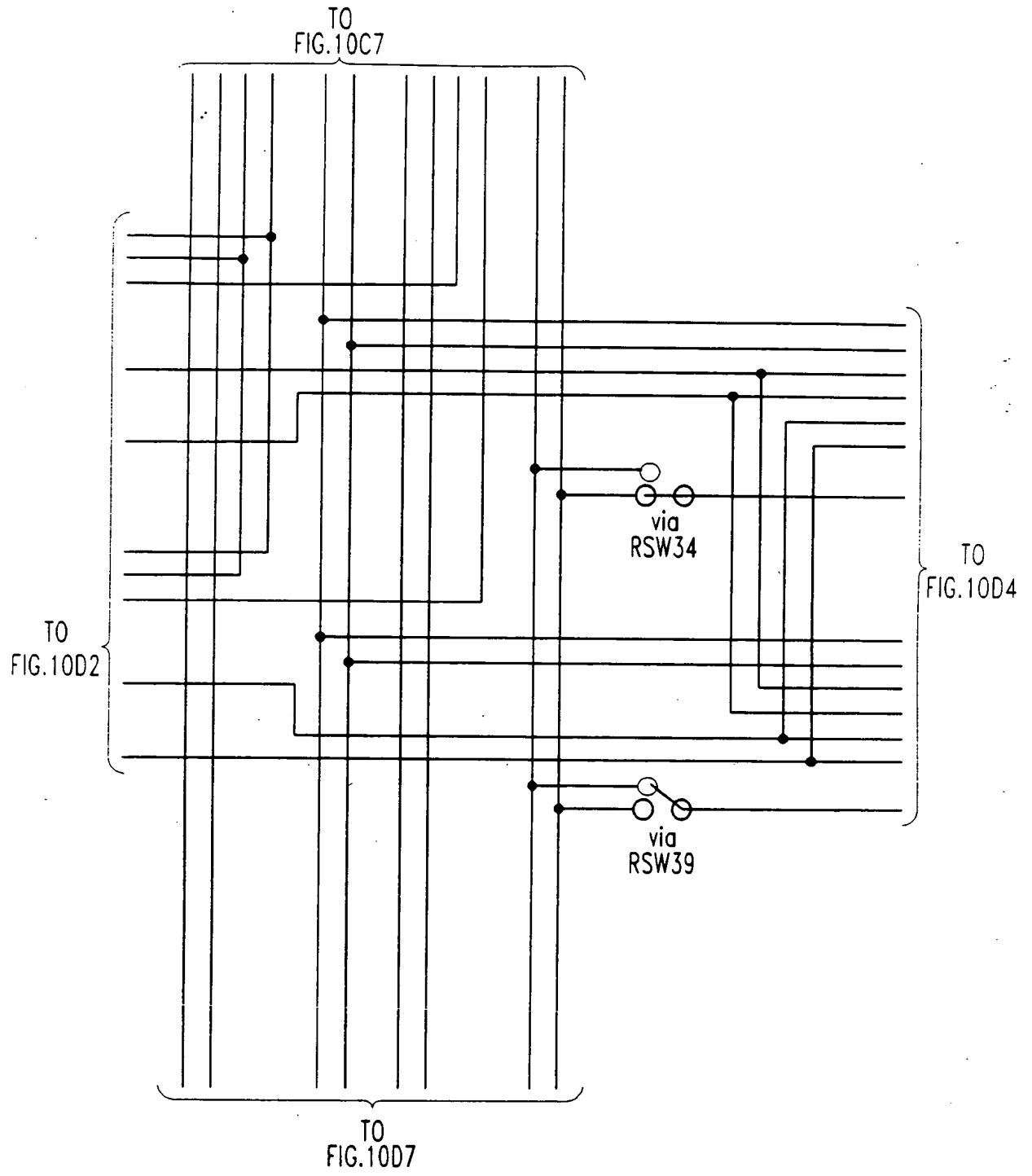


FIG. 10D3

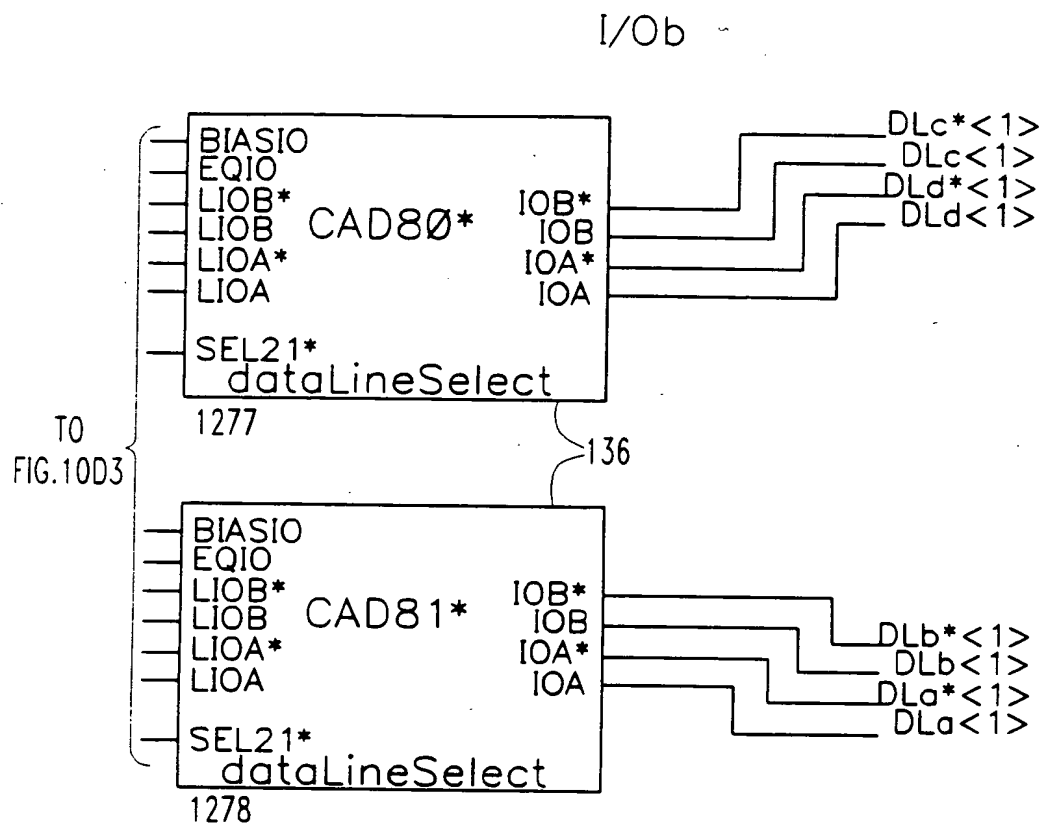


FIG.10D4

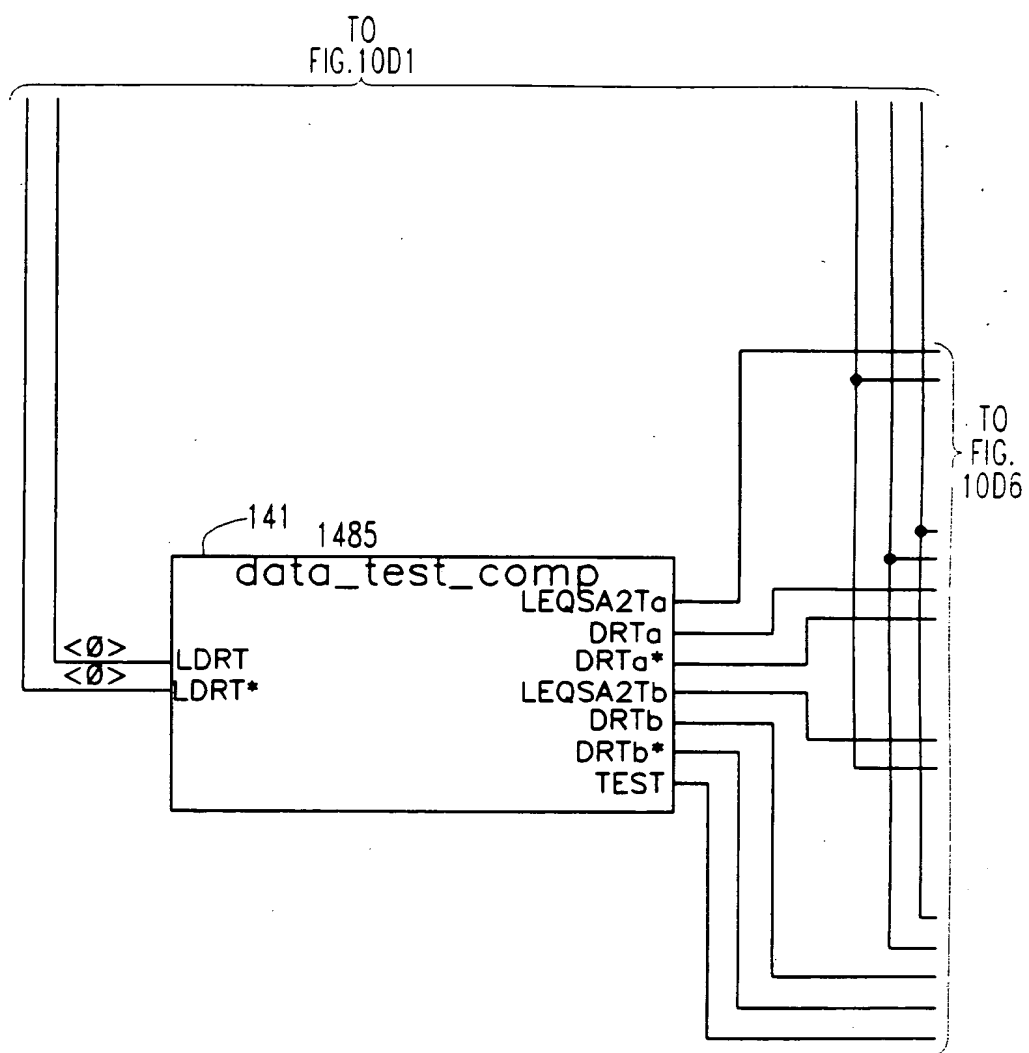


FIG. 10D5

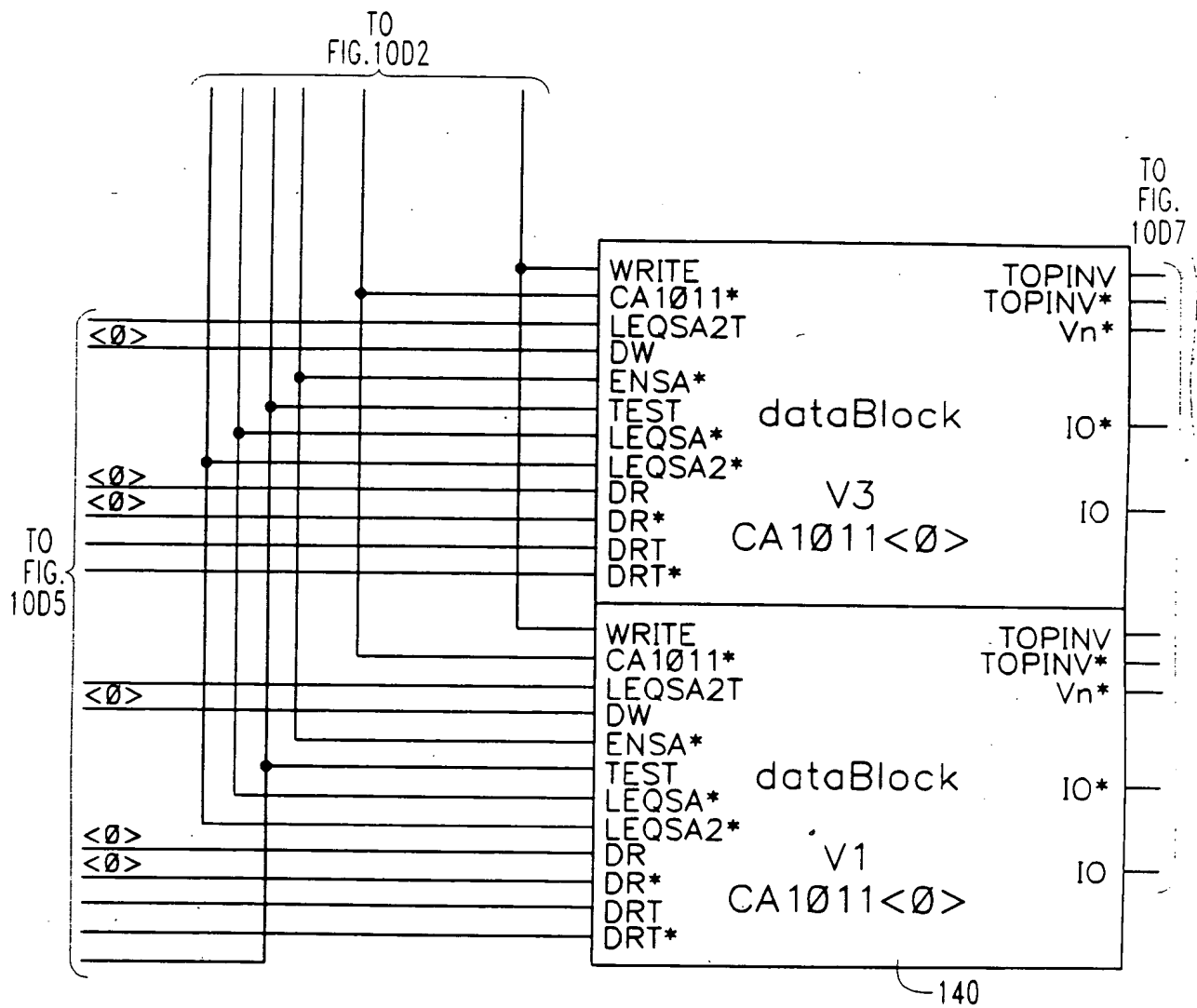


FIG. 10D6

FIG. 10D7

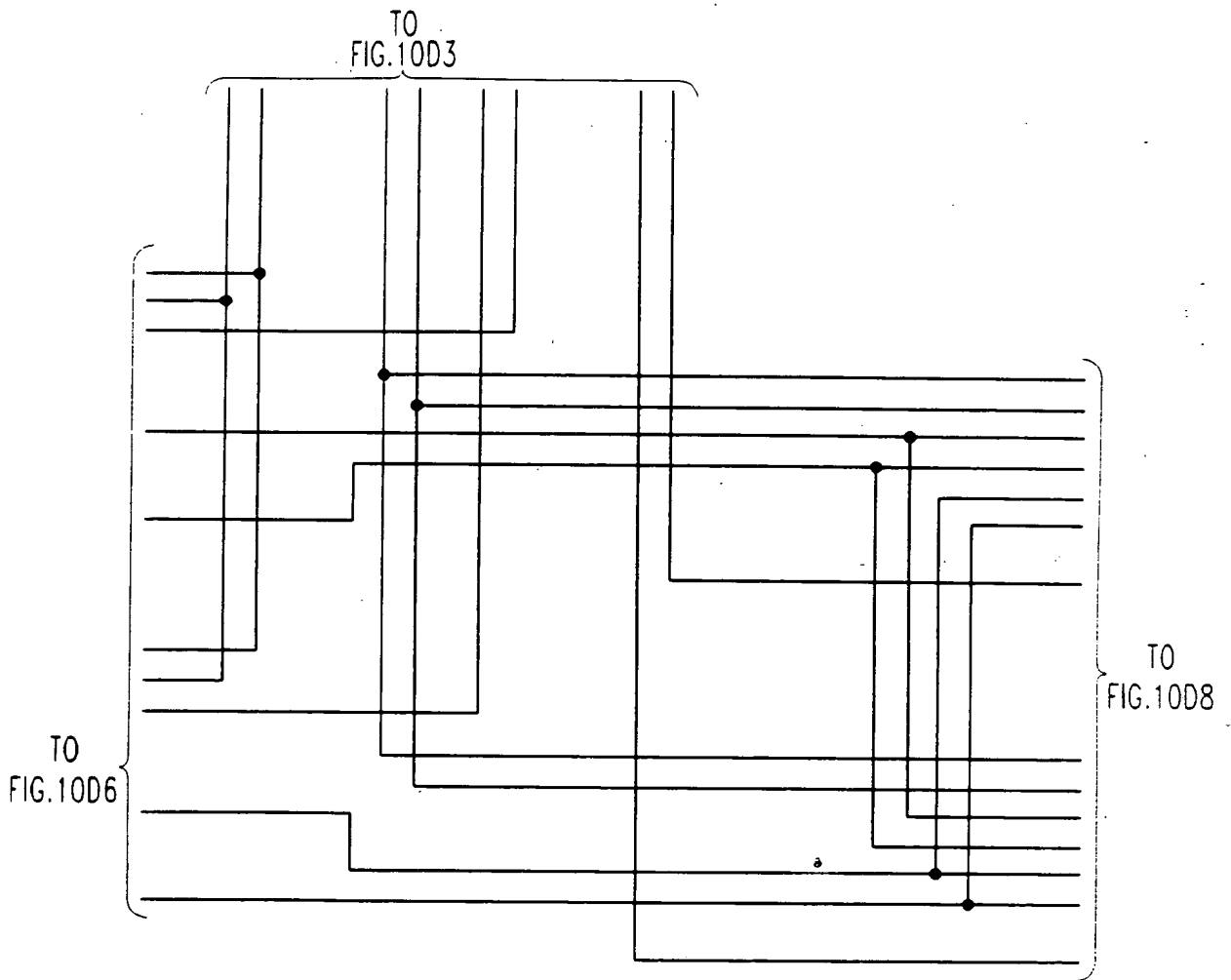
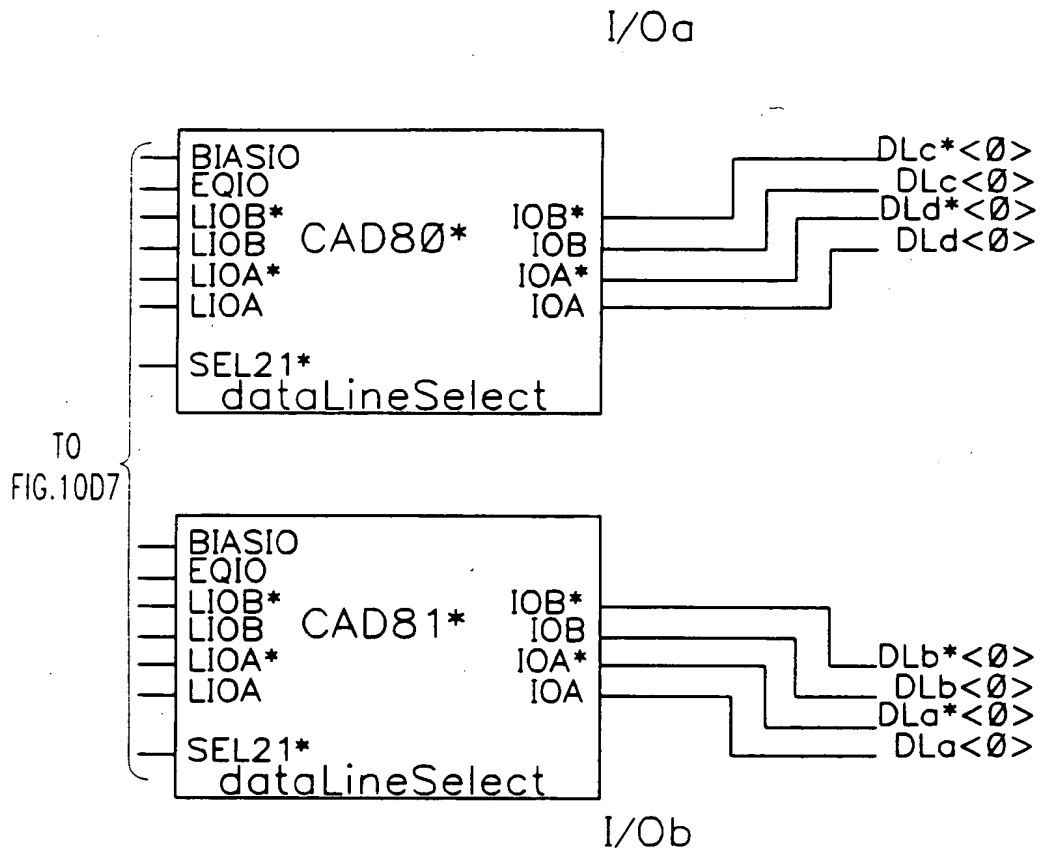
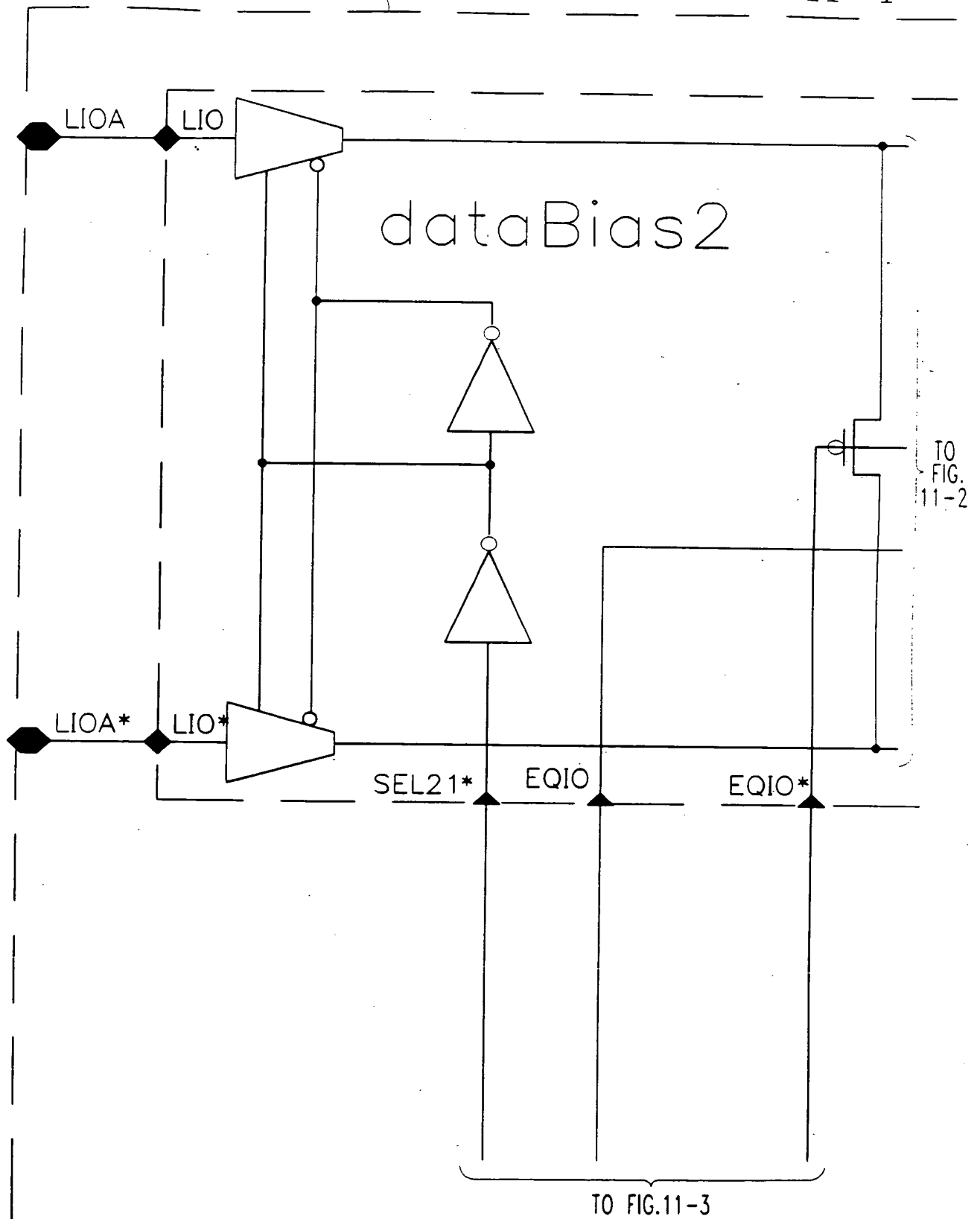


FIG. 10D7

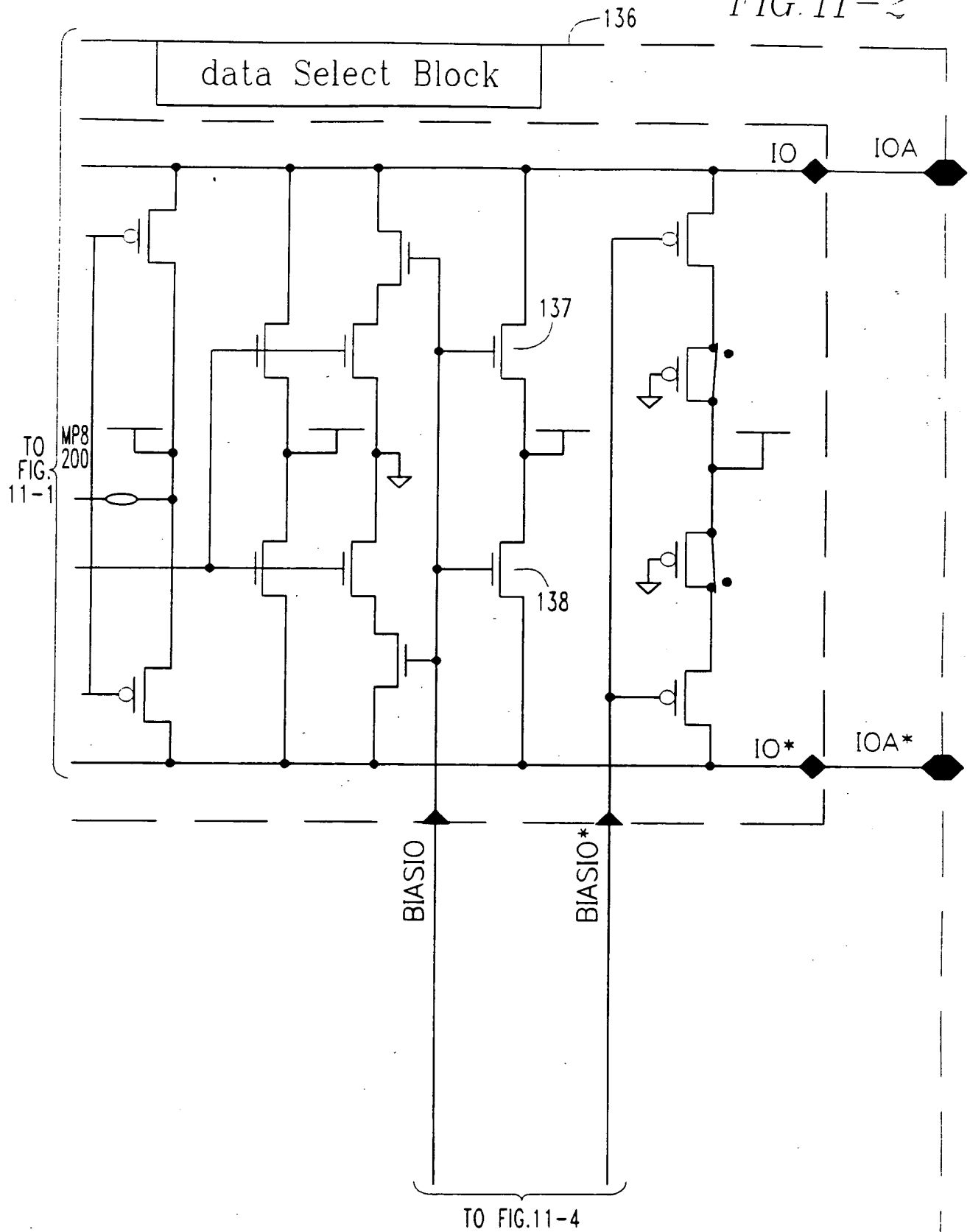


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FIG. 11-2



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TO FIG.11-1

FIG. 11-3

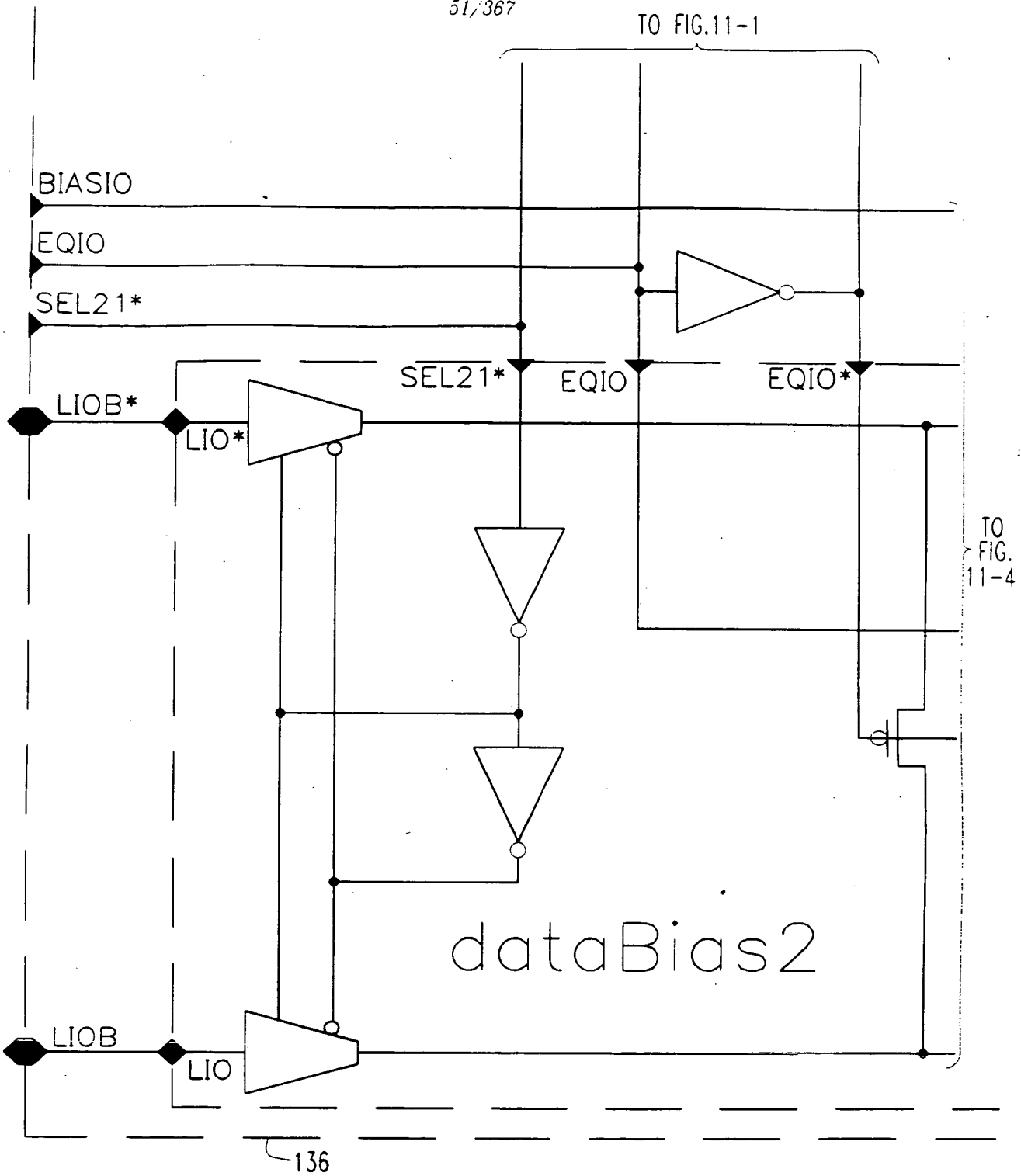


FIG. 11-3

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TO FIG.11-2

TO
FIG.
11-3

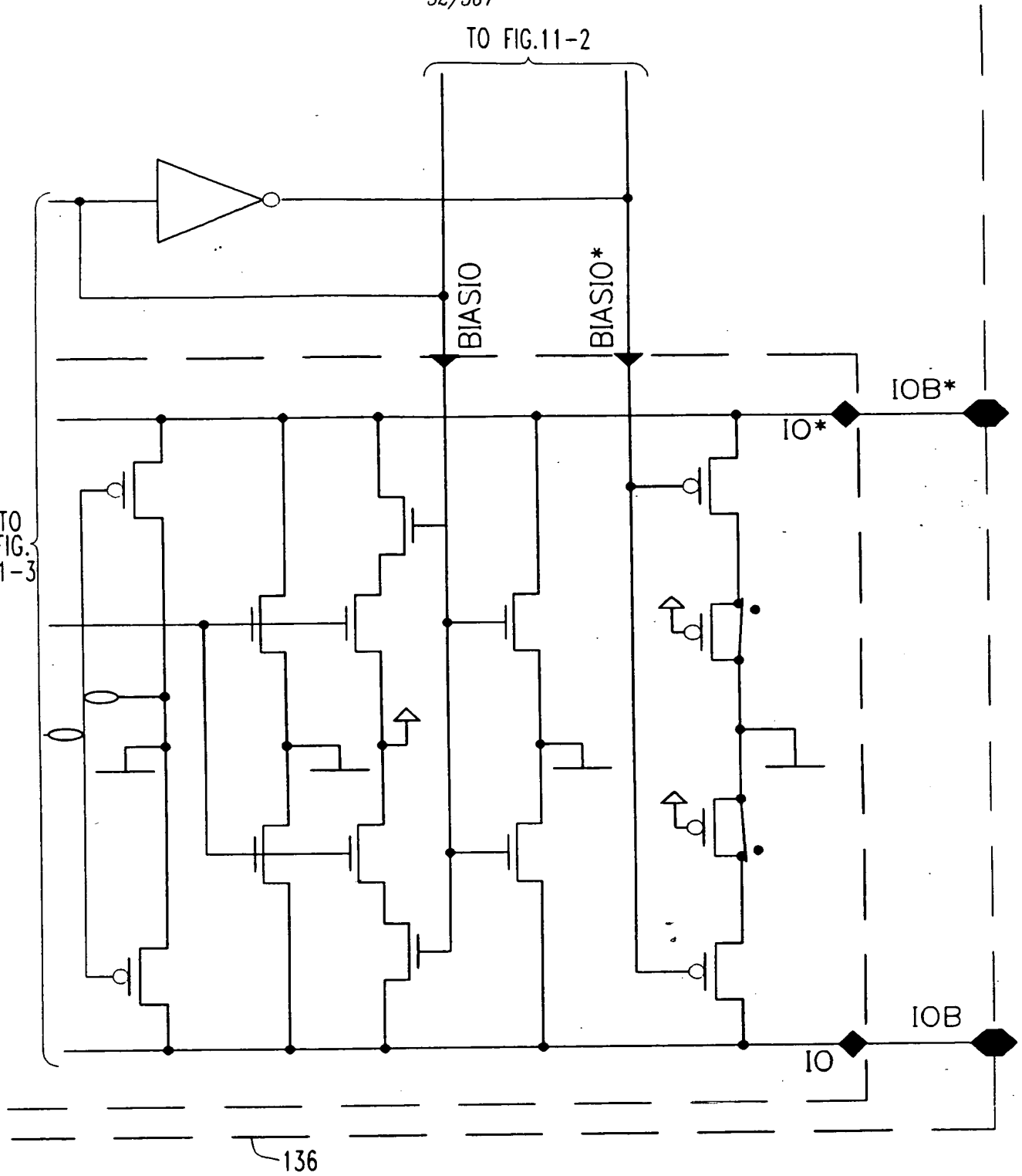


FIG.11-4

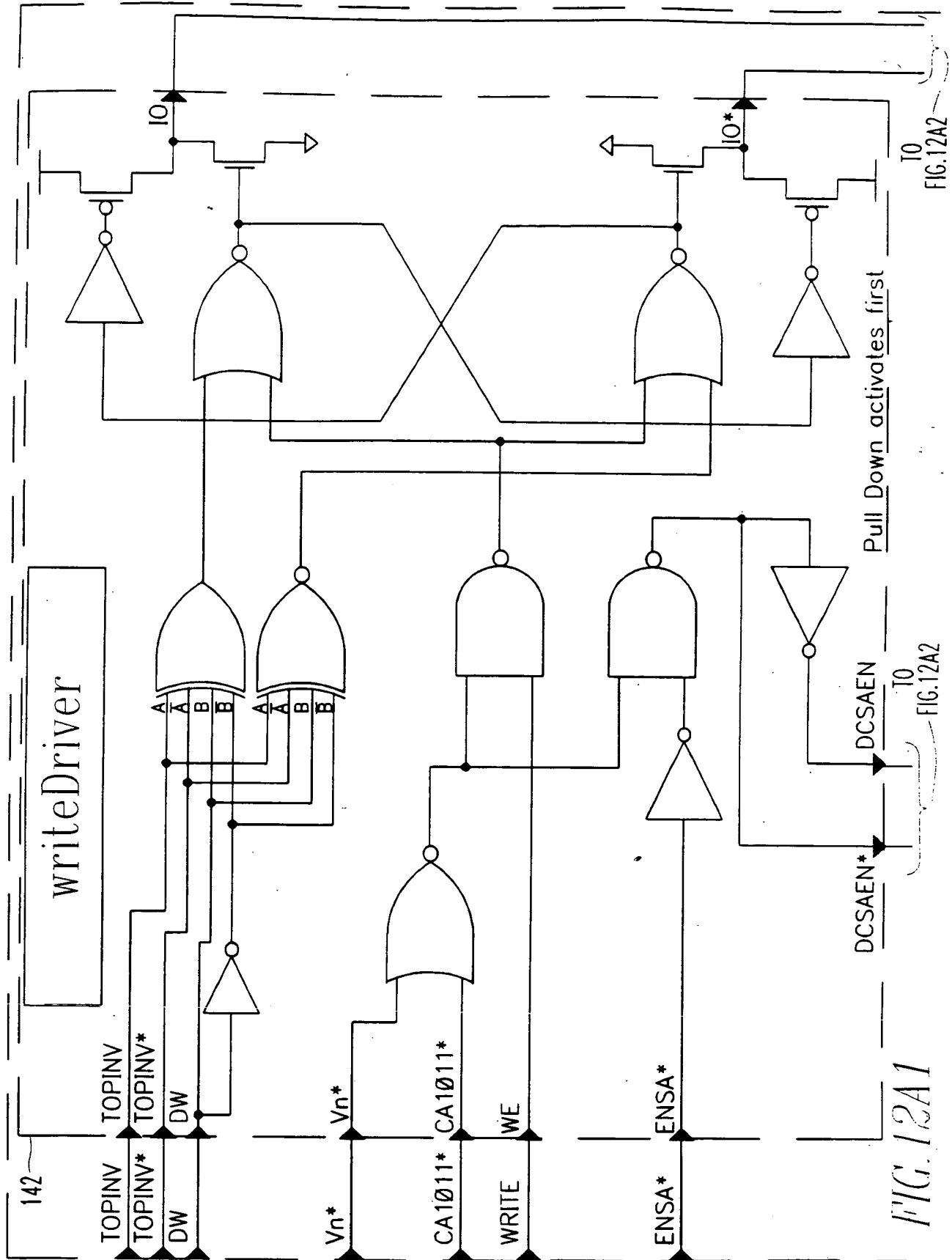


FIG. 12A1

FIG. 12A2

FIG. 12A2

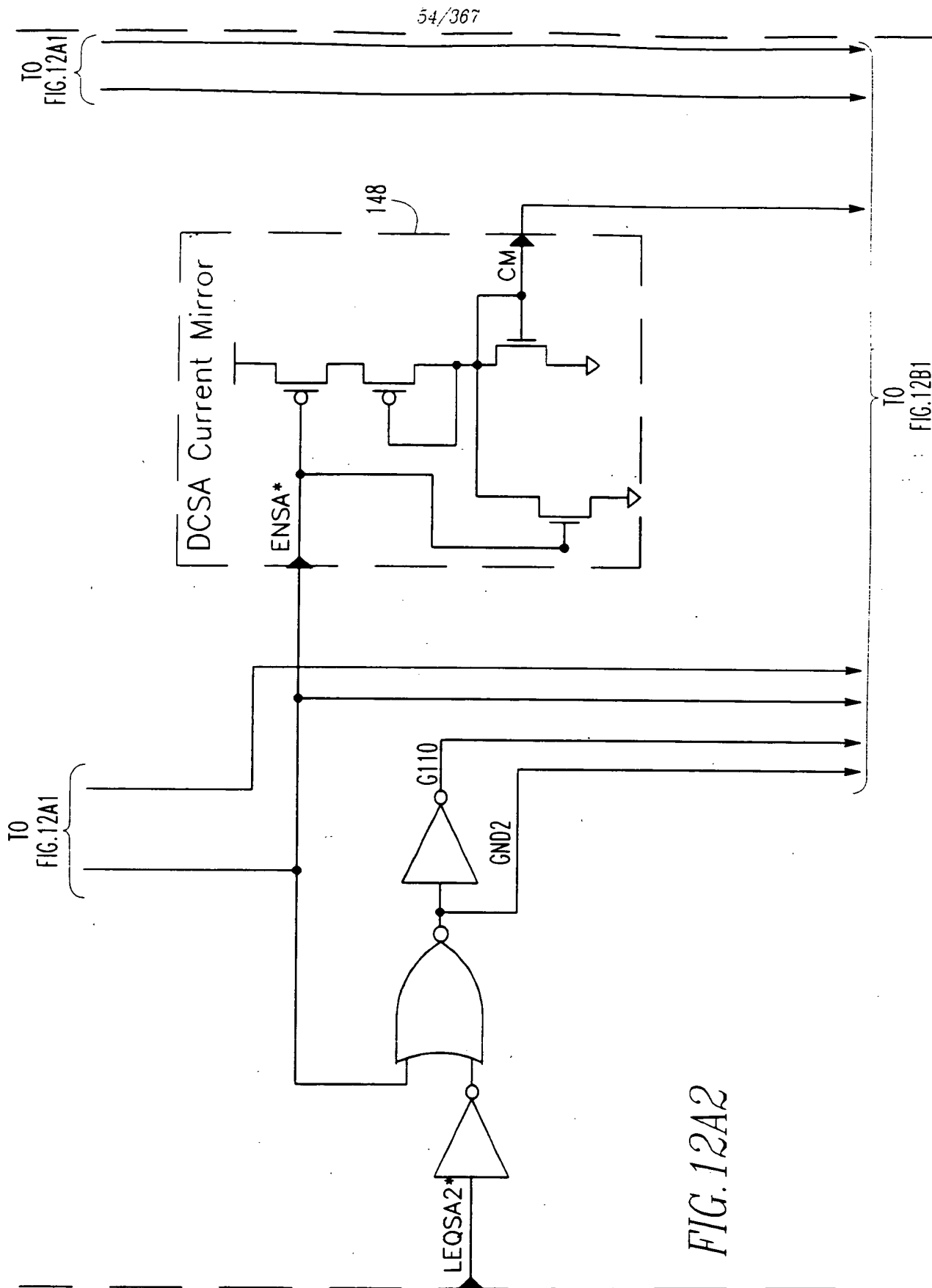
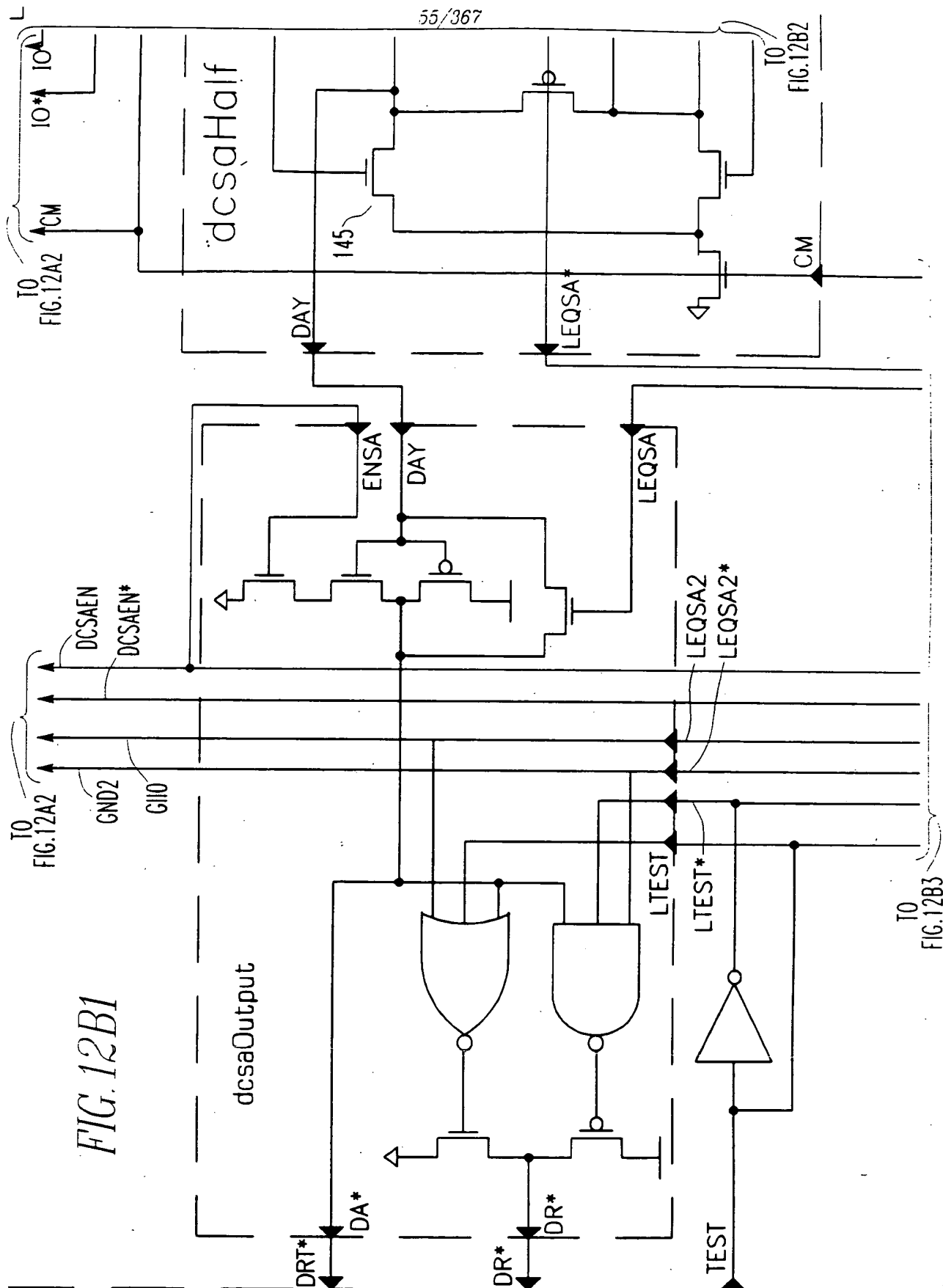


FIG. 12A2



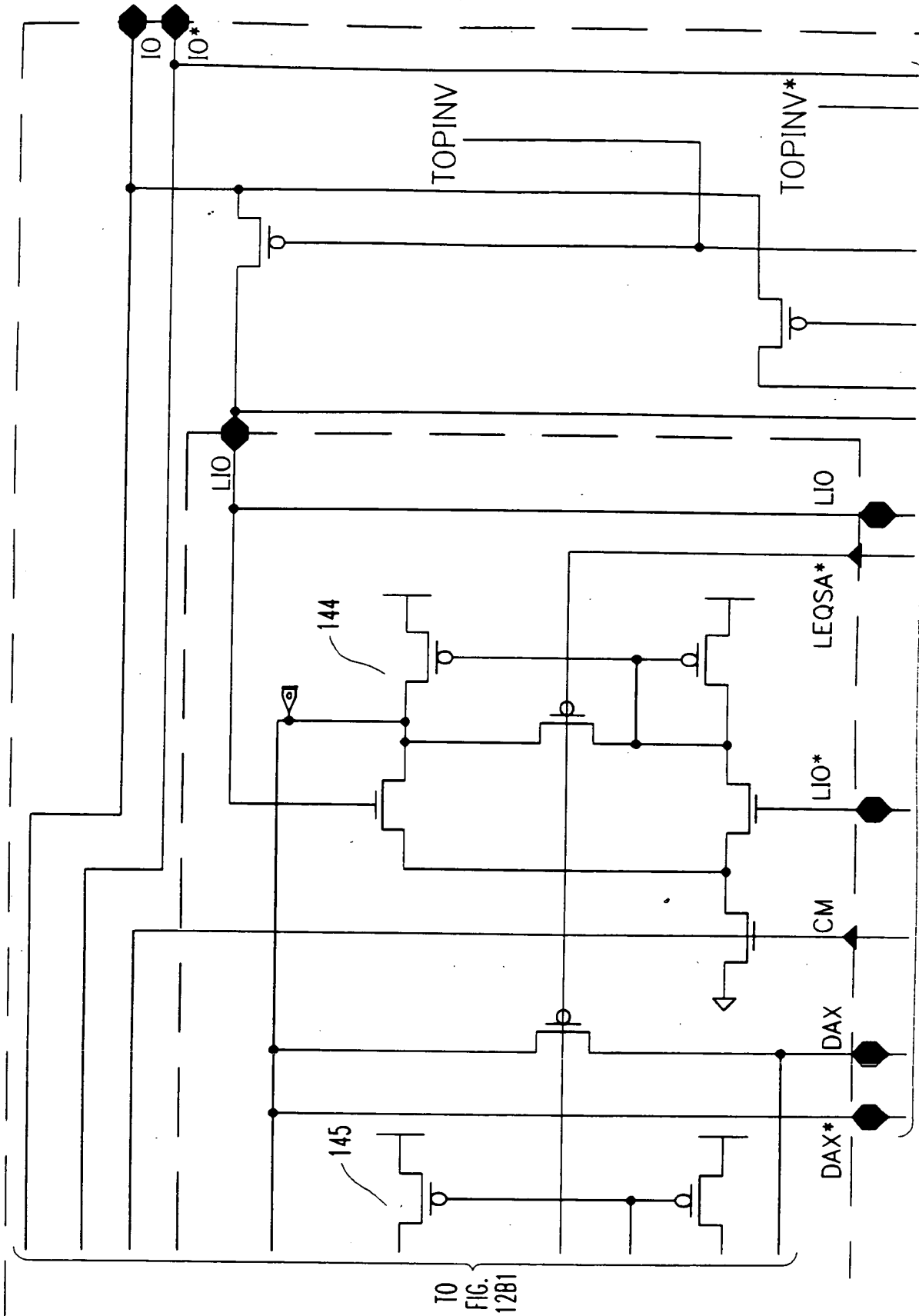
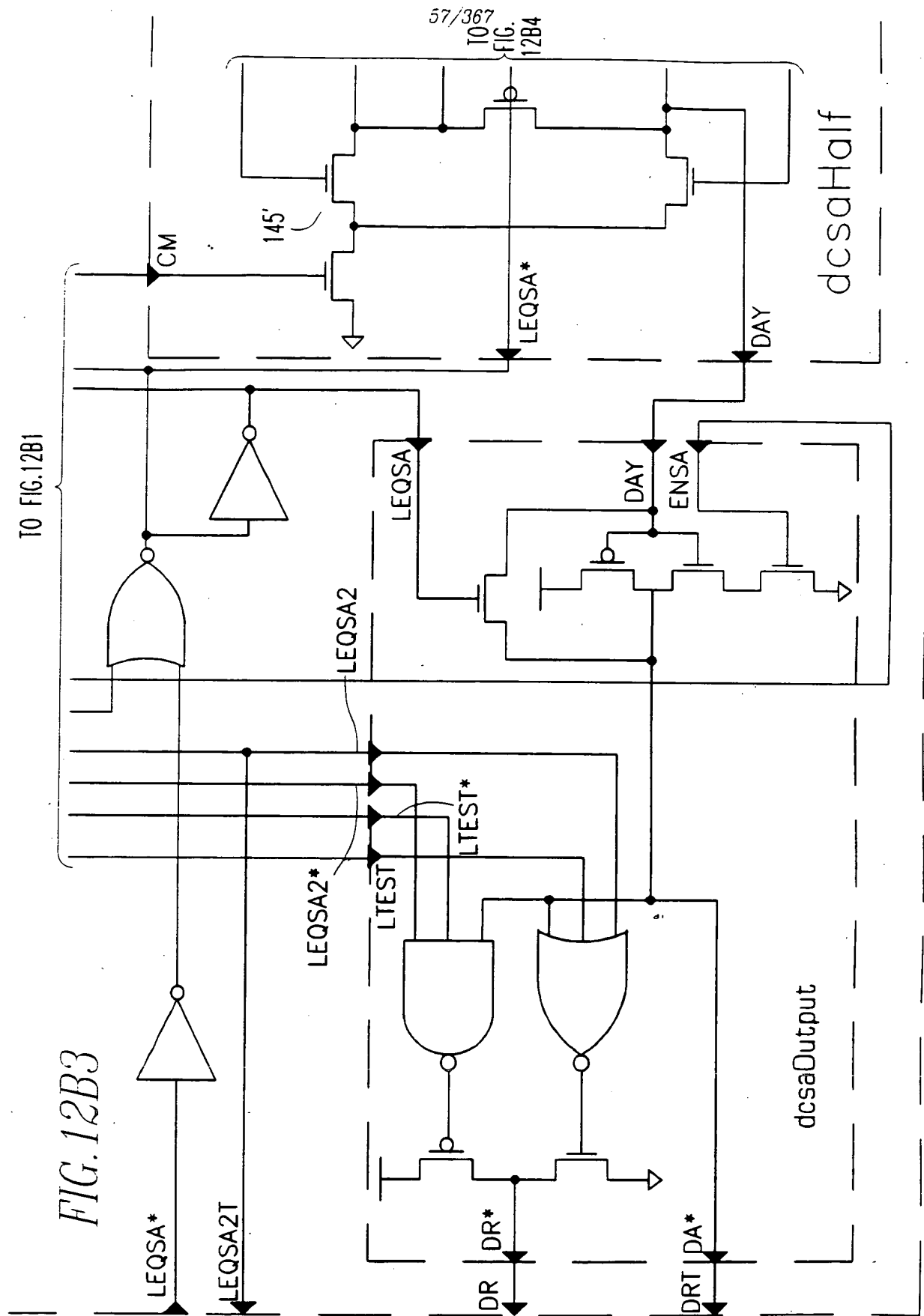
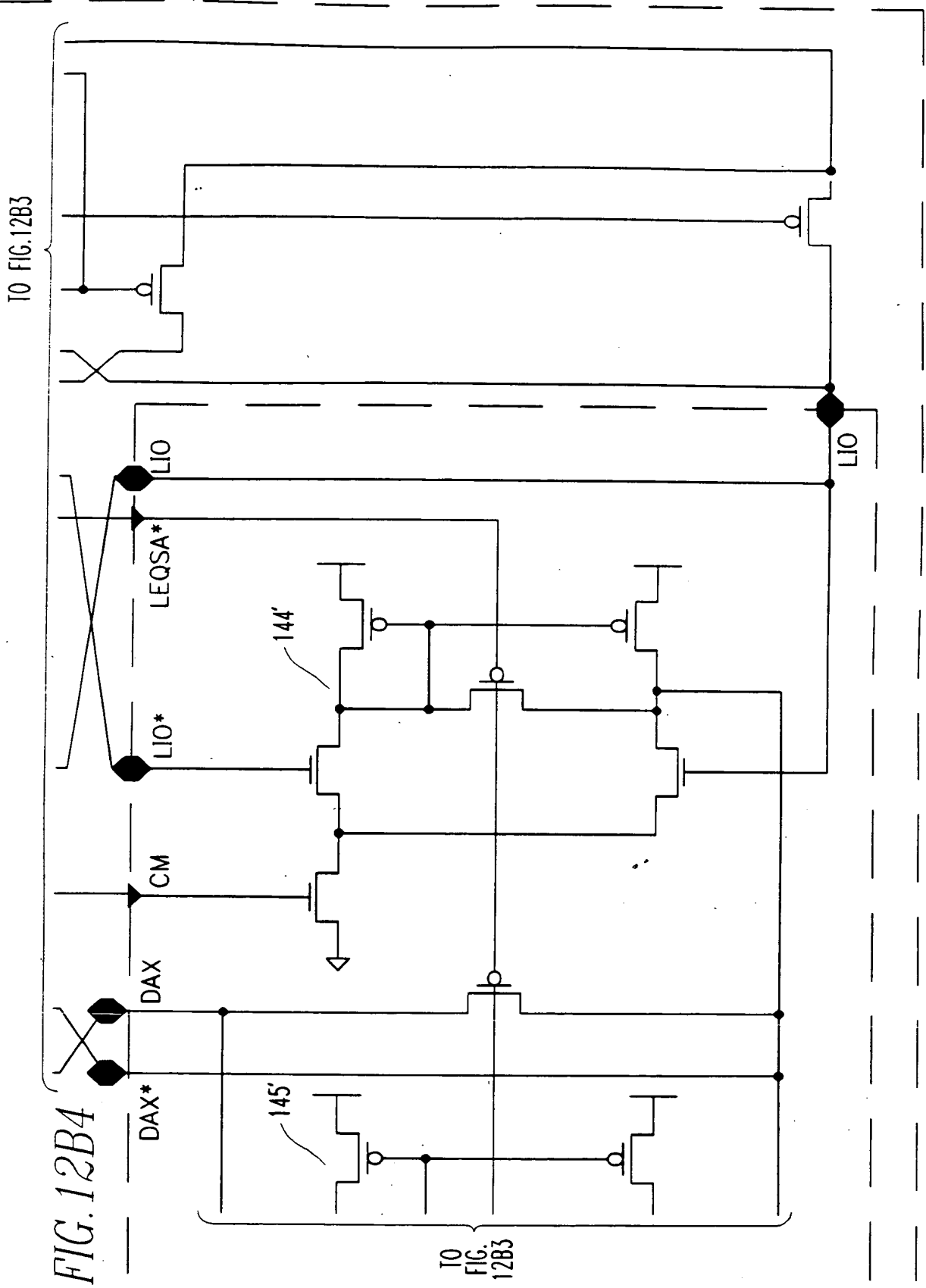
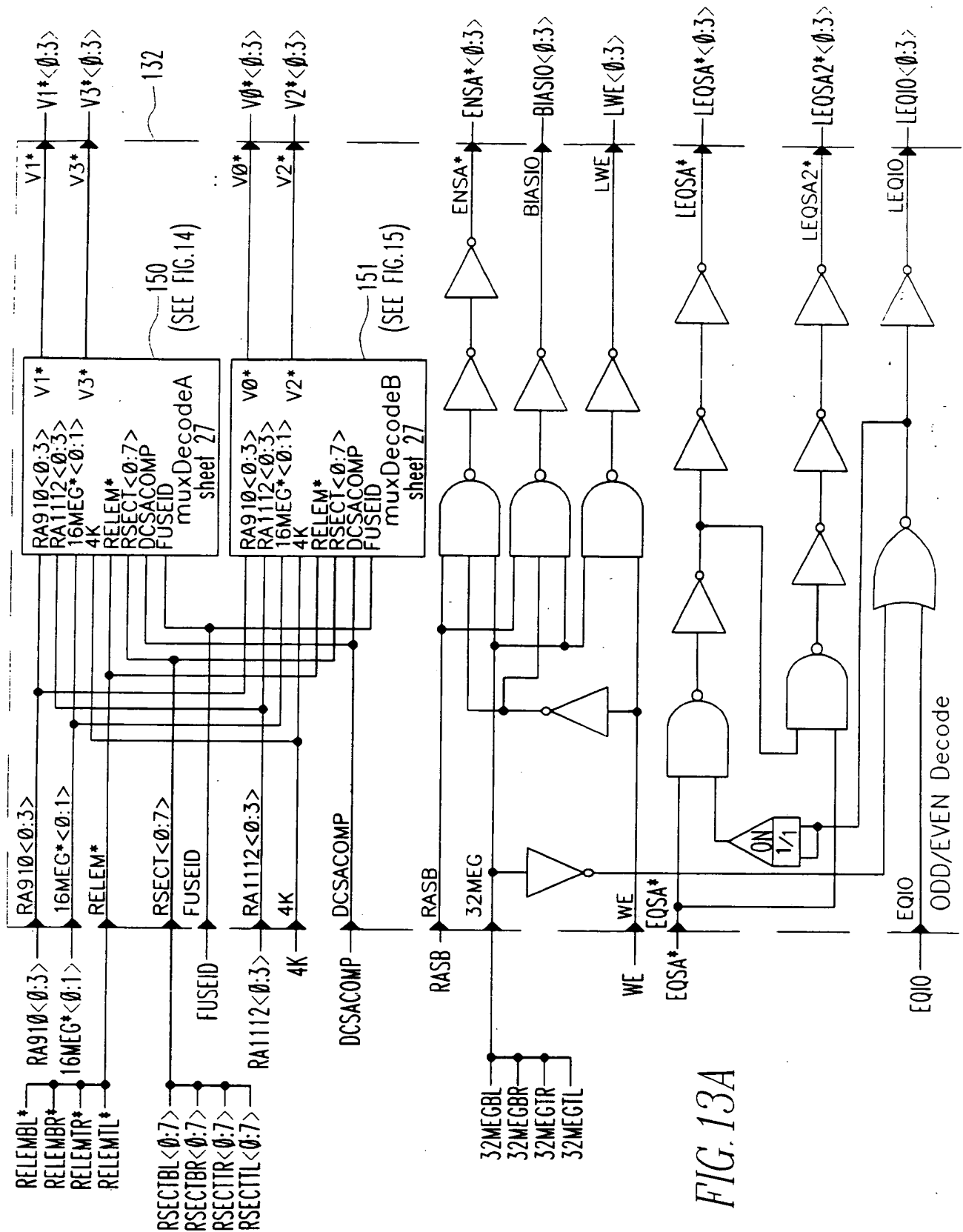


FIG. 12B2

FIG. 12B1







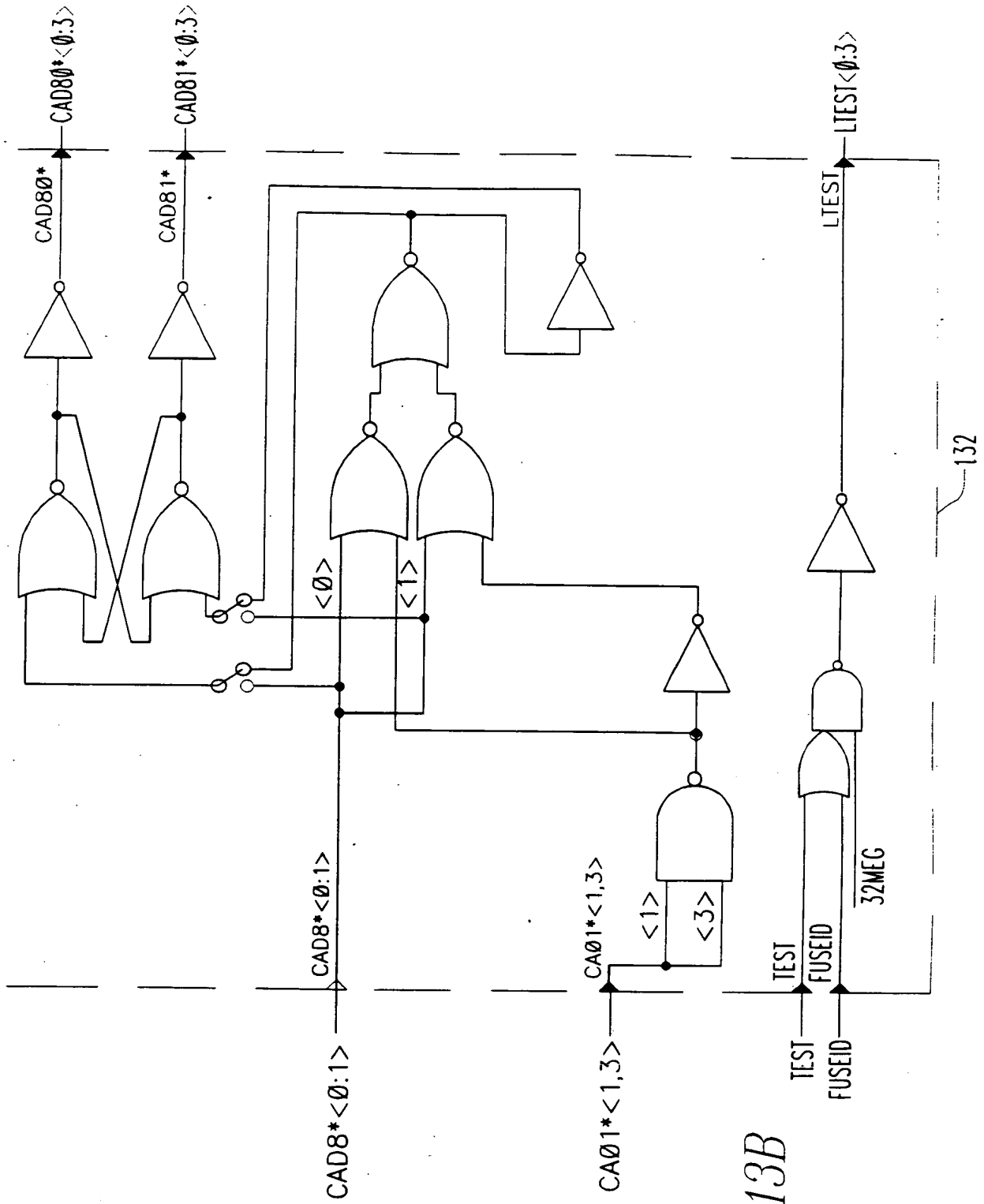


FIG. 13B

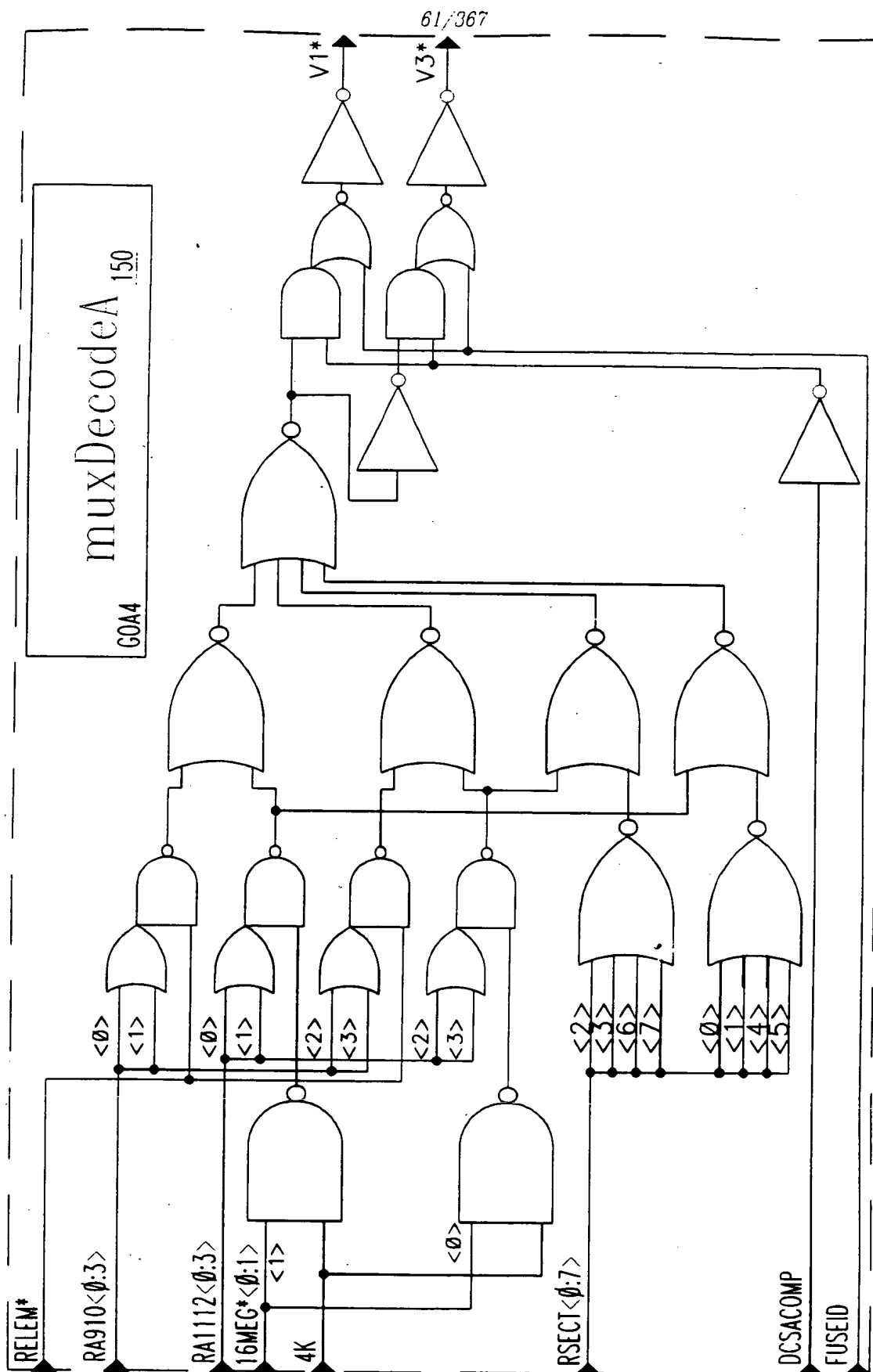


FIG. 14

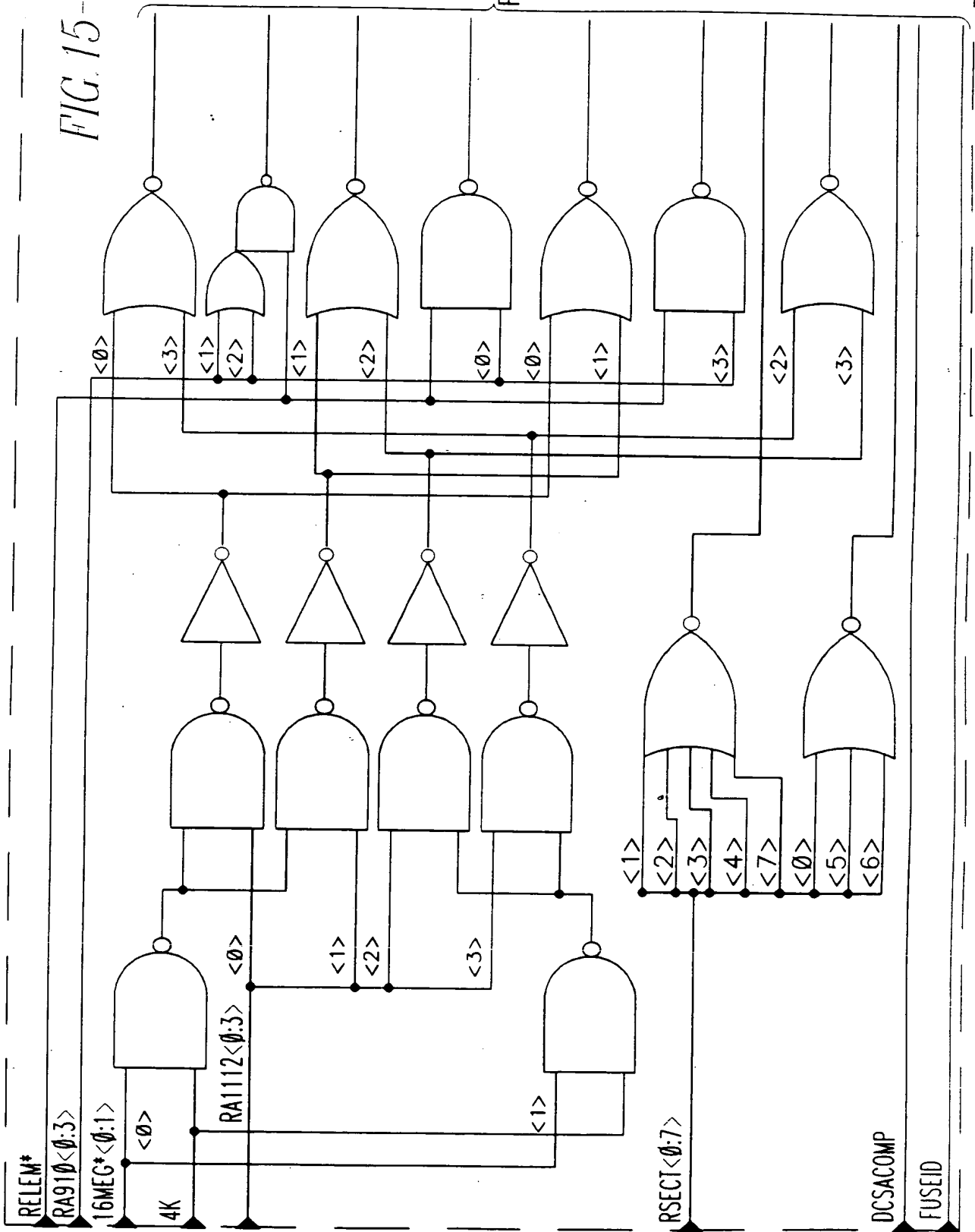
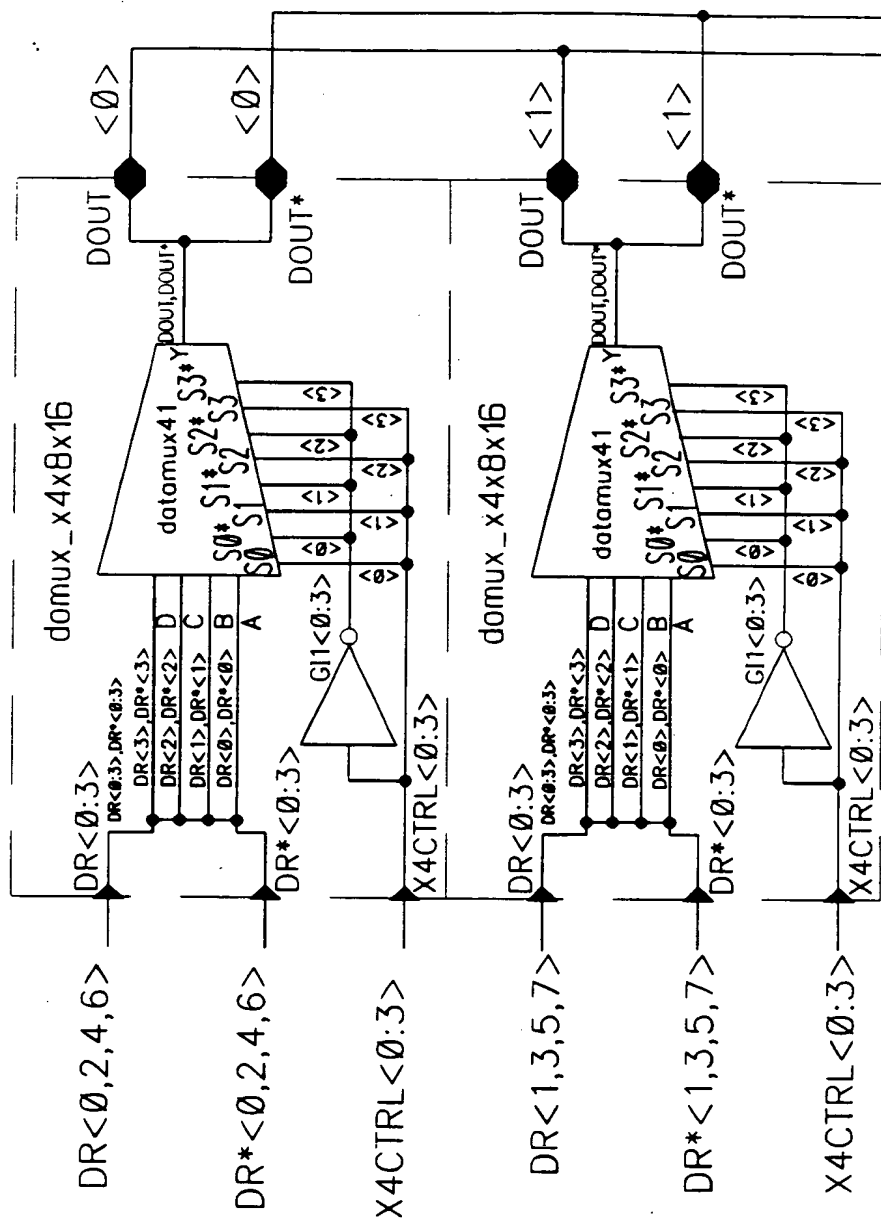


FIG. 16A



TO FIG. 16B

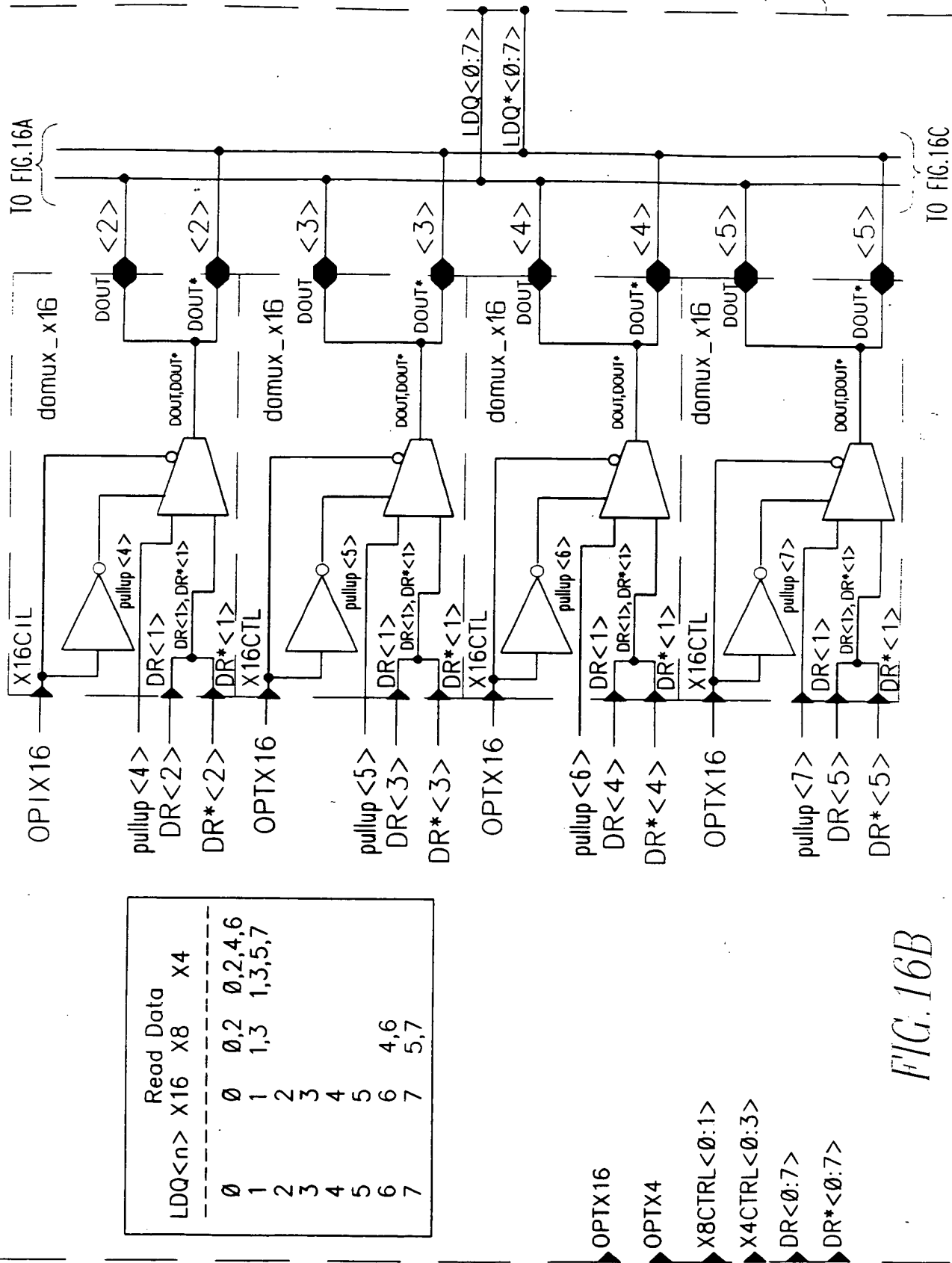
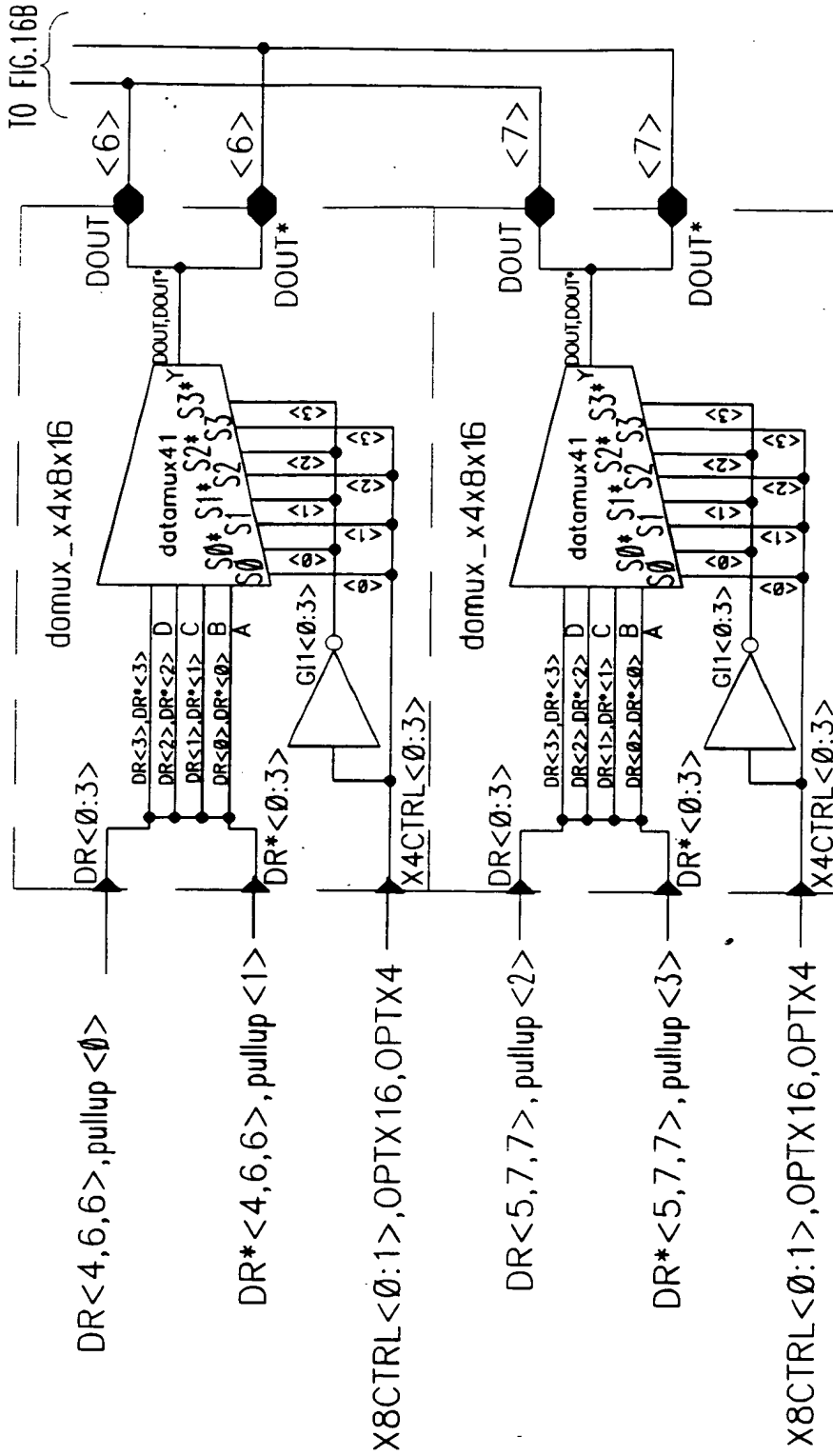


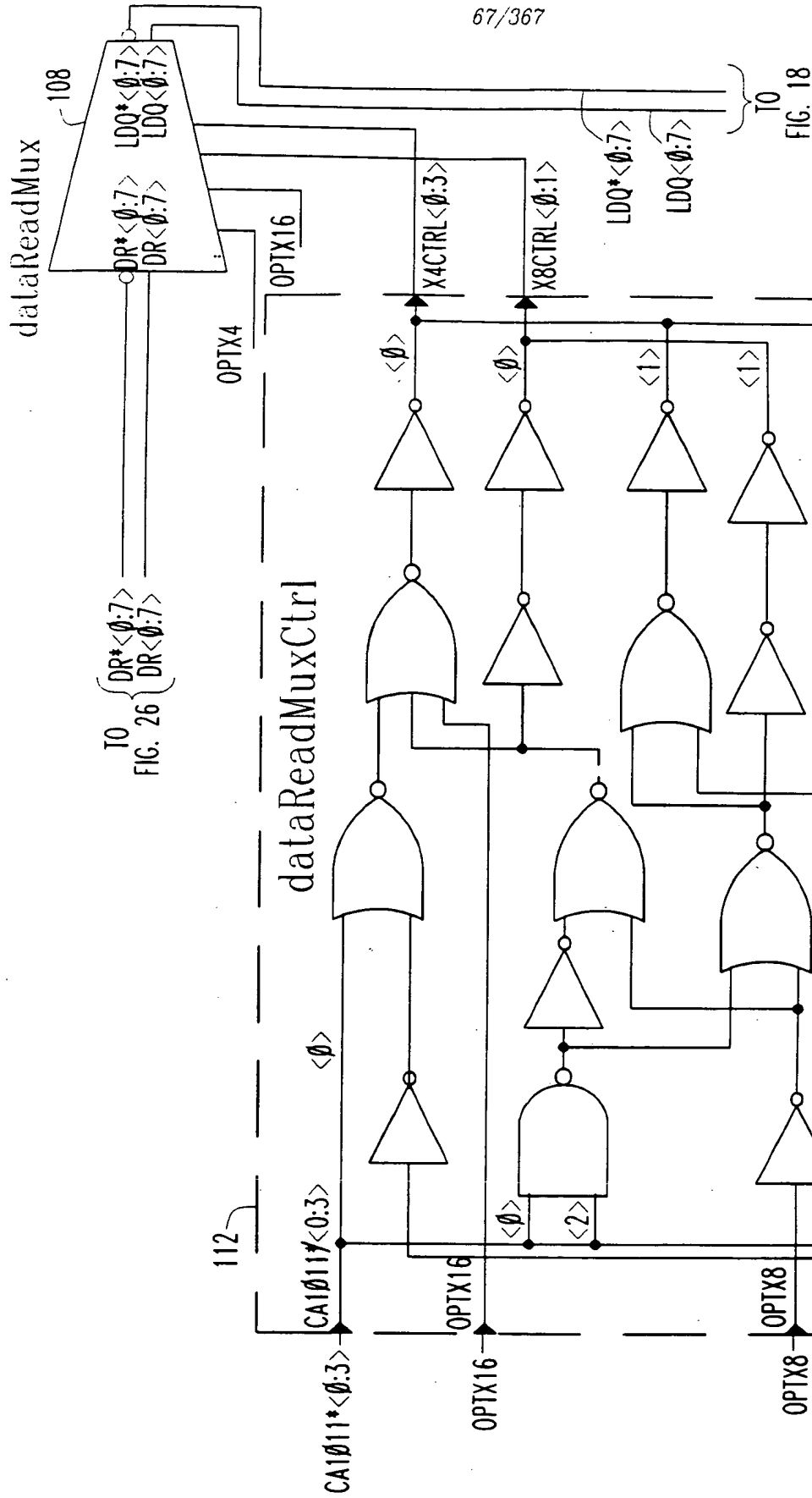
FIG. 16B

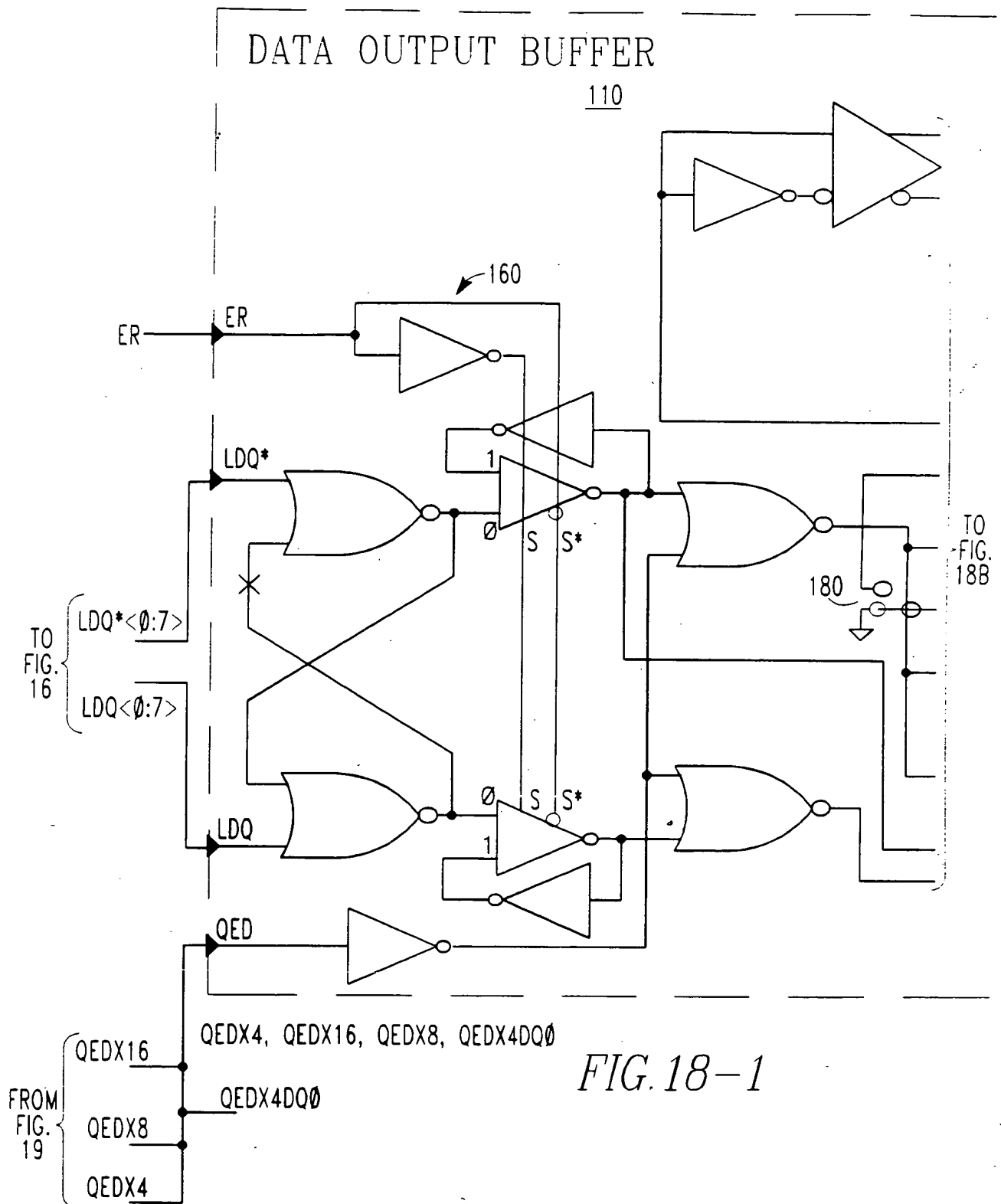


`pullup <0:7>`

dataReadMux

FIG. 16C





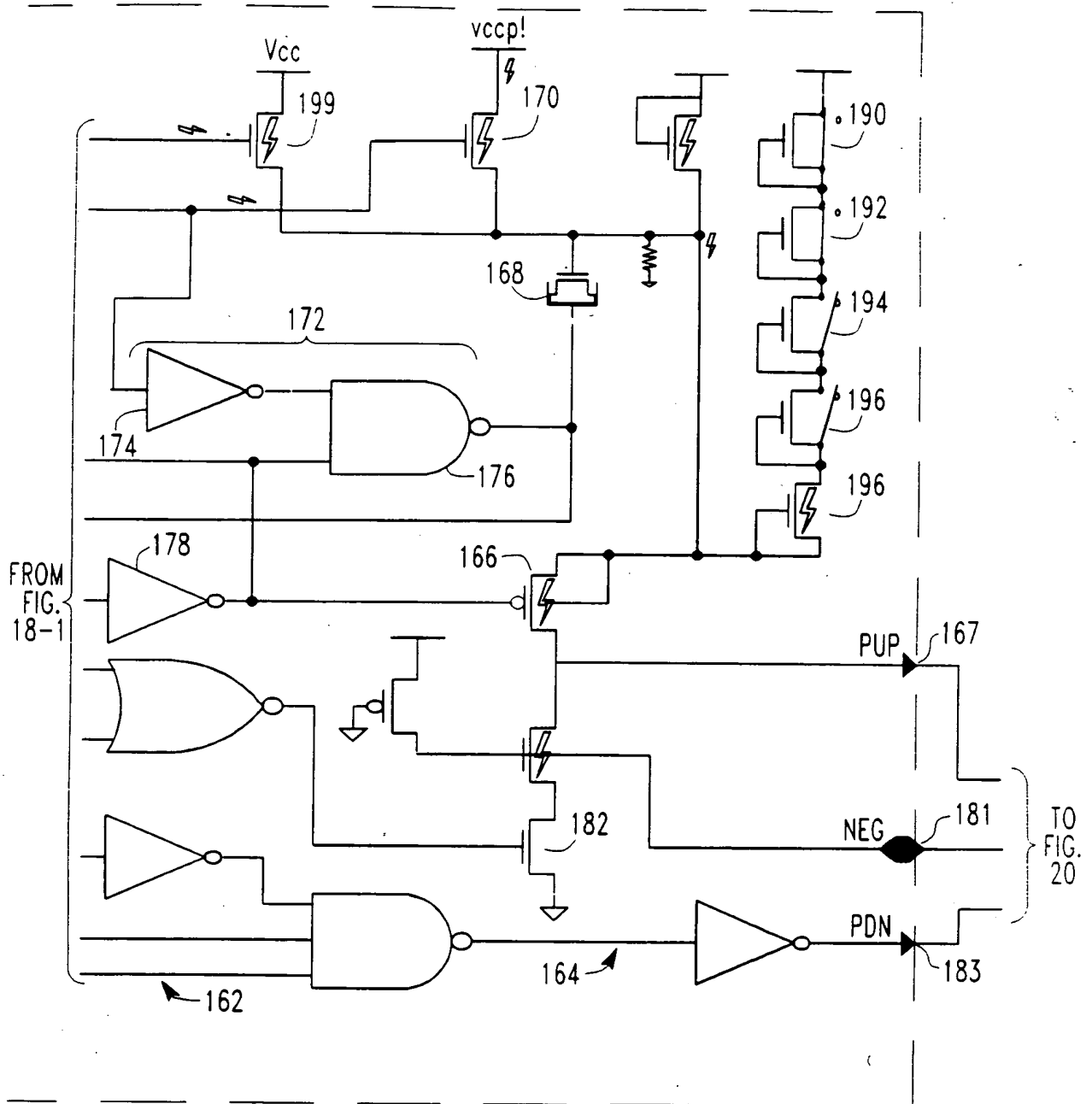


FIG. 18-2

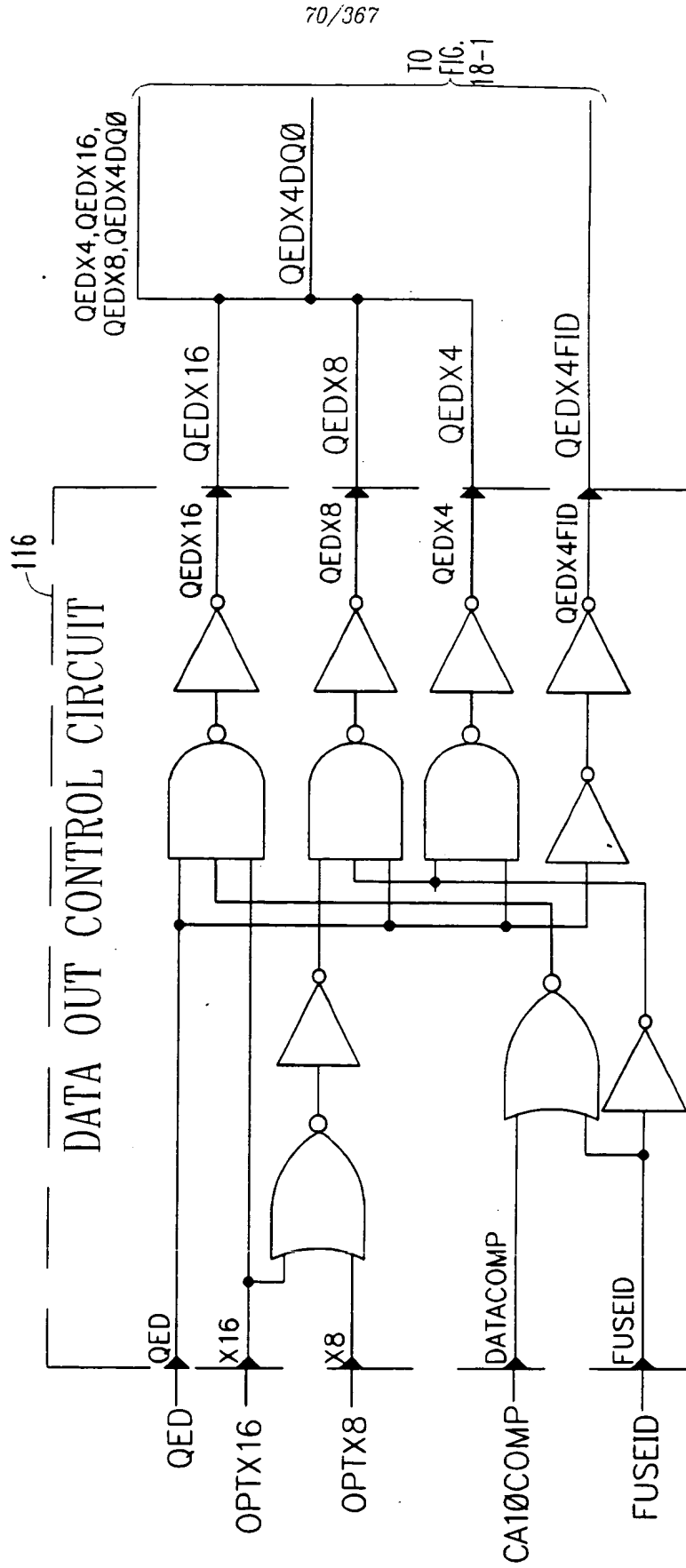
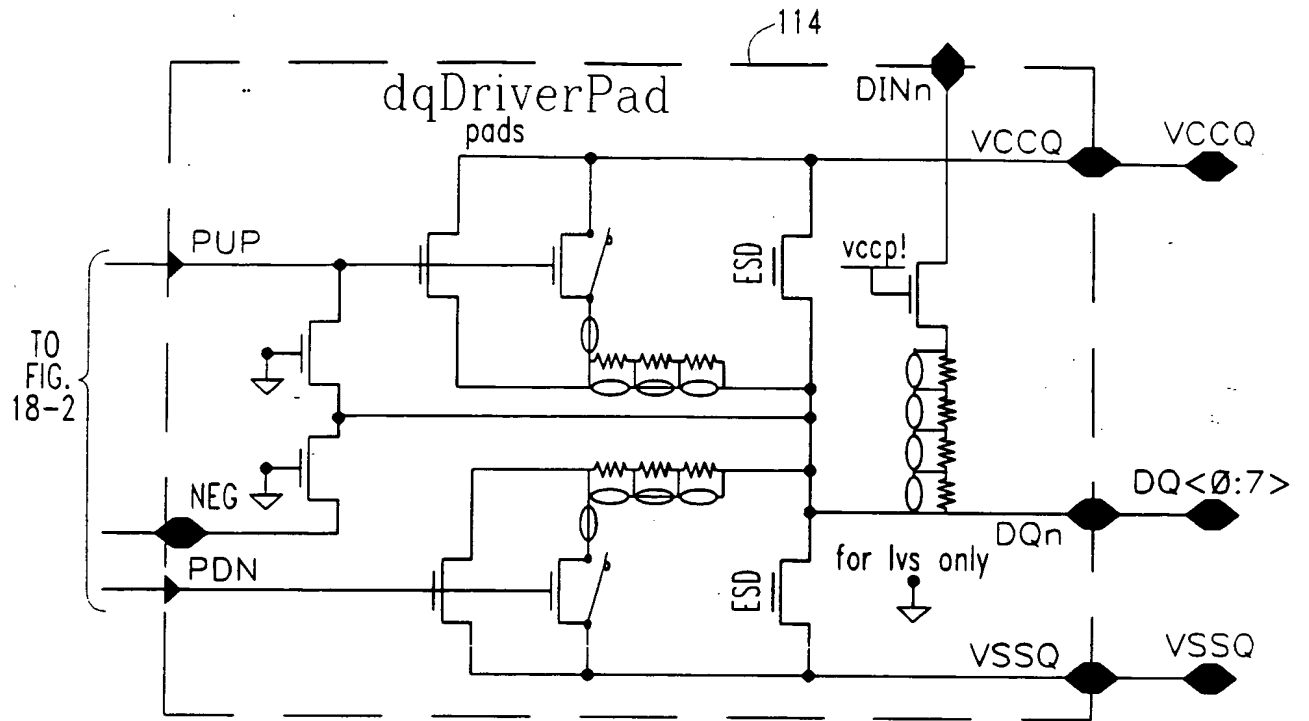


FIG. 19



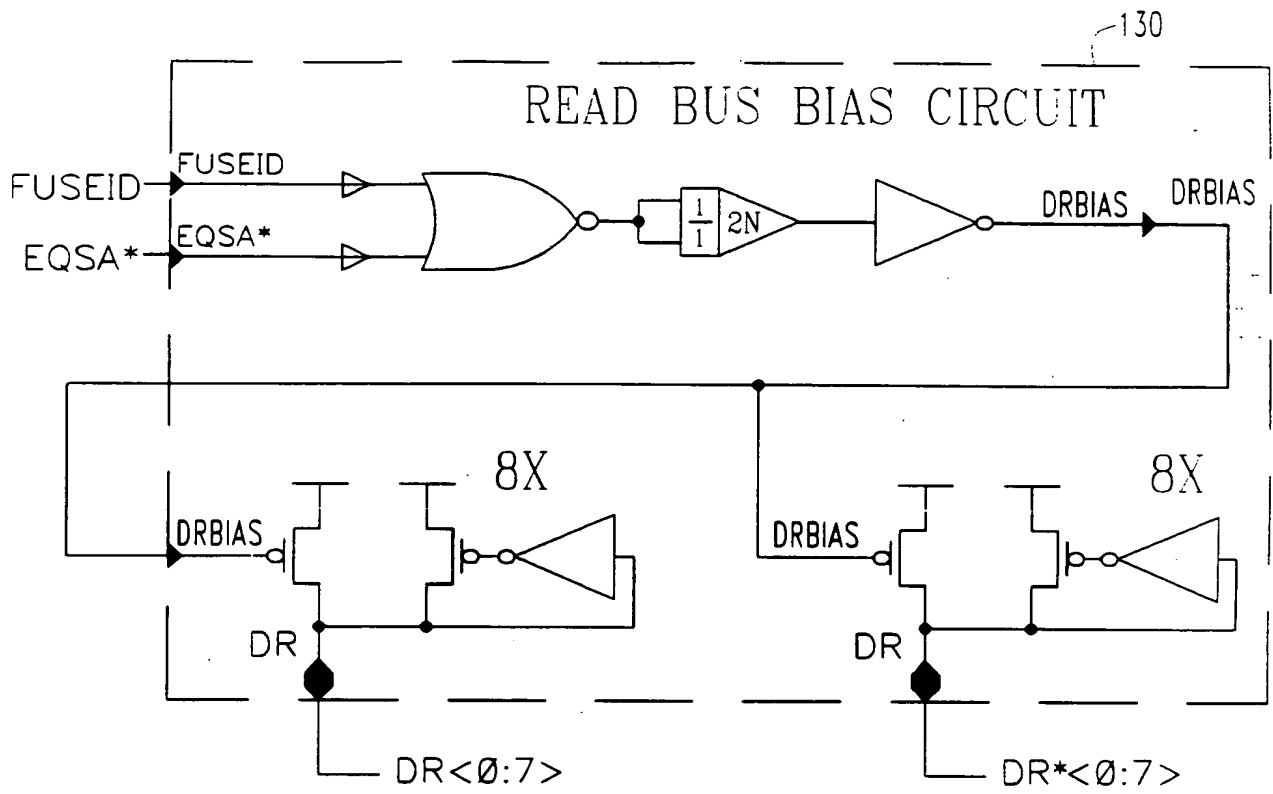


FIG. 21

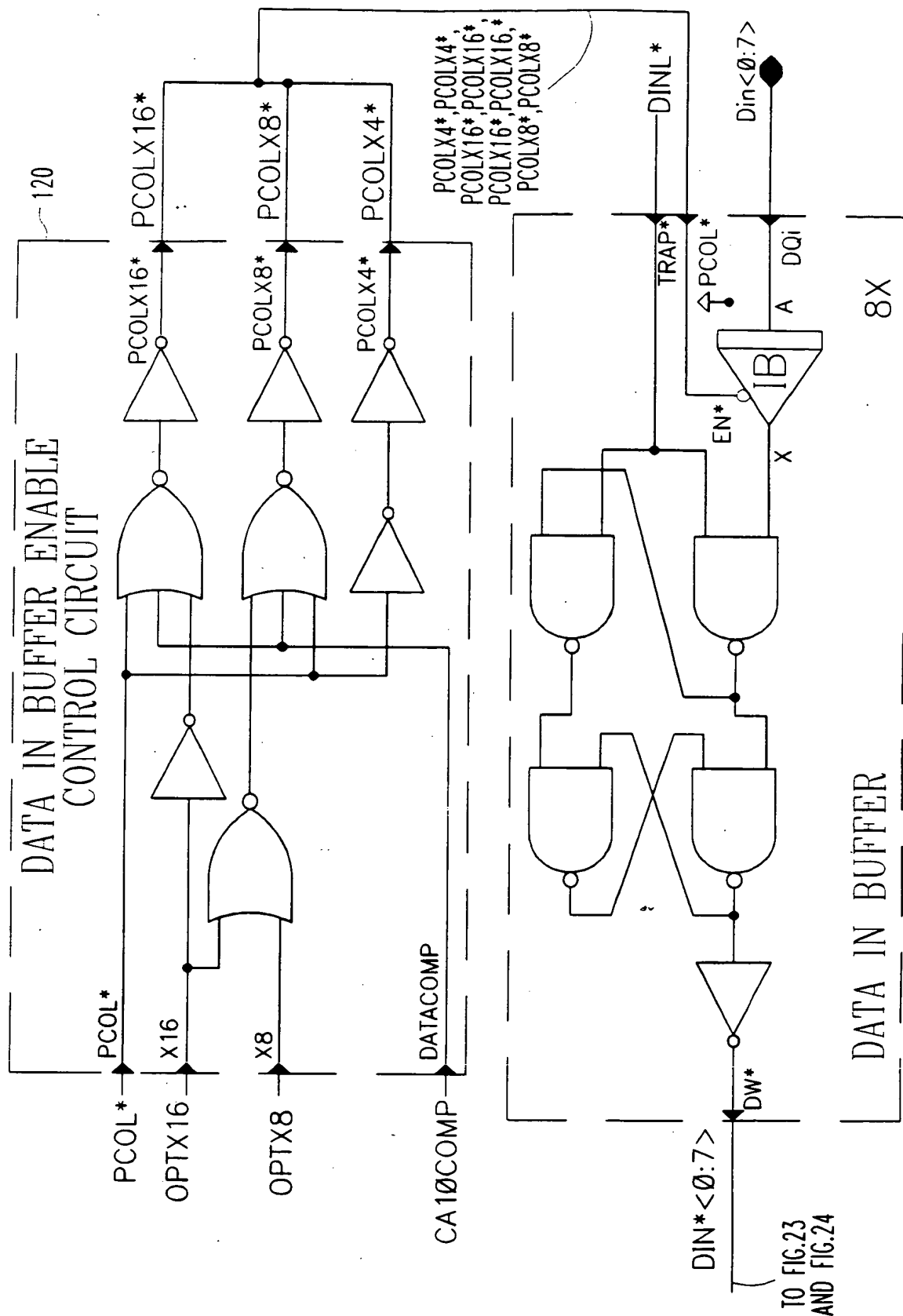
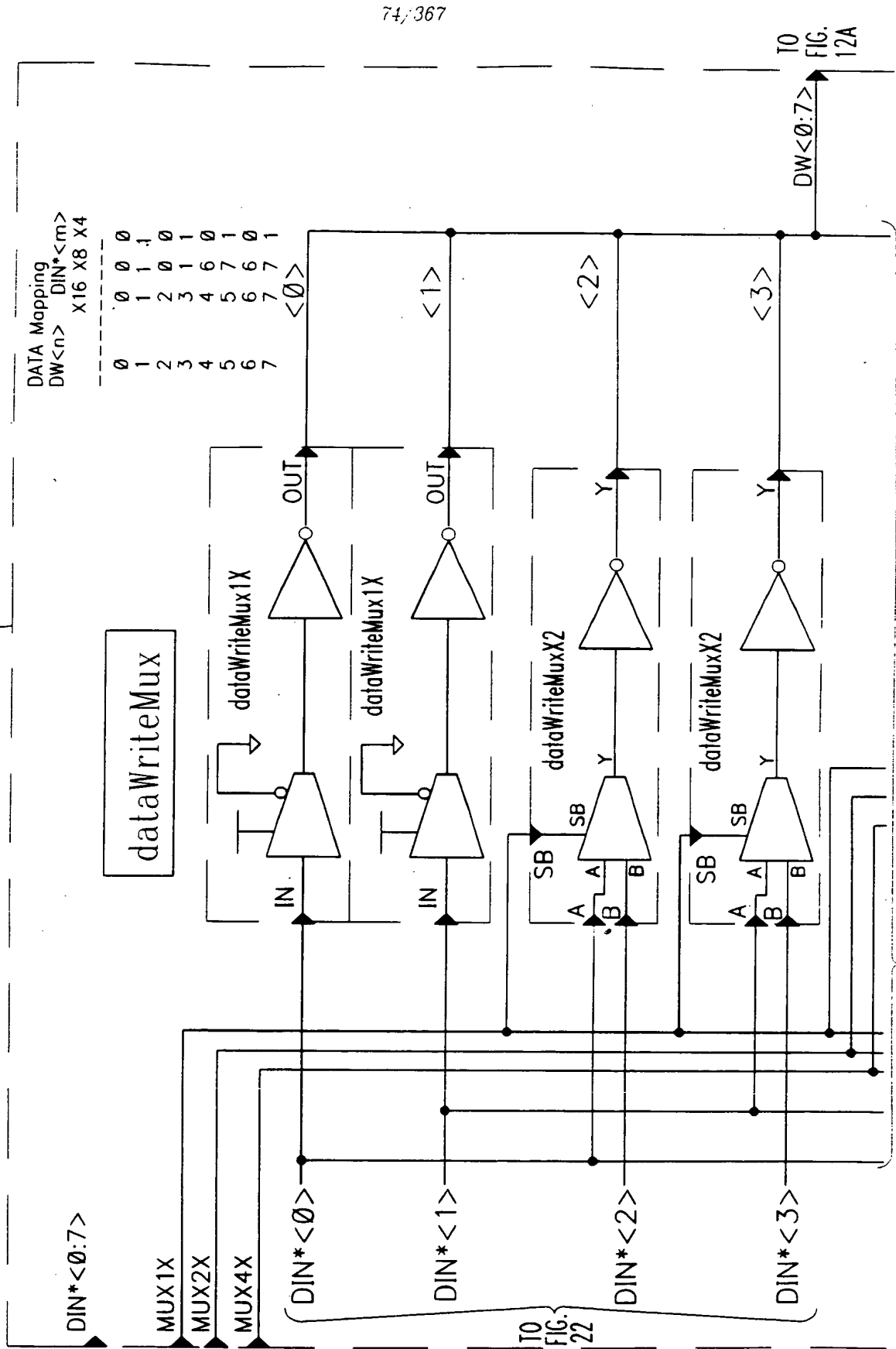


FIG. 22

TO FIG. 23
AND FIG. 24

FIG. 23-1



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FIG. 23-2

FIG. 12A

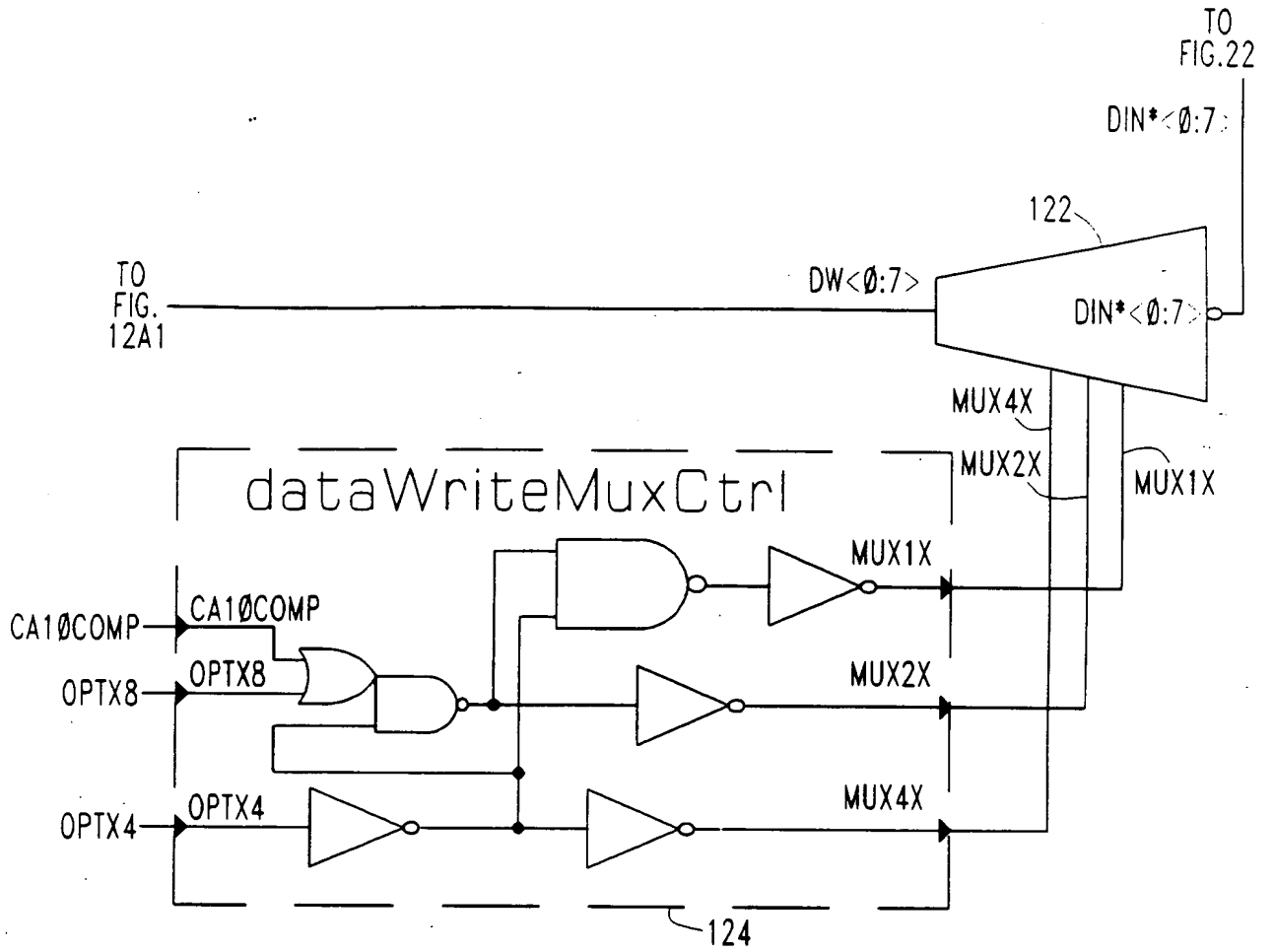


FIG. 24

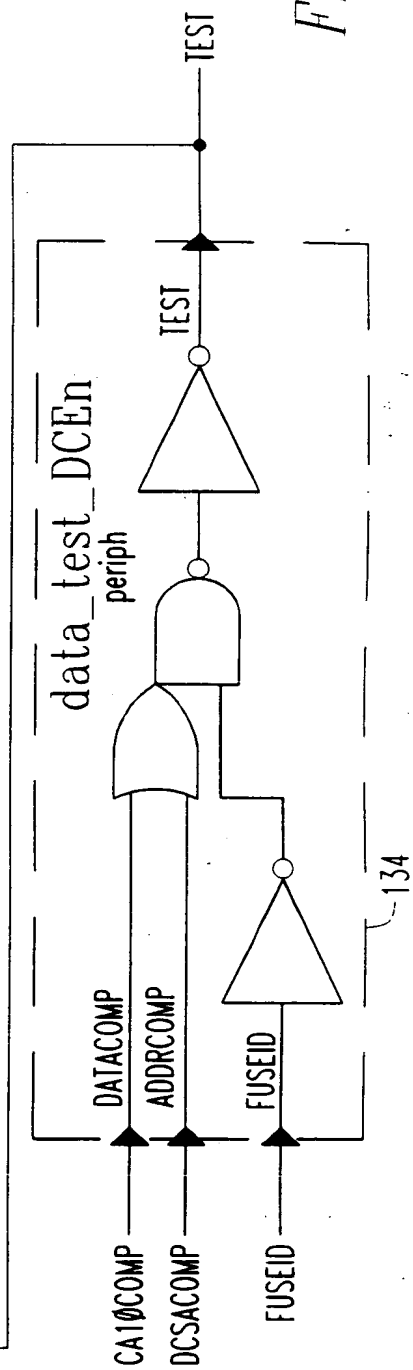
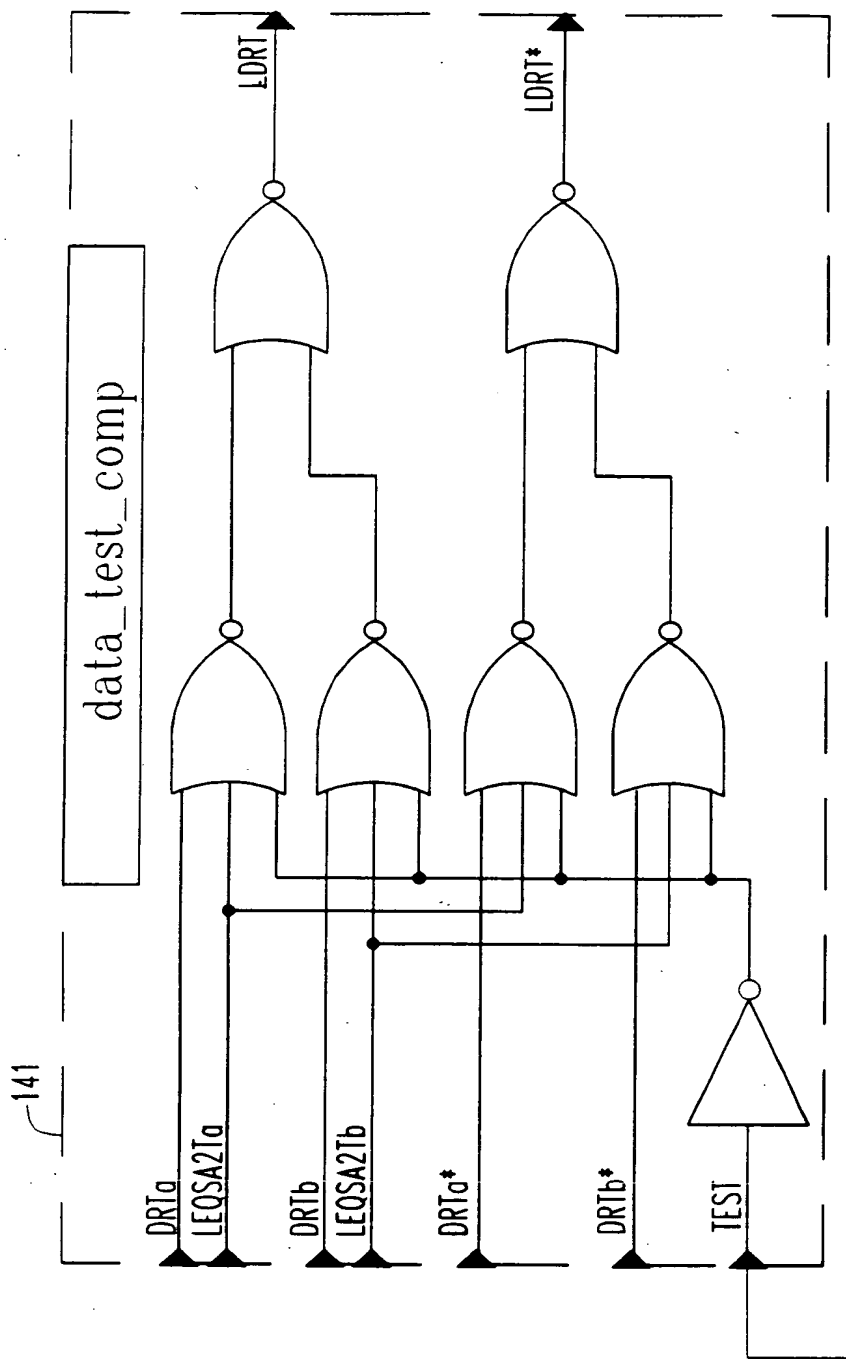


FIG. 25

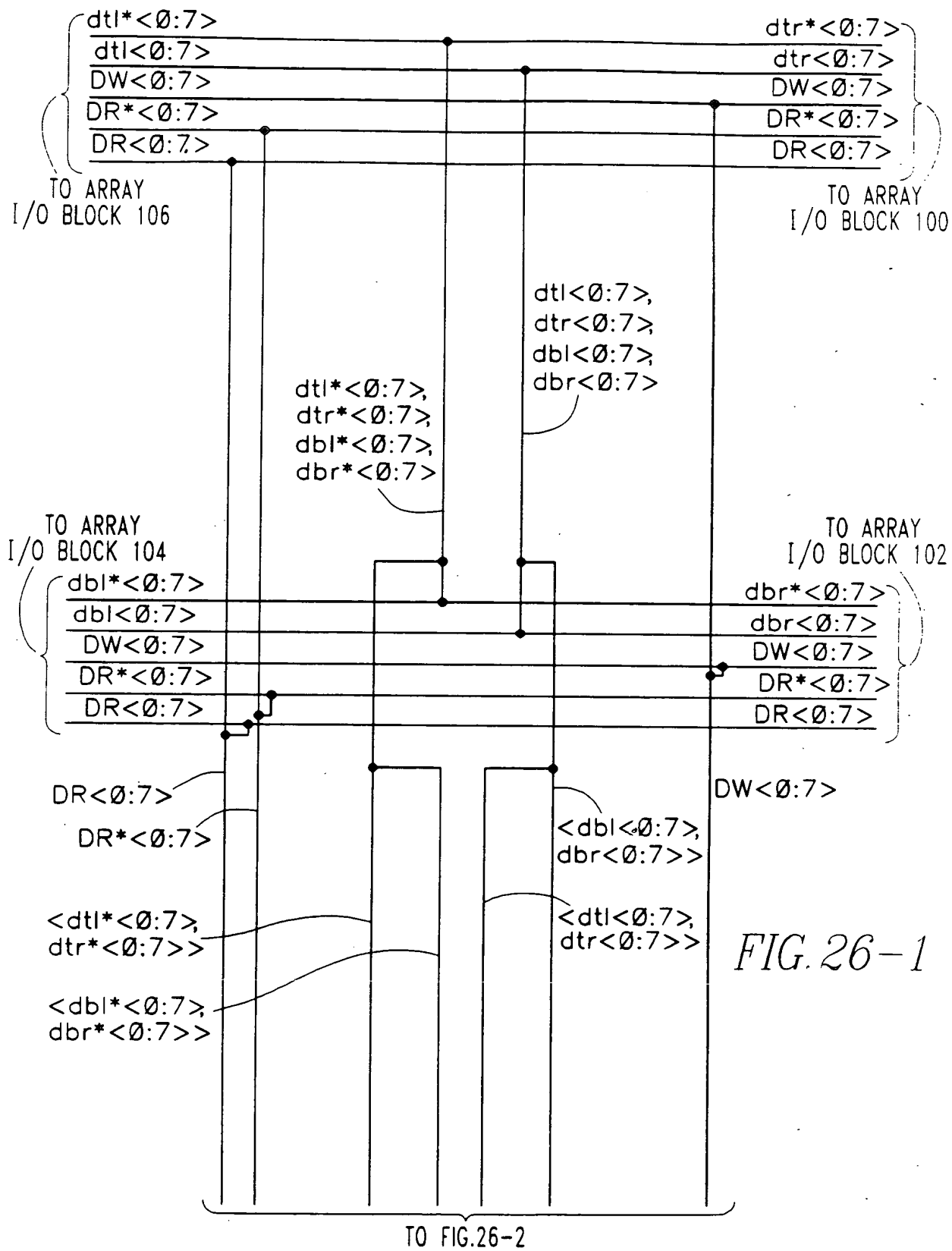


FIG. 26-1

FROM FIG.26-1

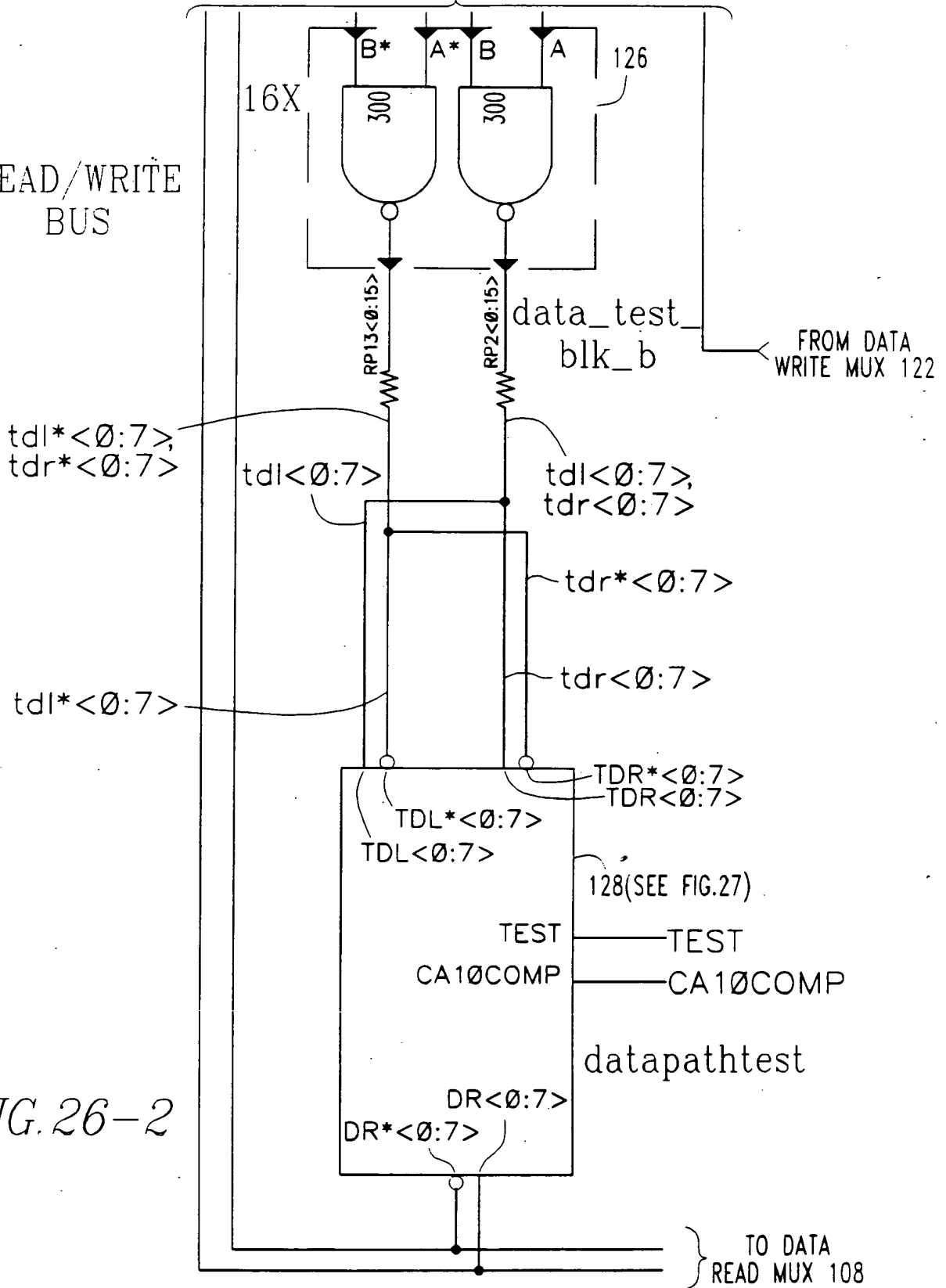
READ/WRITE
BUS

FIG.26-2

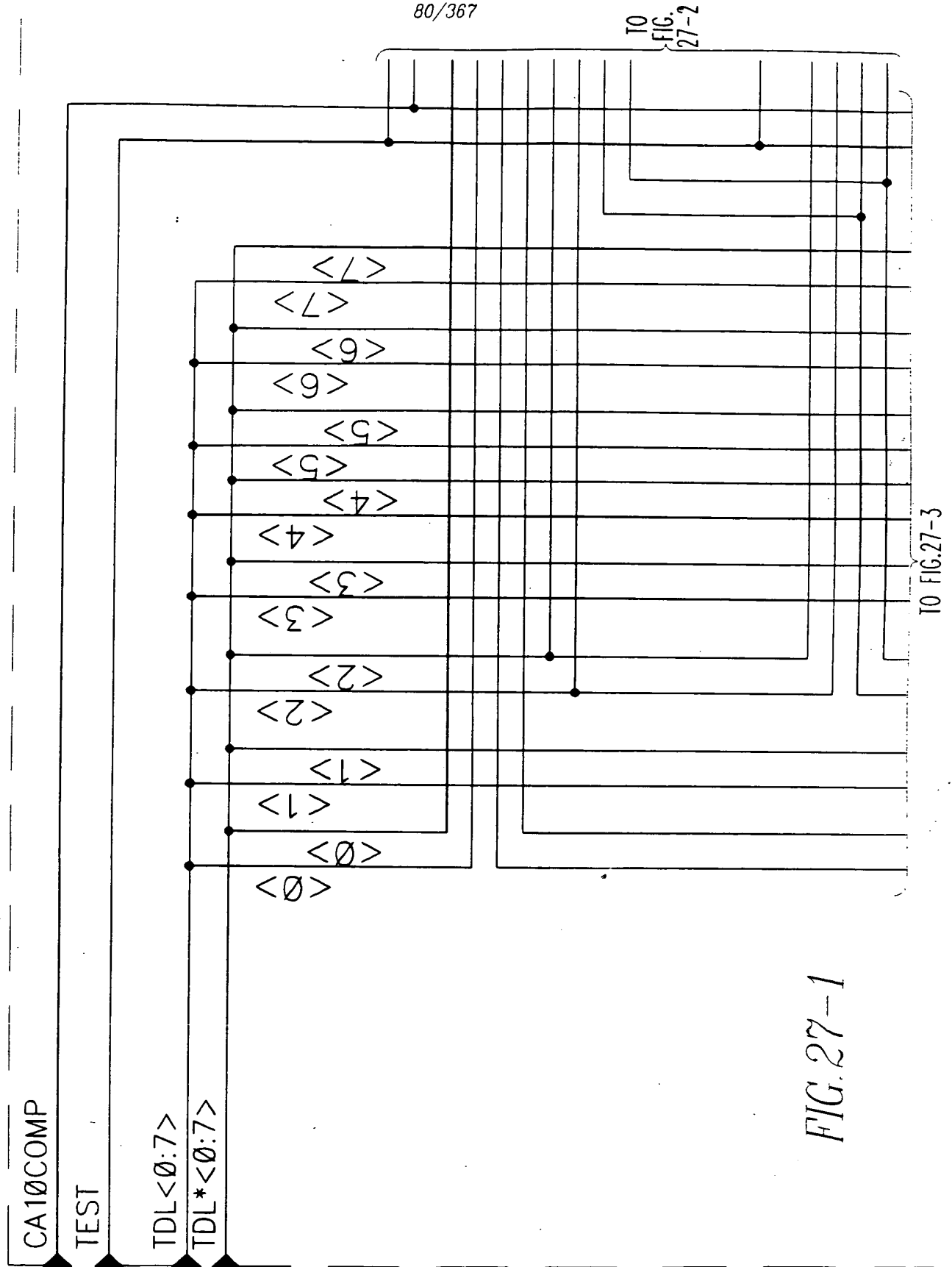
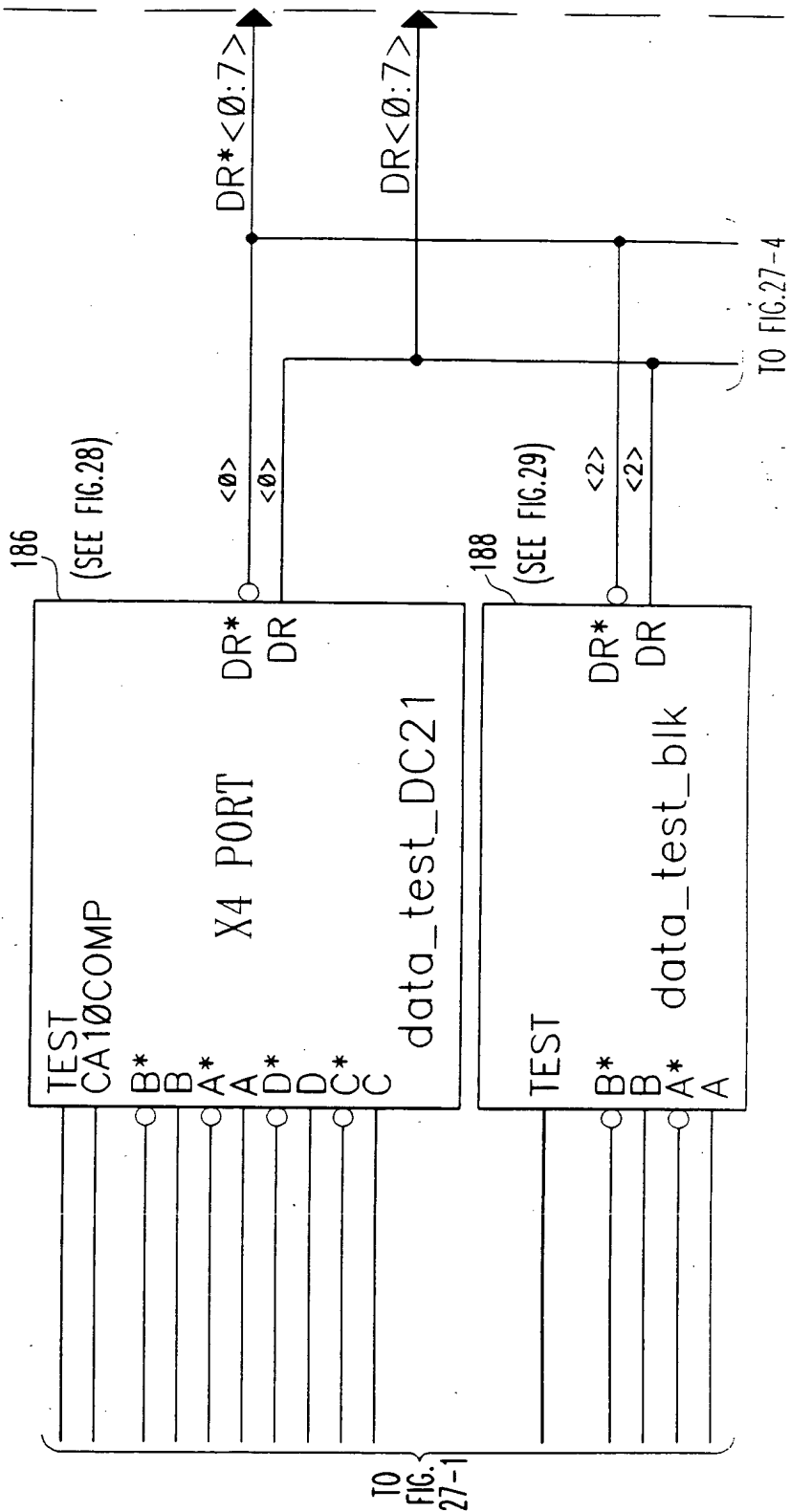


FIG. 27-2

dataPathTest
Block 128



TO FIG. 27-1

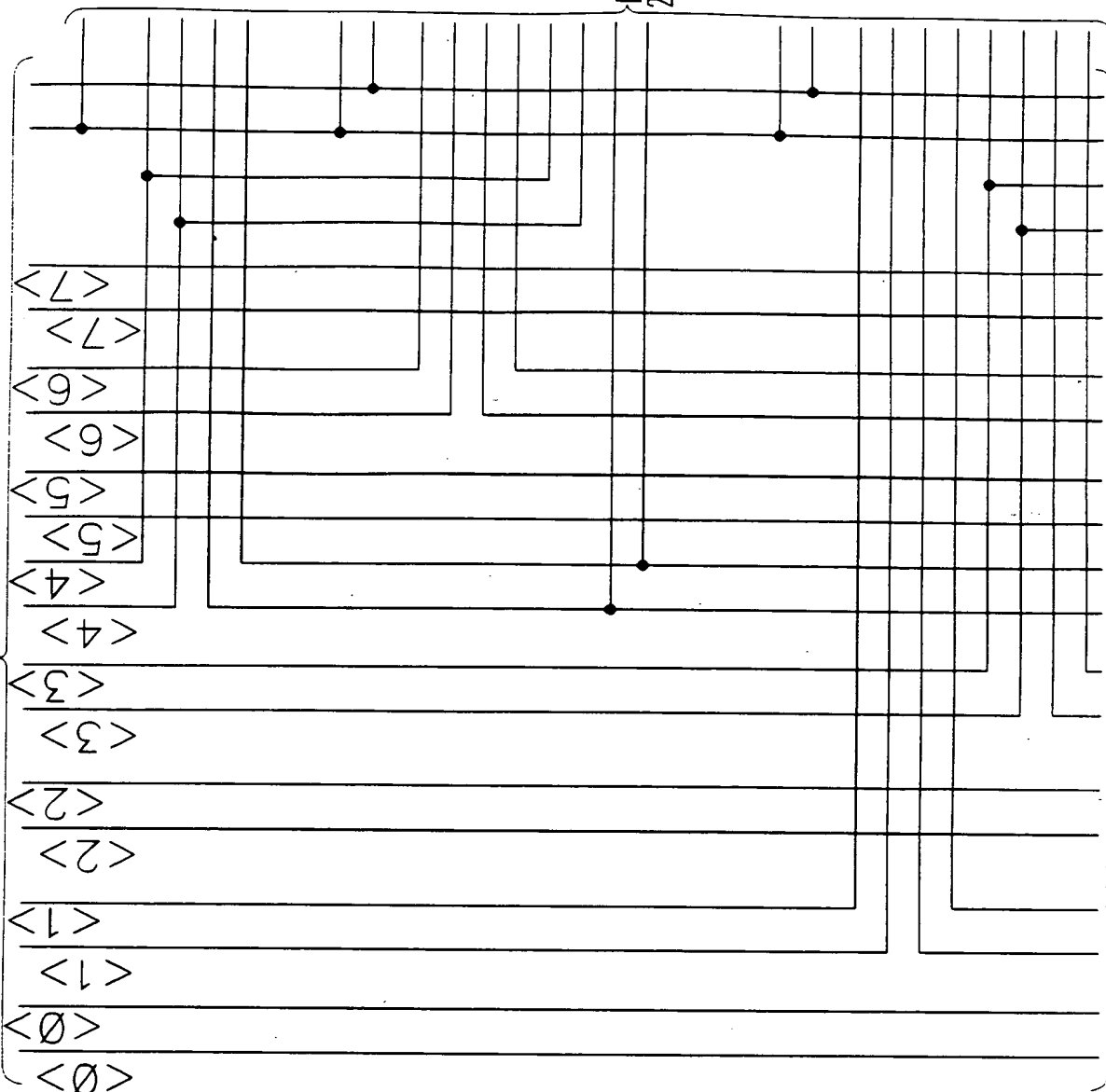


FIG. 27-3

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FIG. 27-4

TO FIG. 27-5

FIG. 27-5

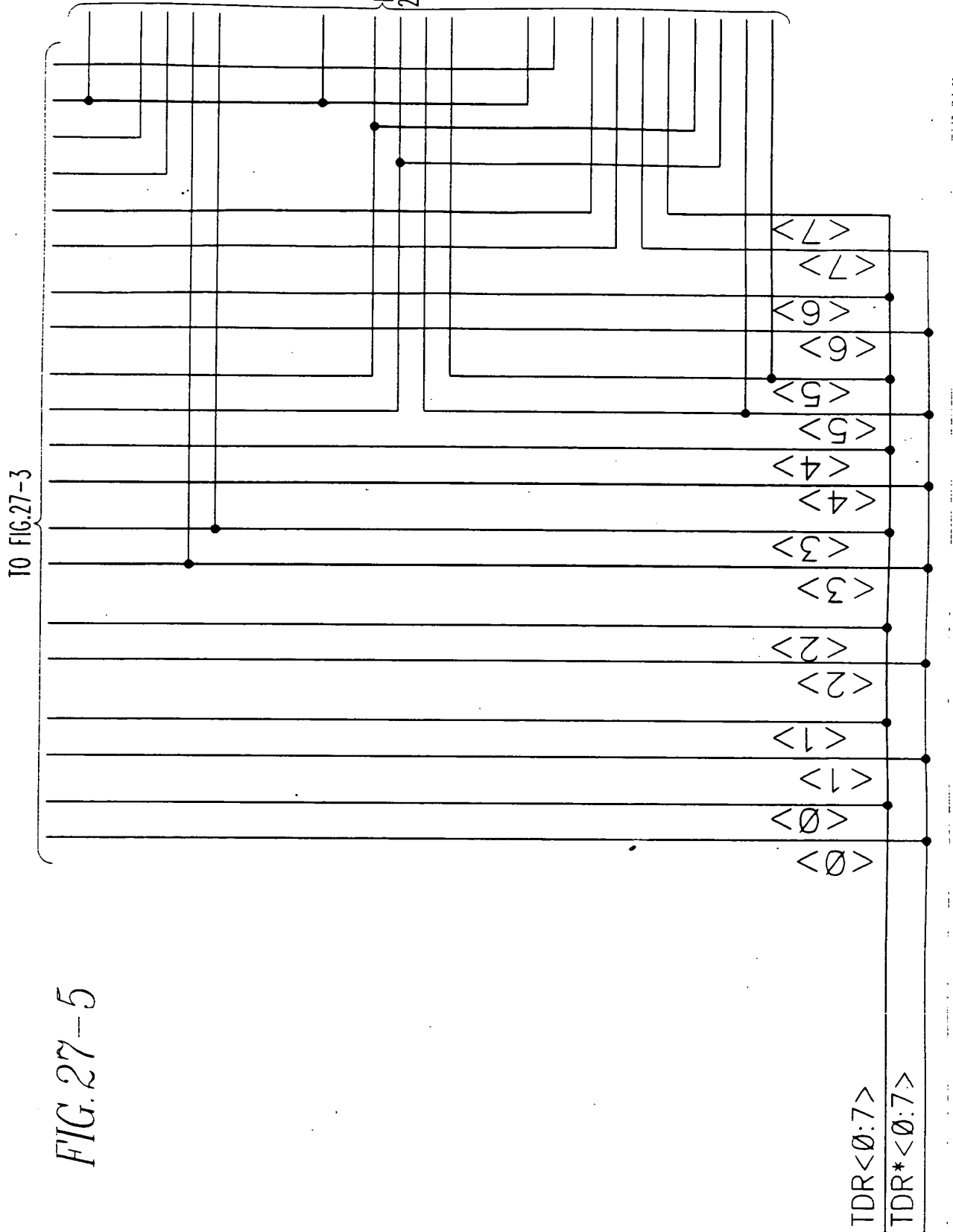


FIG. 27-5

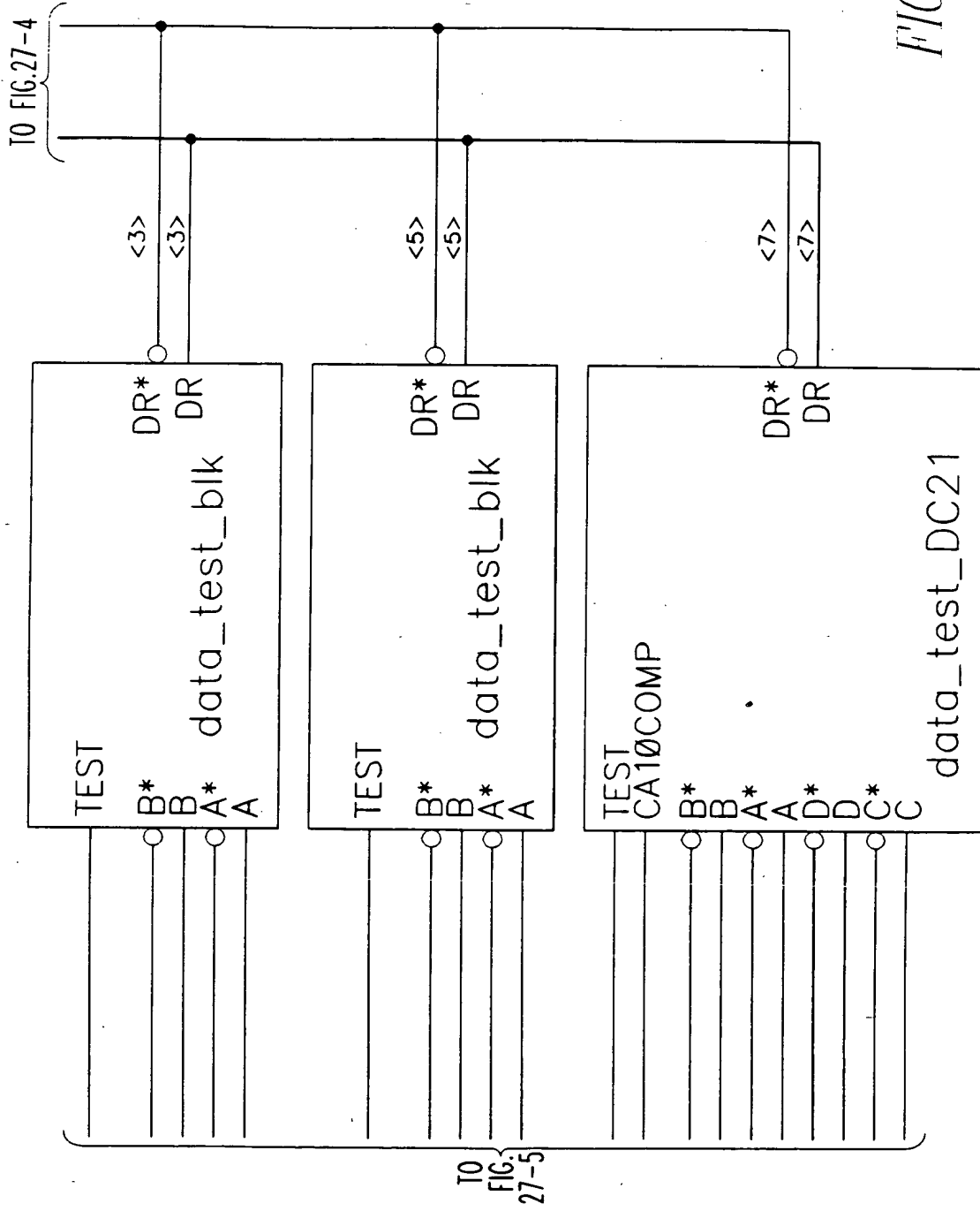


FIG. 27-6

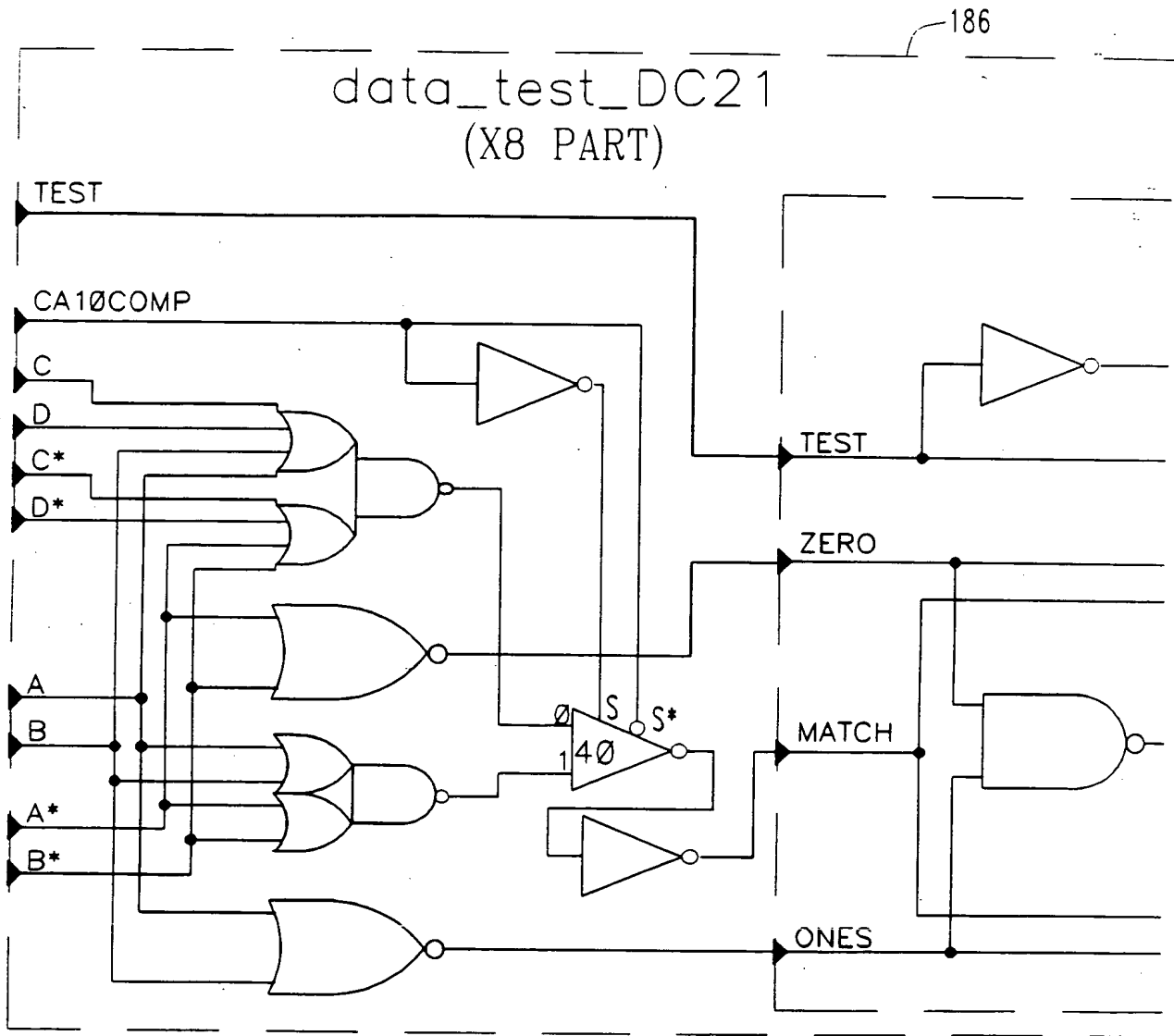


FIG. 28-1

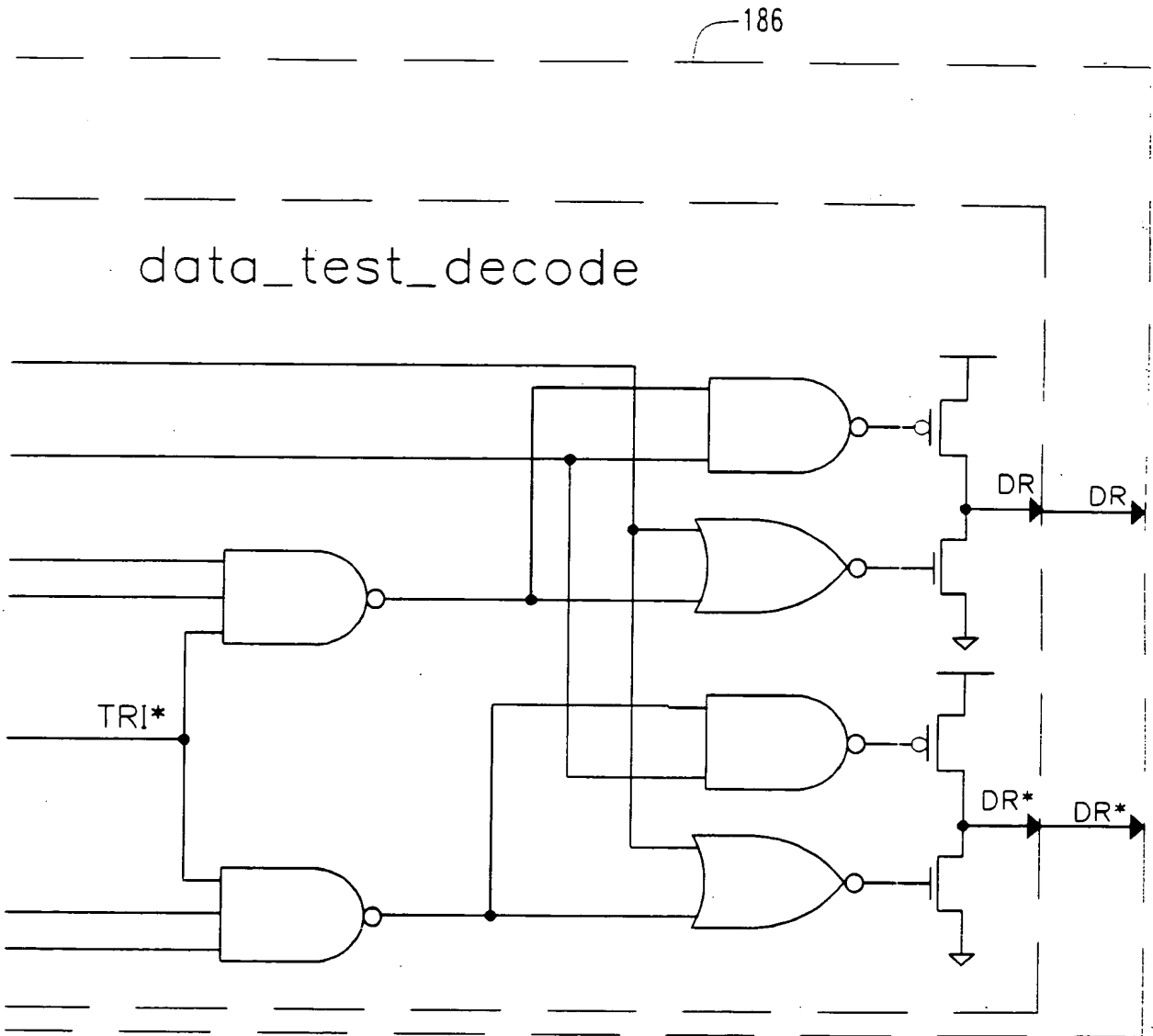
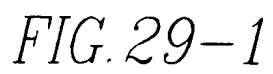


FIG. 28-2



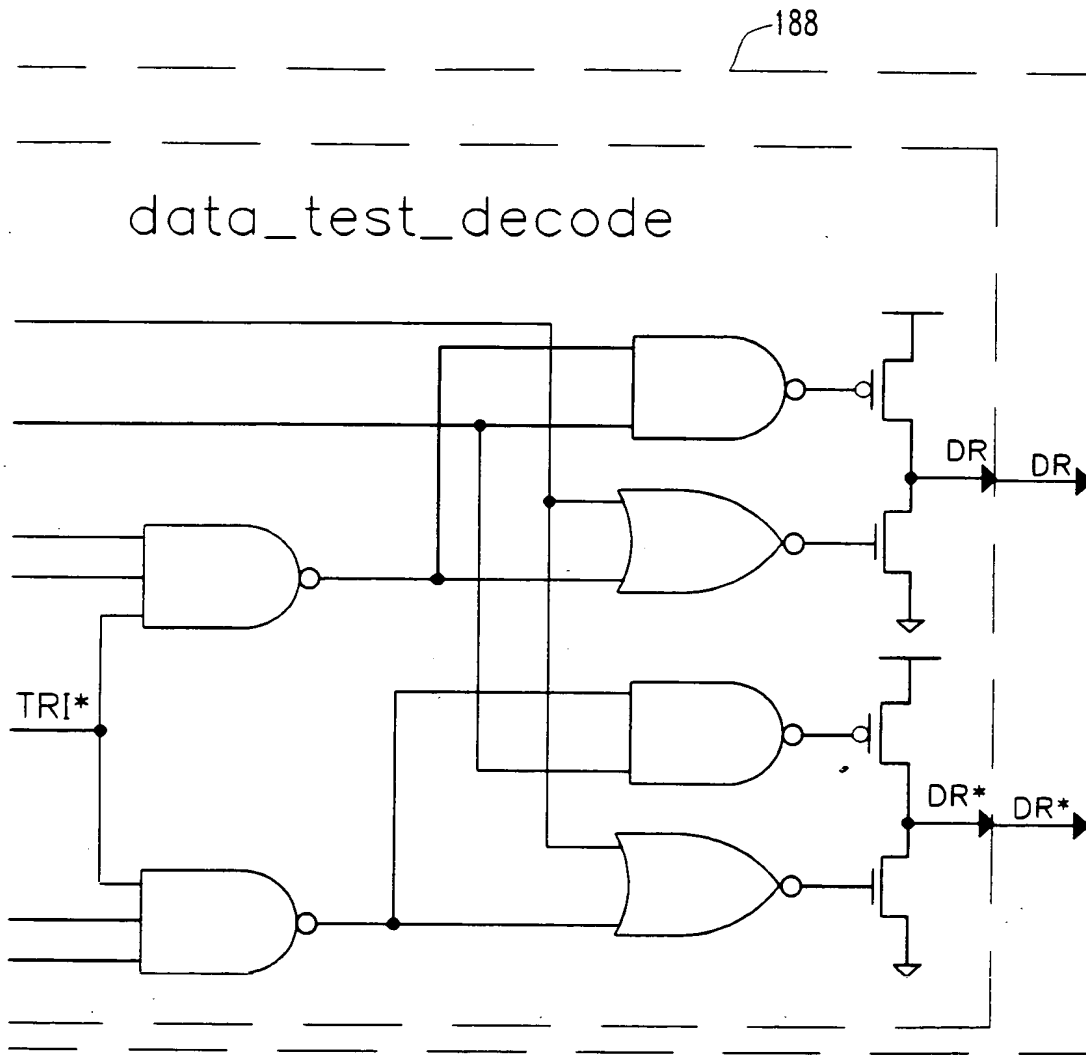
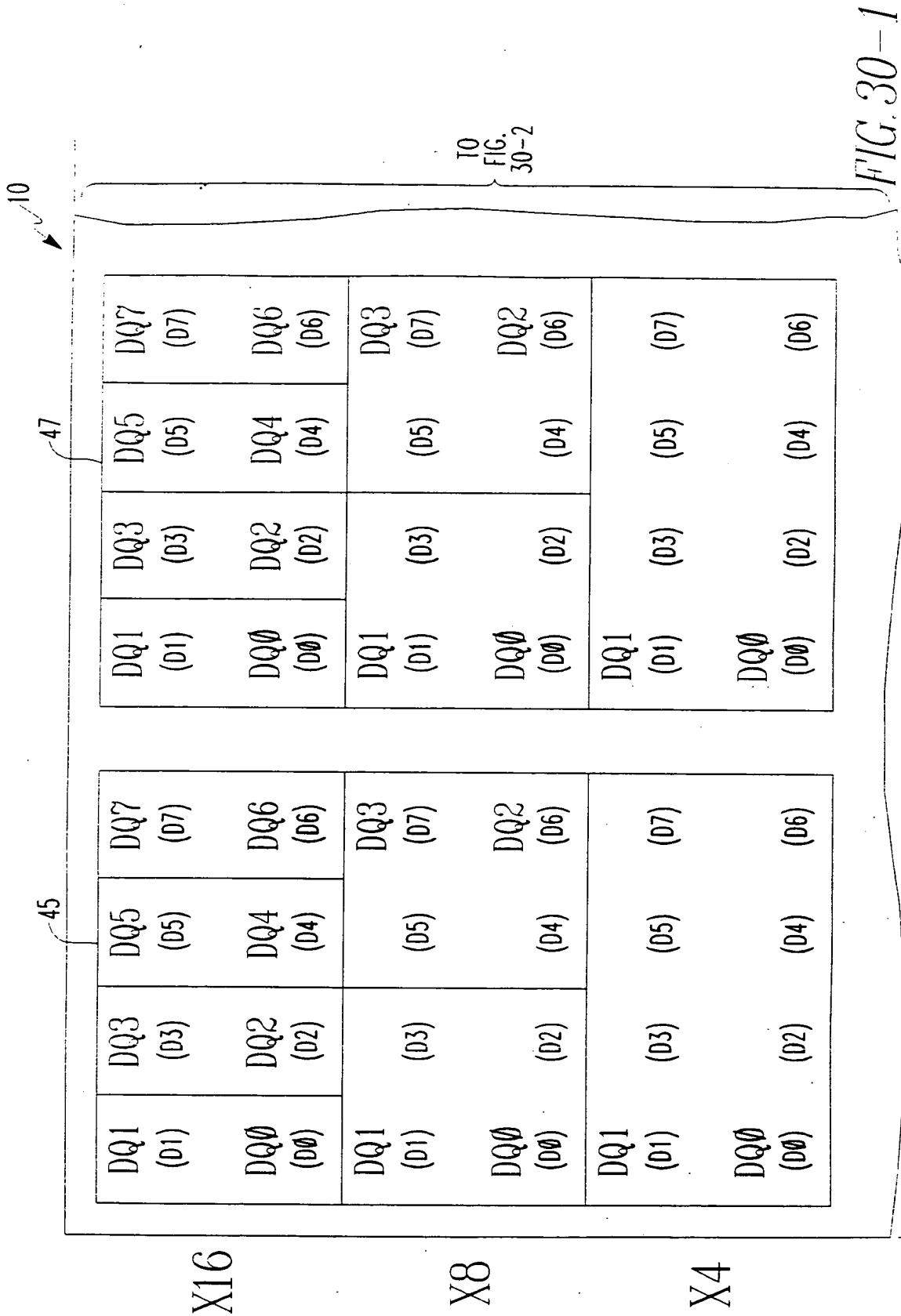
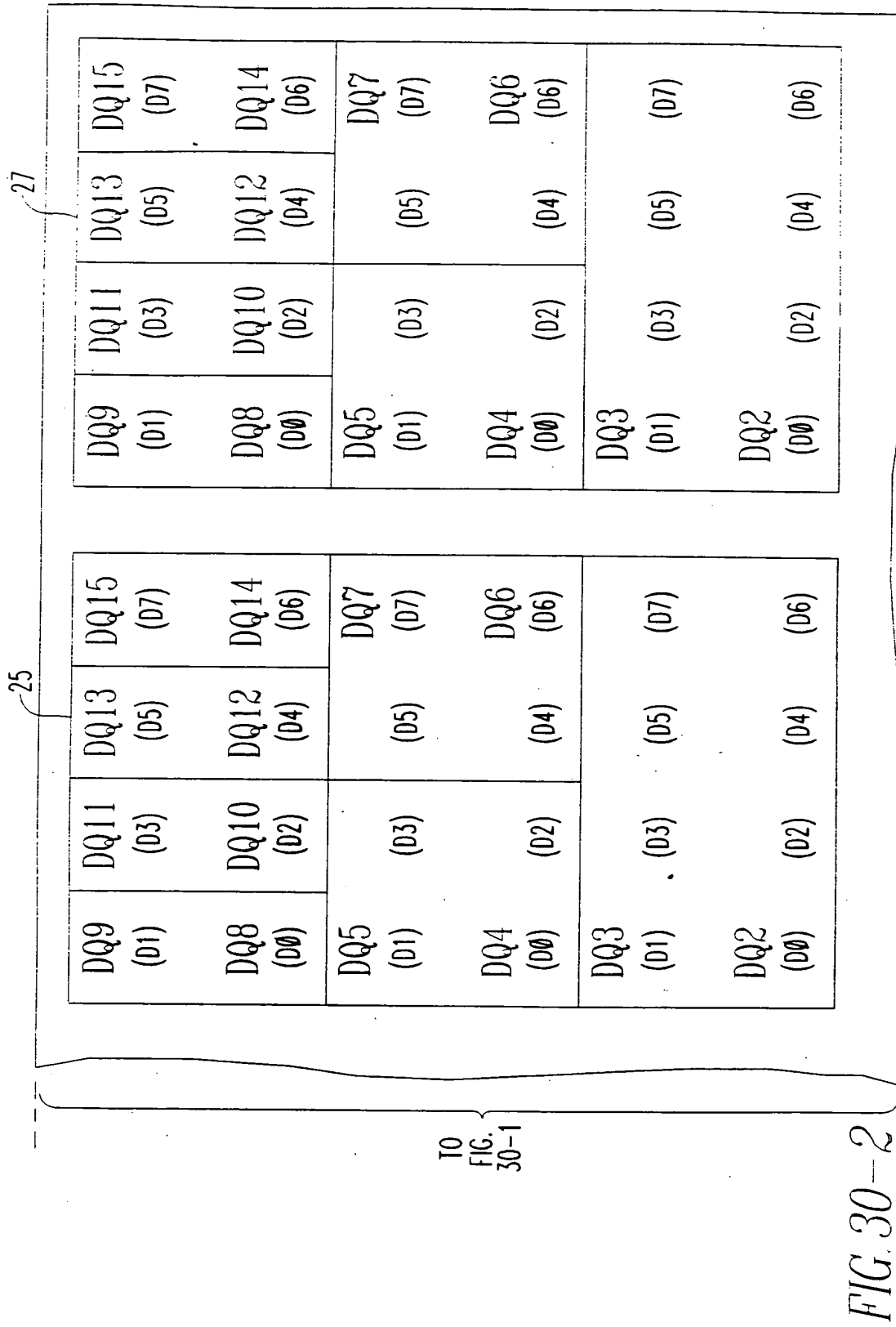


FIG. 29-2





10 FIG. 30-1

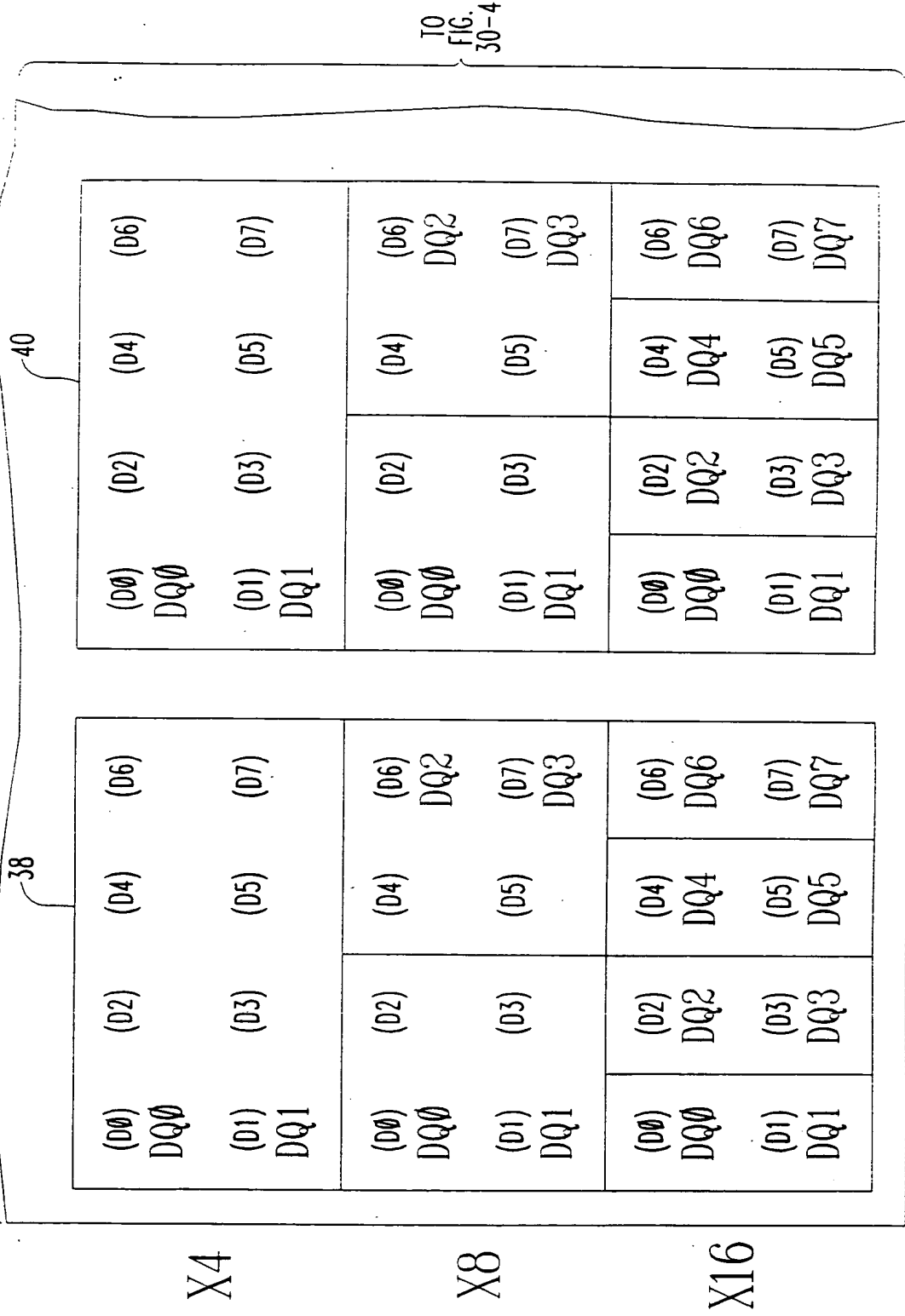


FIG. 30-3

TO FIG. 30-2

<div>31</div>		(00) DQ2	(02)	(04)	(06)
		(01) DQ3	(03)	(05)	(07)
<div>33</div>		(00) DQ4	(02)	(04)	(06) DQ6
		(01) DQ5	(03)	(05)	(07) DQ7
		(00) DQ8	(02) DQ10	(04) DQ12	(06) DQ14
		(01) DQ9	(03) DQ11	(05) DQ13	(07) DQ15

TO
FIG.
30-3

FIG. 30-4

TO FIG. 31A1
↓

N/C	N/C	VSSQ	VSS	VCC1 Probe							
N/C	N/C	VSSQ	VSS	NCSV							
VSSQ	DQ4	VSSQ	VSS	NCSV							
12	13	14	15	16	17	18	19	20	21	22	23
DQ3	VCCQ	VCCX	WE								
N/C	VCCQ	VCCX	WE								
N/C	VCCQ	VCCX	WE								

FIG. 31A2

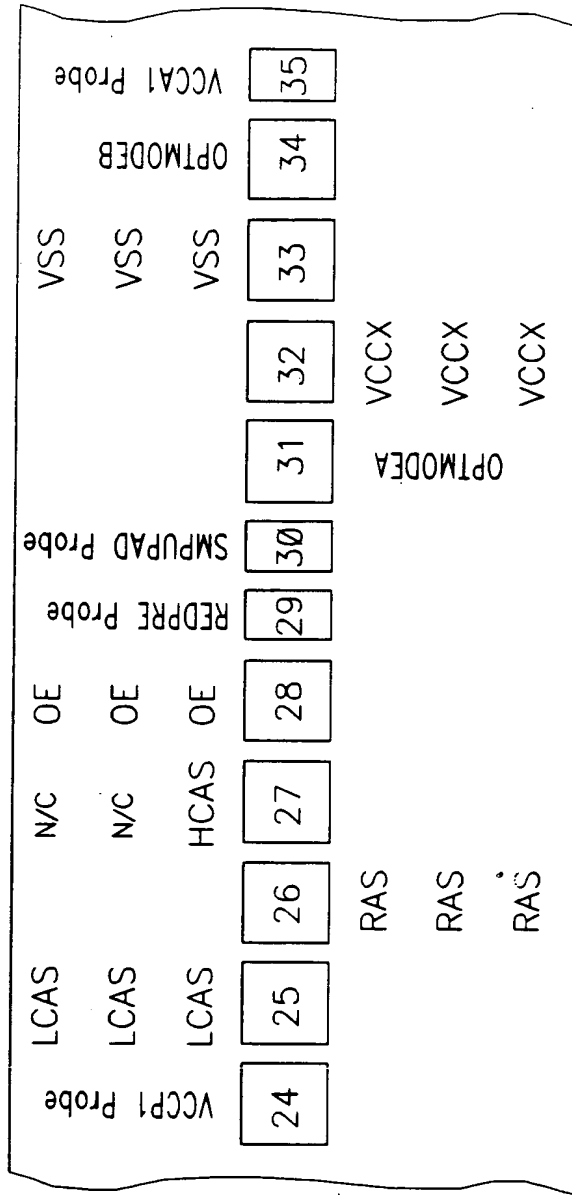


FIG. 31B1

FIG. 31B2

FIG. 31B1

TO FIG. 31B1

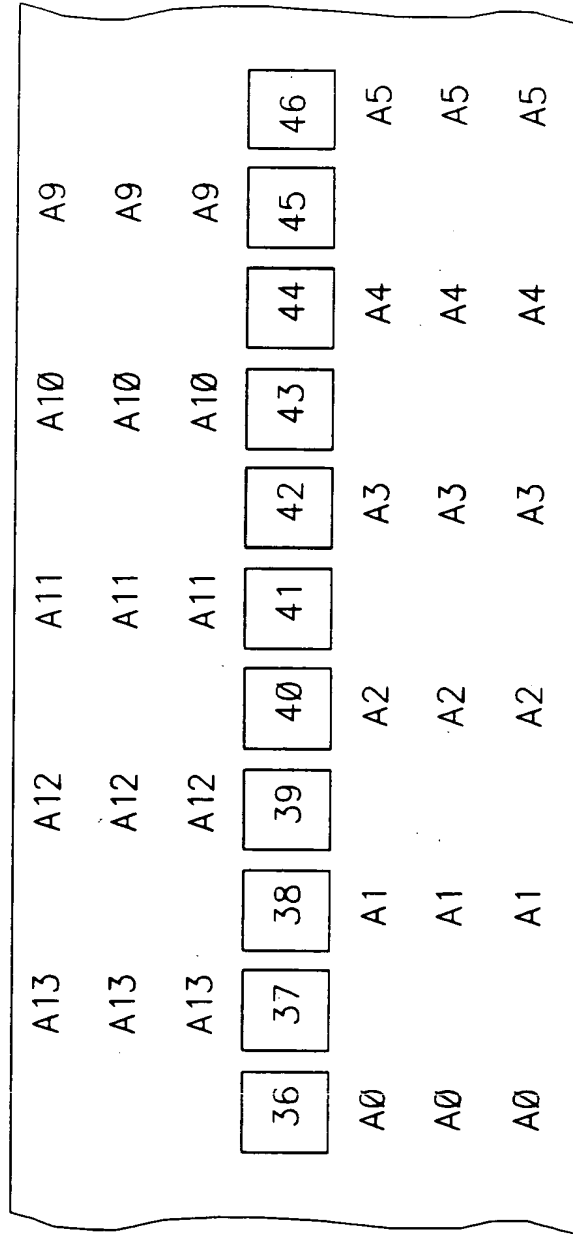


FIG. 31B2

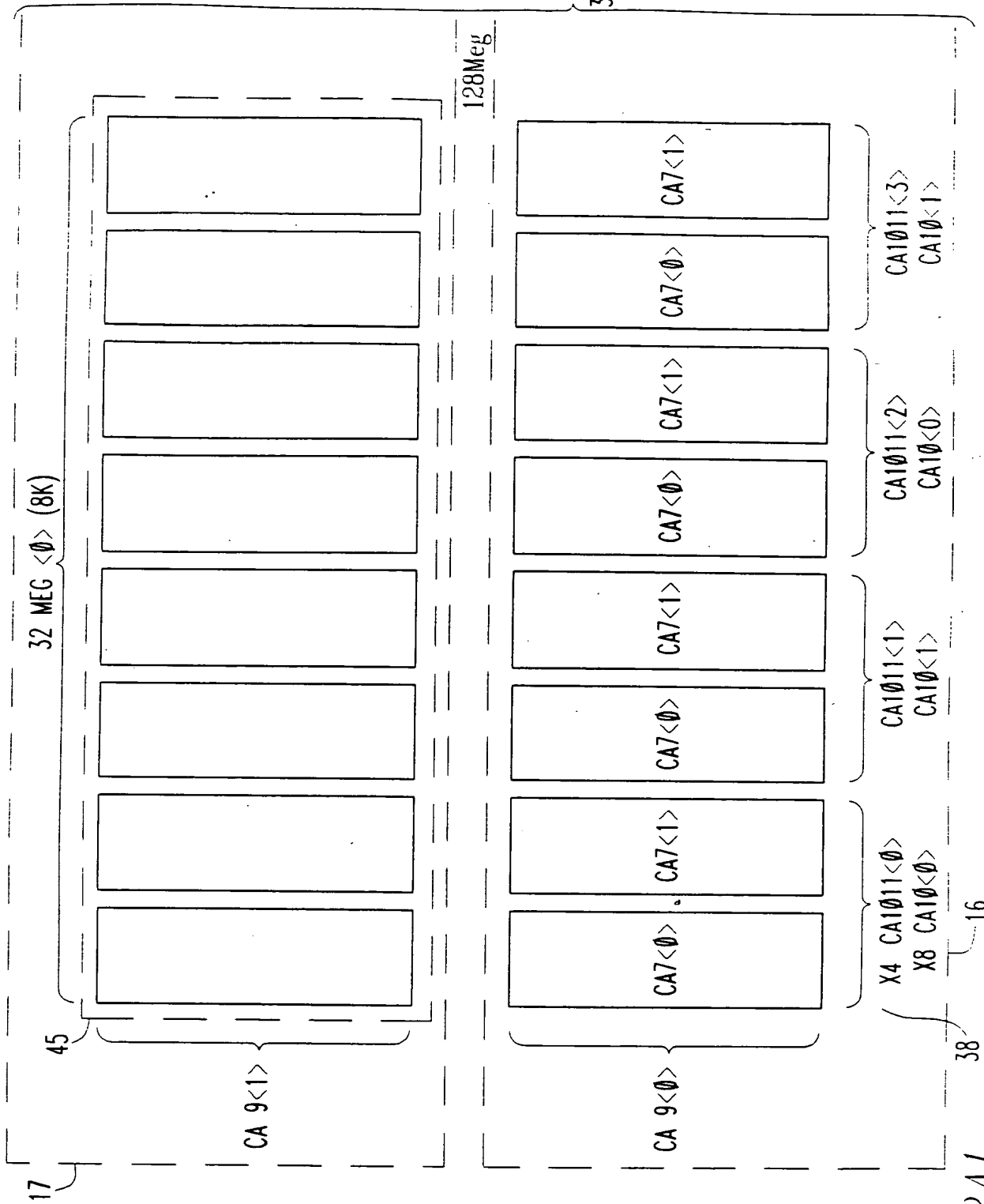
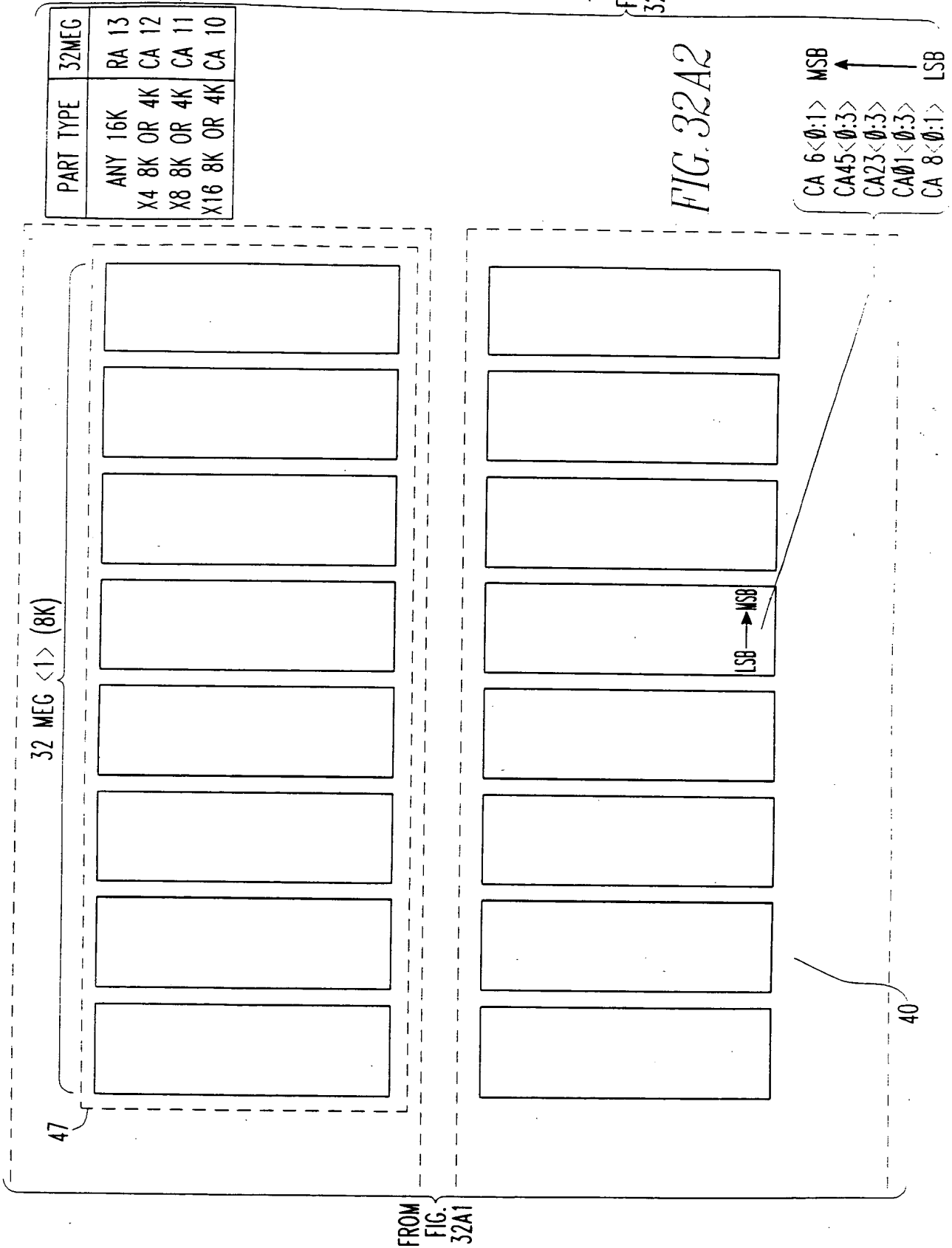


FIG. 32A1



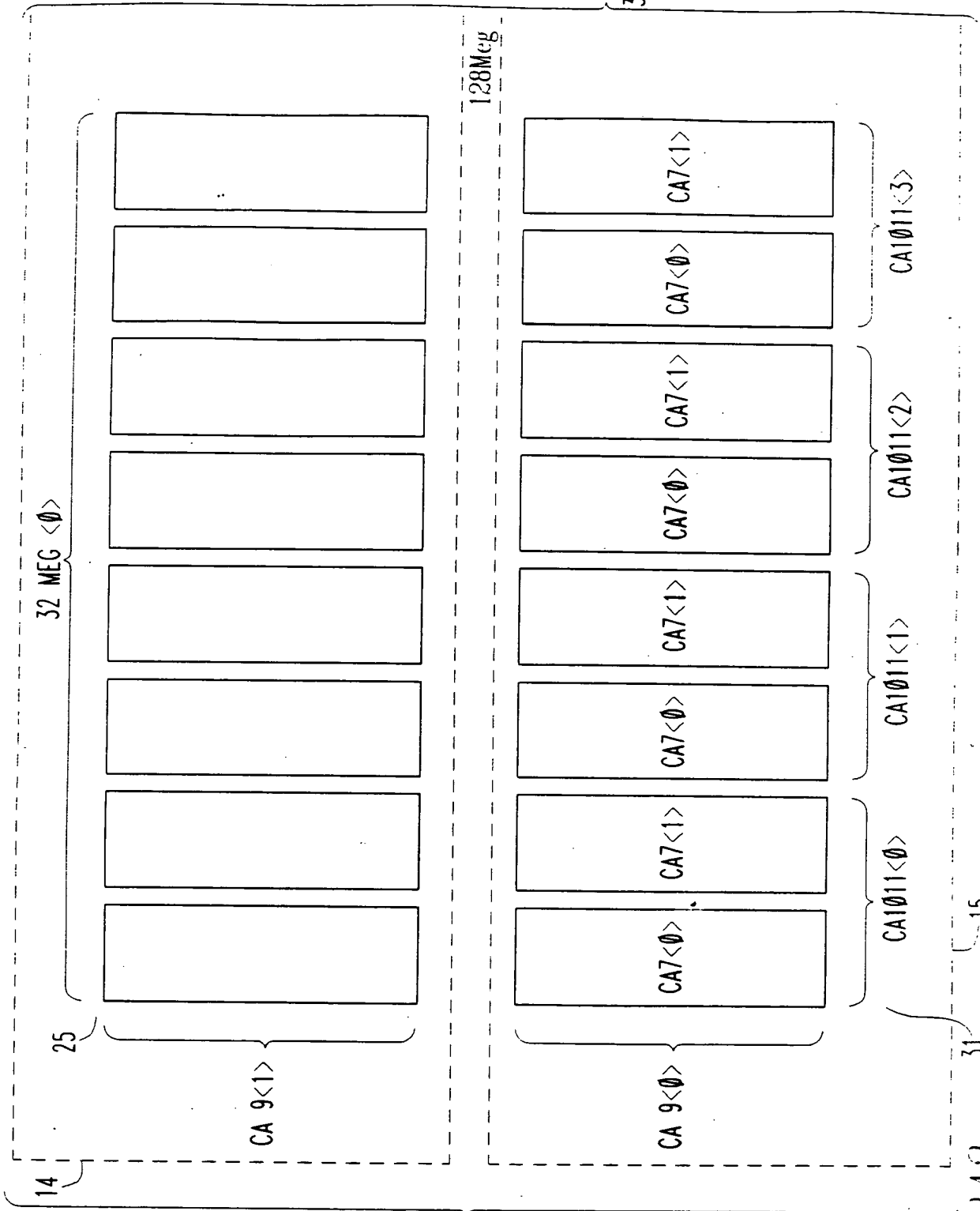


FIG. 32A3

FIG. 32A3

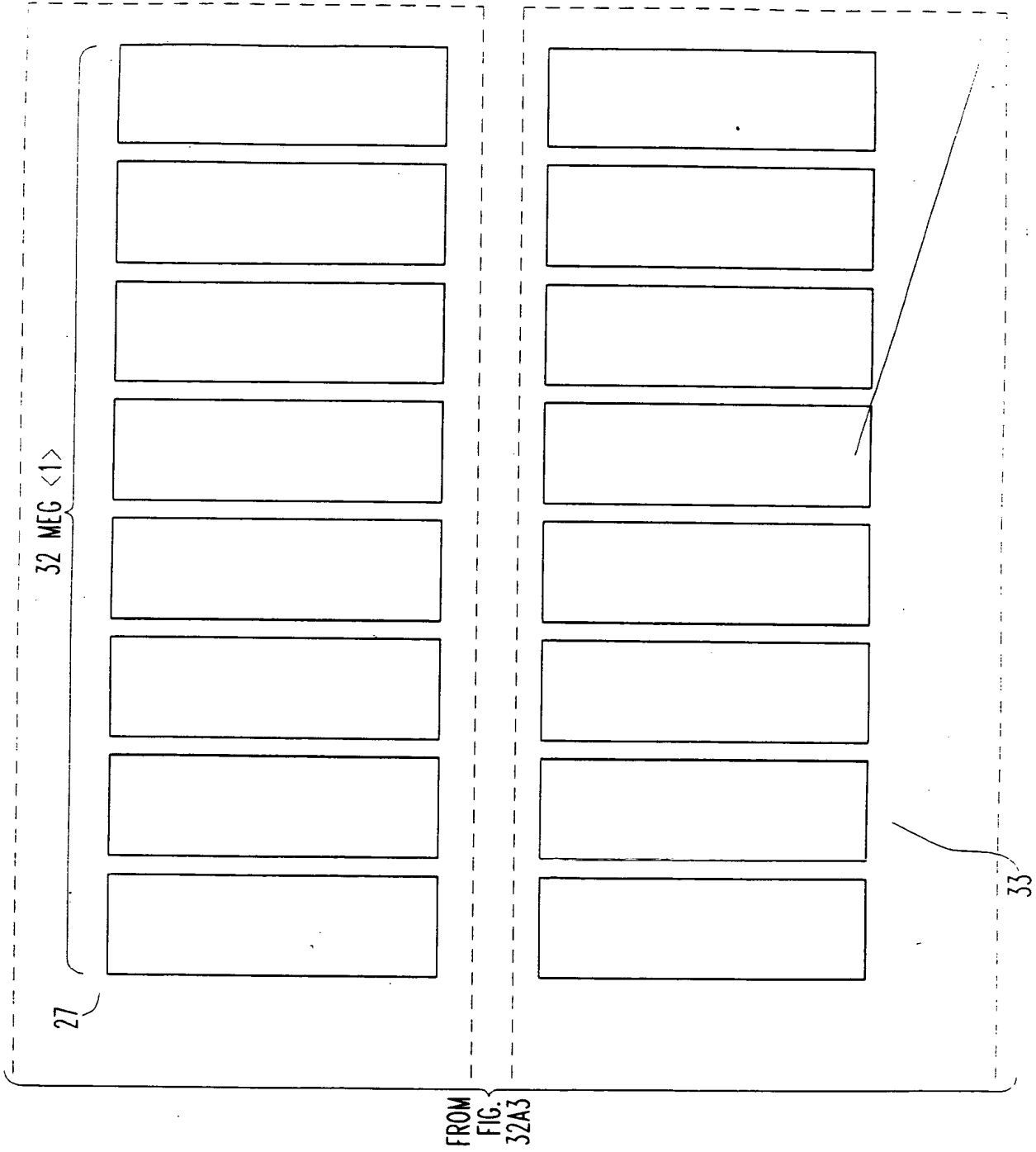


FIG. 32A4

CA 6 <0:1> MSB
 CA 45 <0:3>
 CA 23 <0:3>
 CA 01 <0:3>
 CA 8 <0:1> LSB

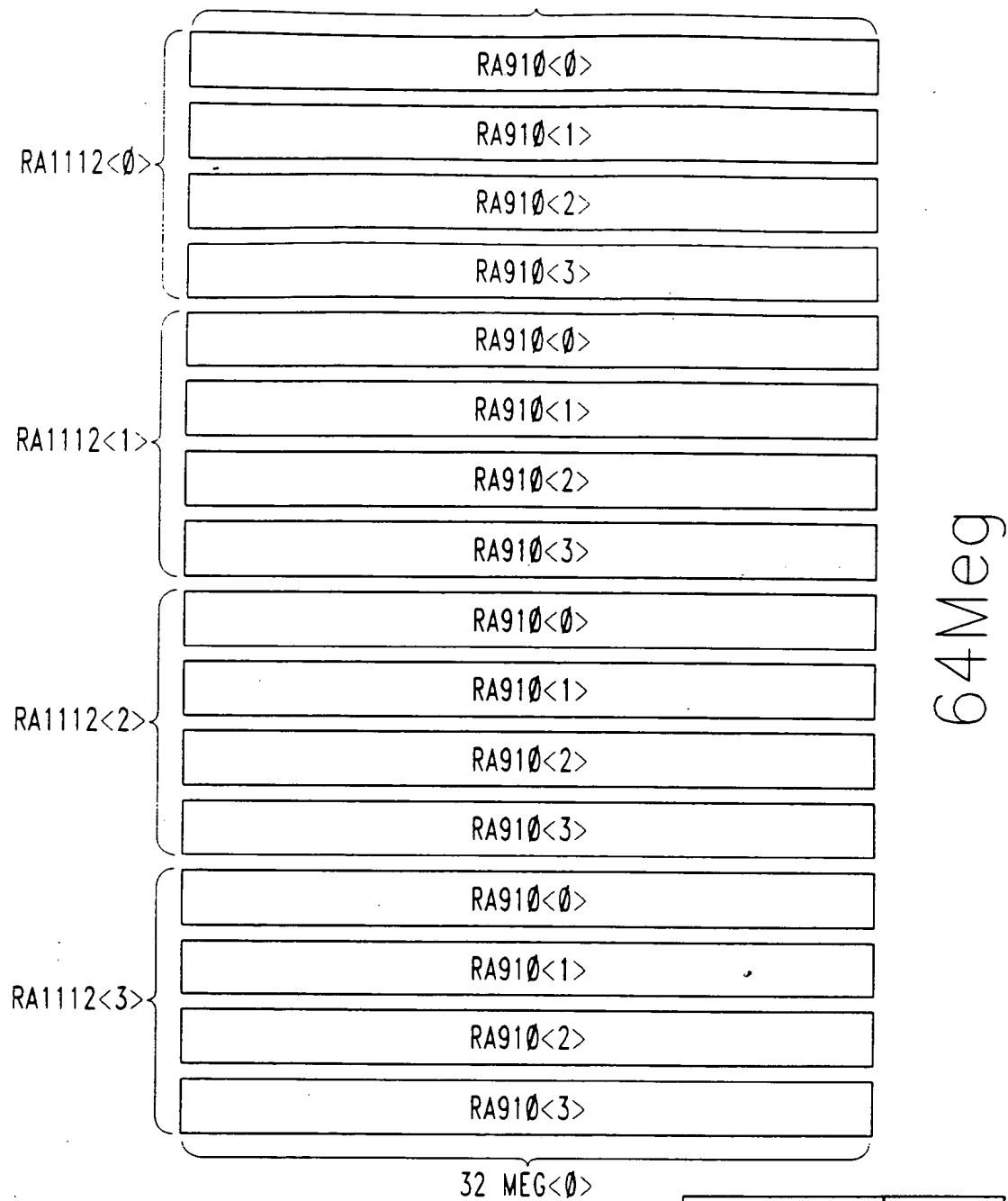


FIG. 32B1

PART TYPE	32MEG
ANY 16K	RA_13
X4 8K OR 4K	CA_12
X8 8K OR 4K	CA_11
X16 8K OR 4K	CA_10

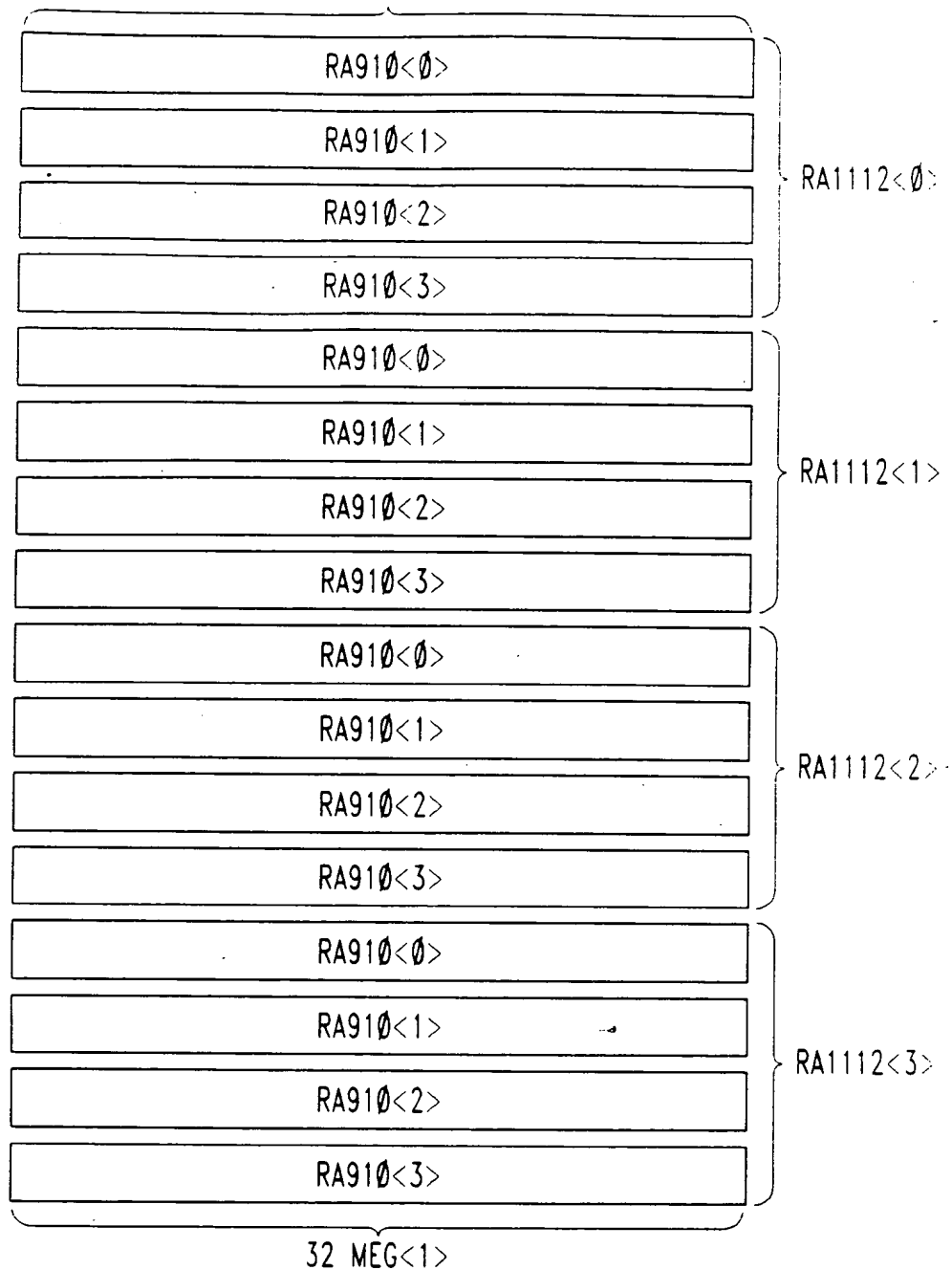
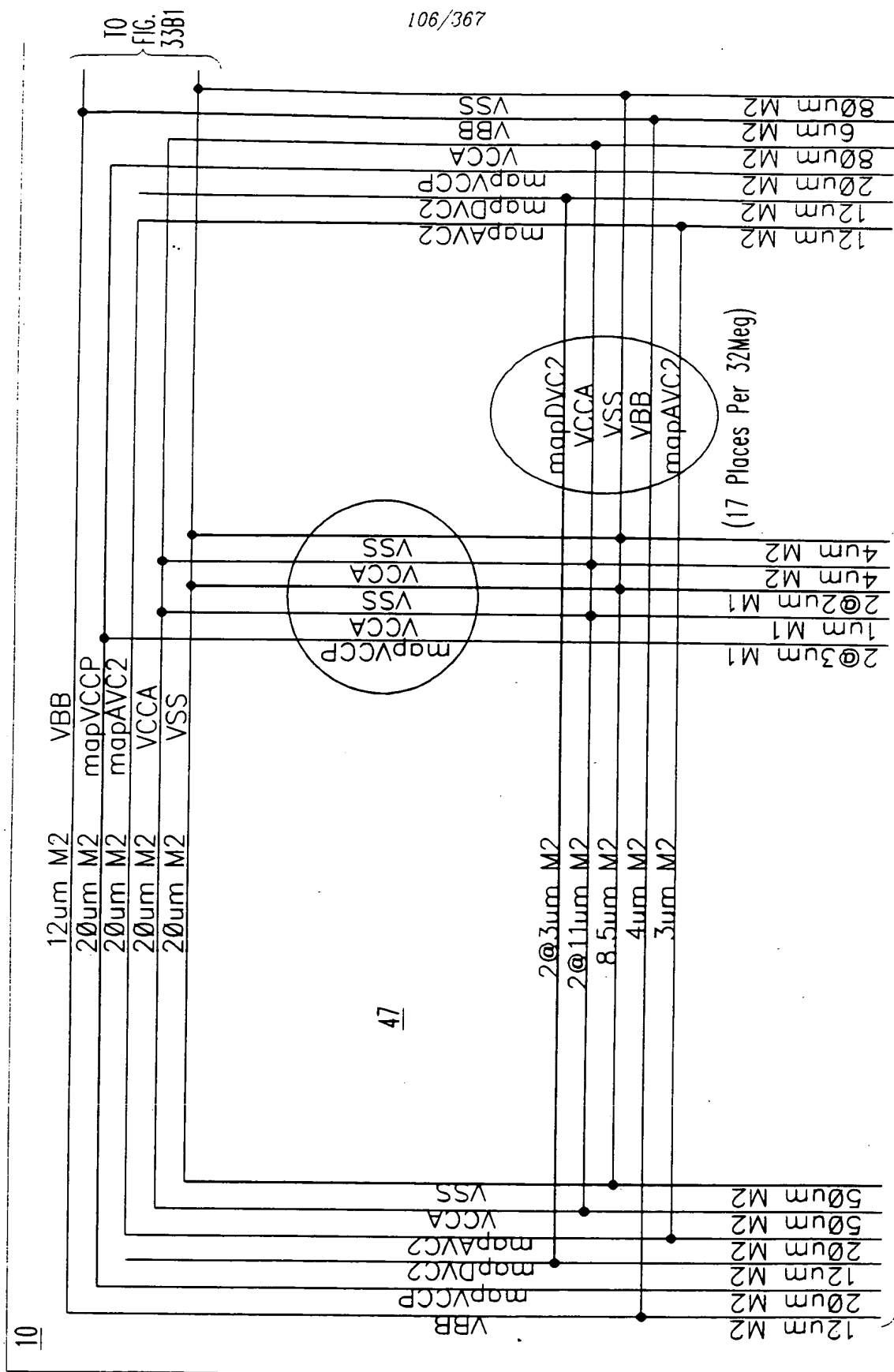


FIG. 32B2



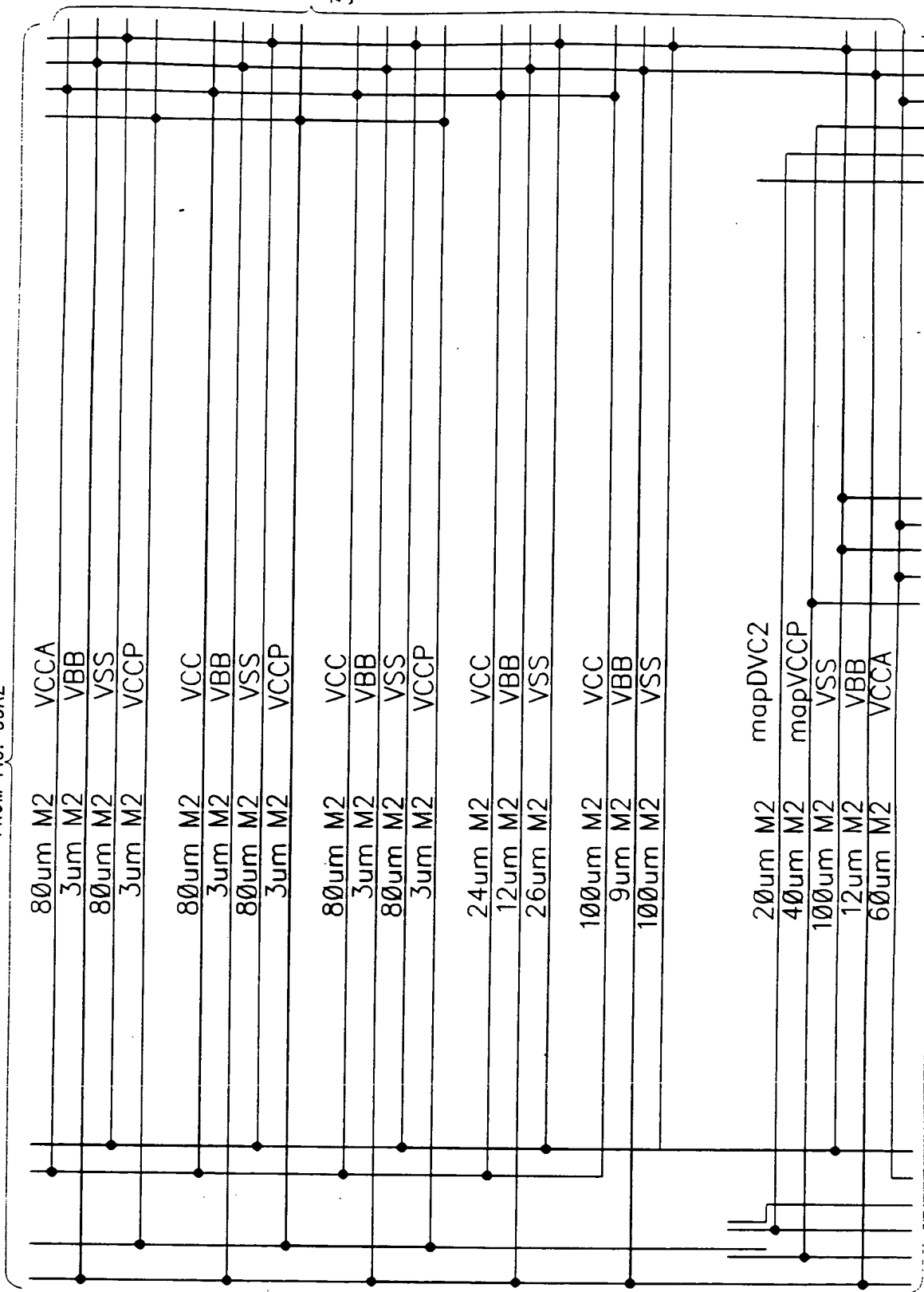
TO FIG. 33A2

FIG. 33A

[illegible]

FIG. 33A2

TO FIG. 33A4



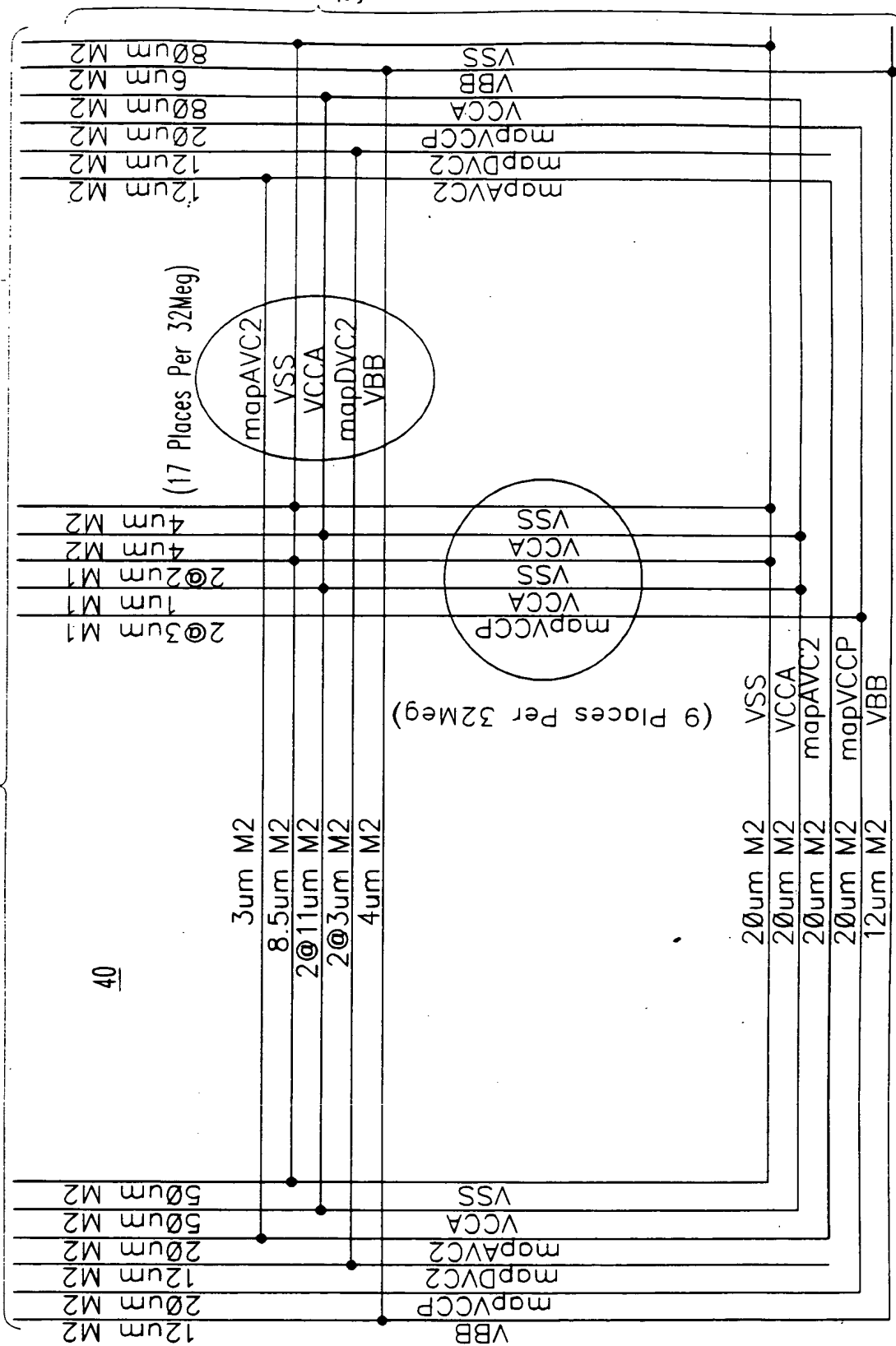
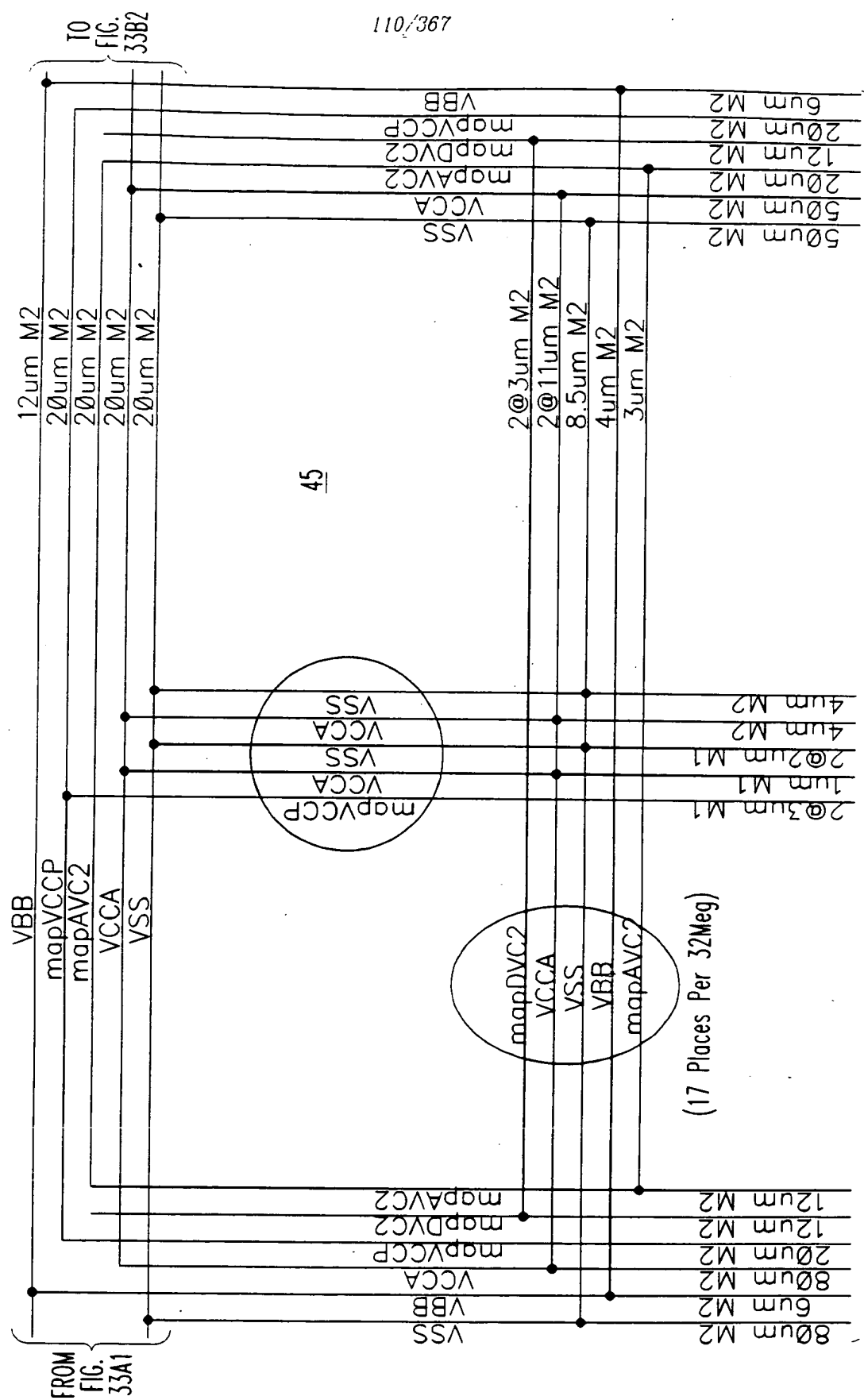
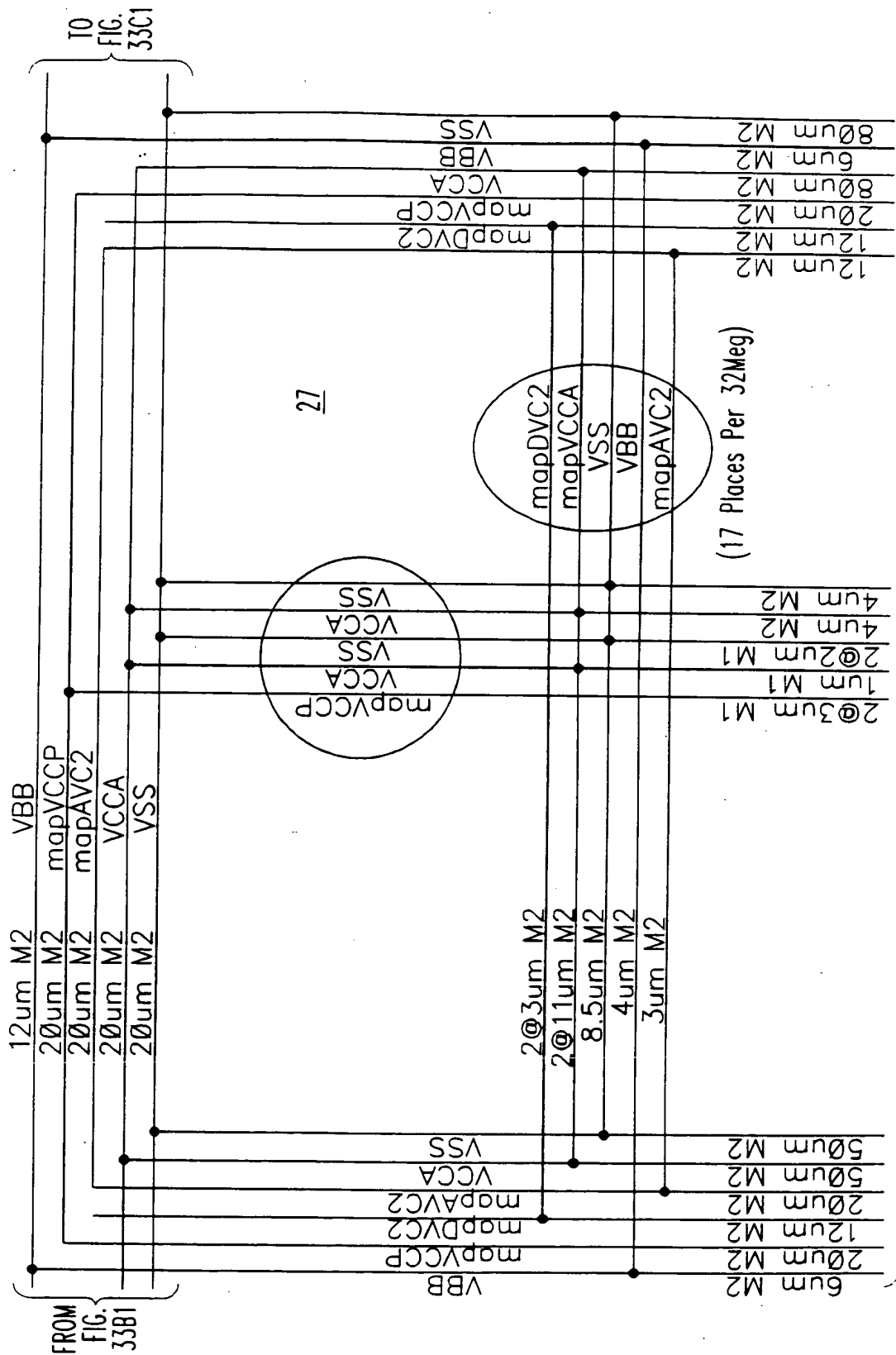


FIGURE 33A



TO FIG. 33B3

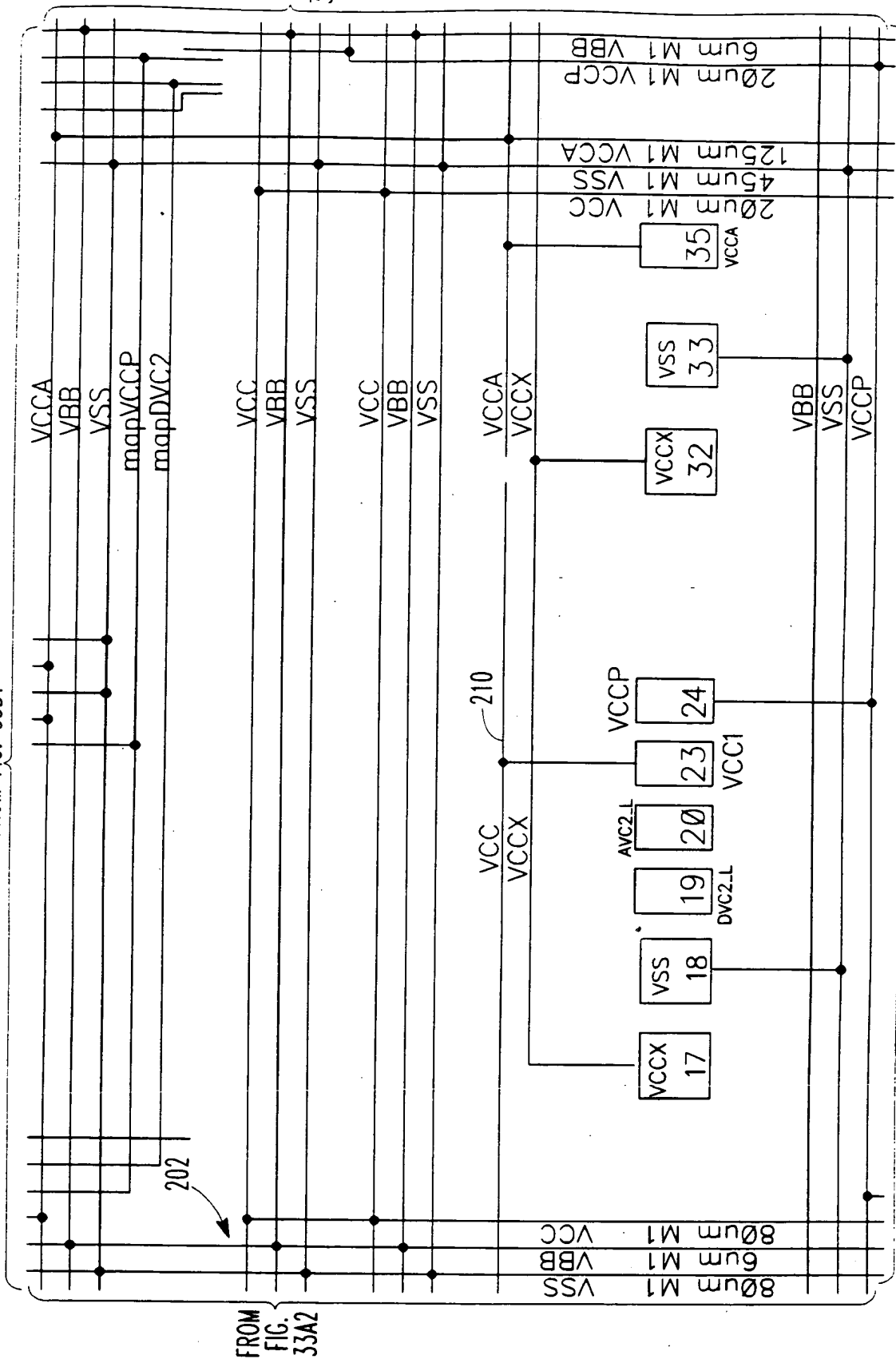
17C-3331



TO FIG. 33B4

FIG. 33B2

FROM FIG. 33B1



FROM
FIG.
33A2

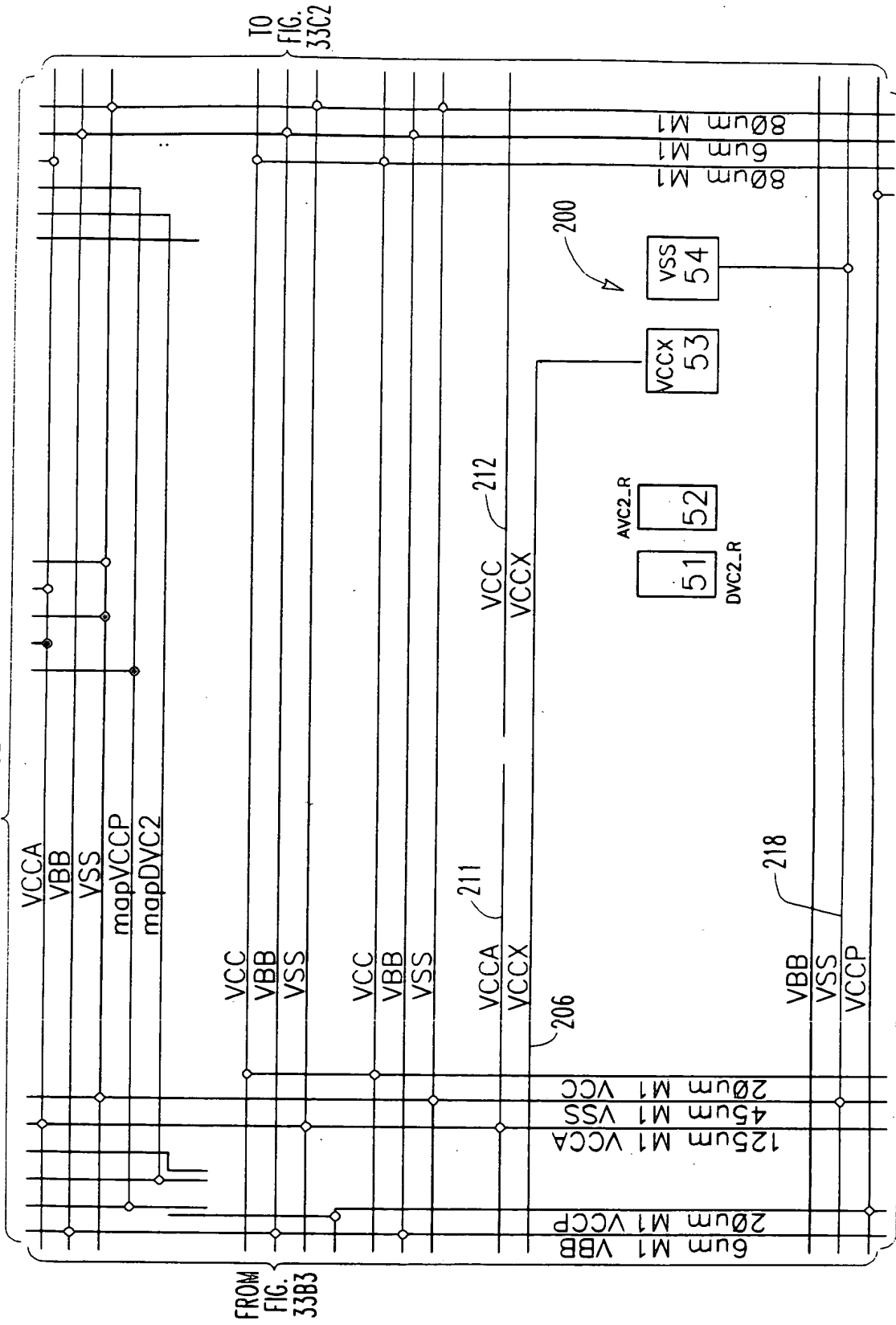
FIG.
33B4

112/367

TO FIG. 33B3

FIG. 33B3

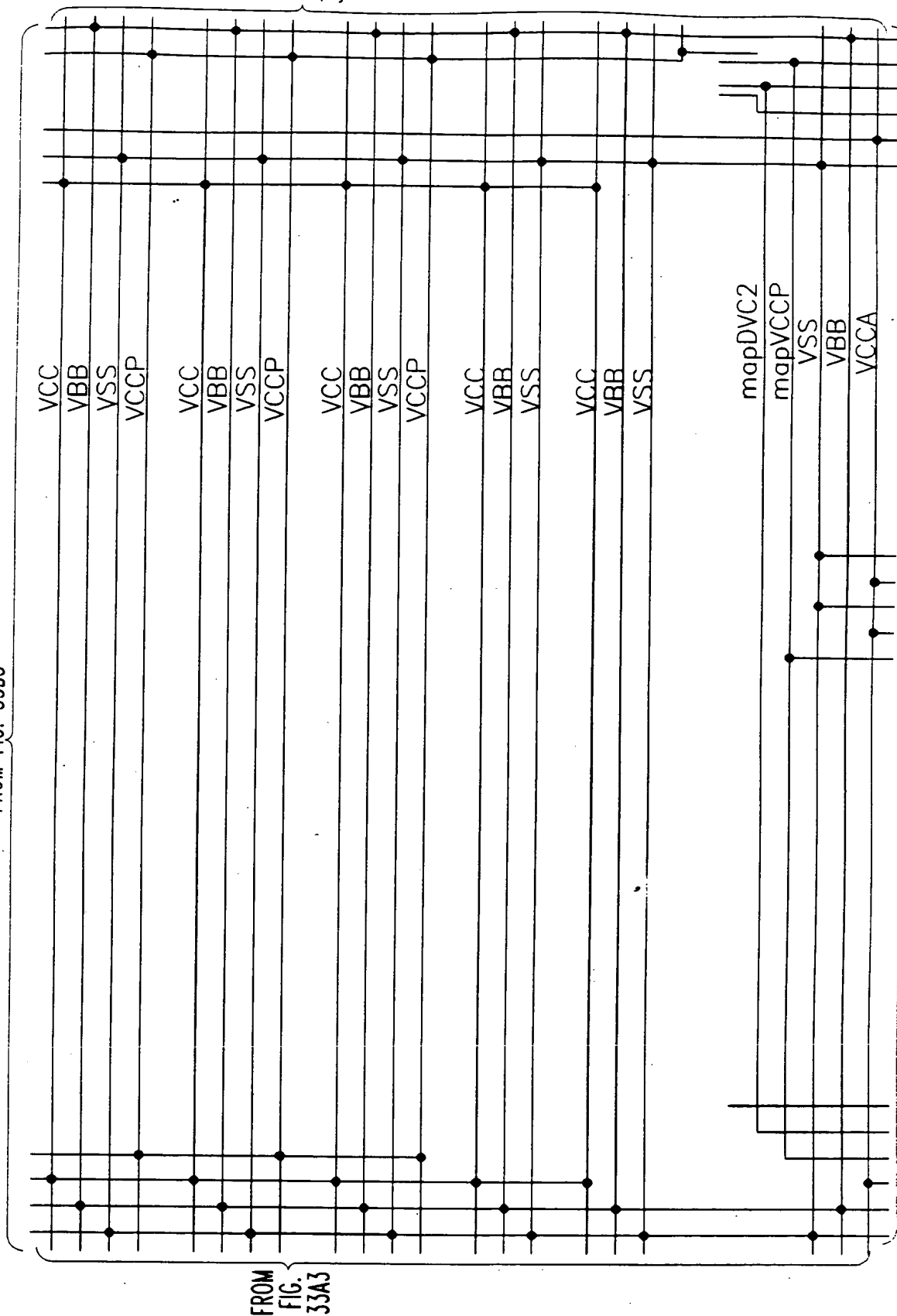
FROM FIG. 33B2



TO FIG. 33B6

FIG. 33B4

FROM FIG. 33B3

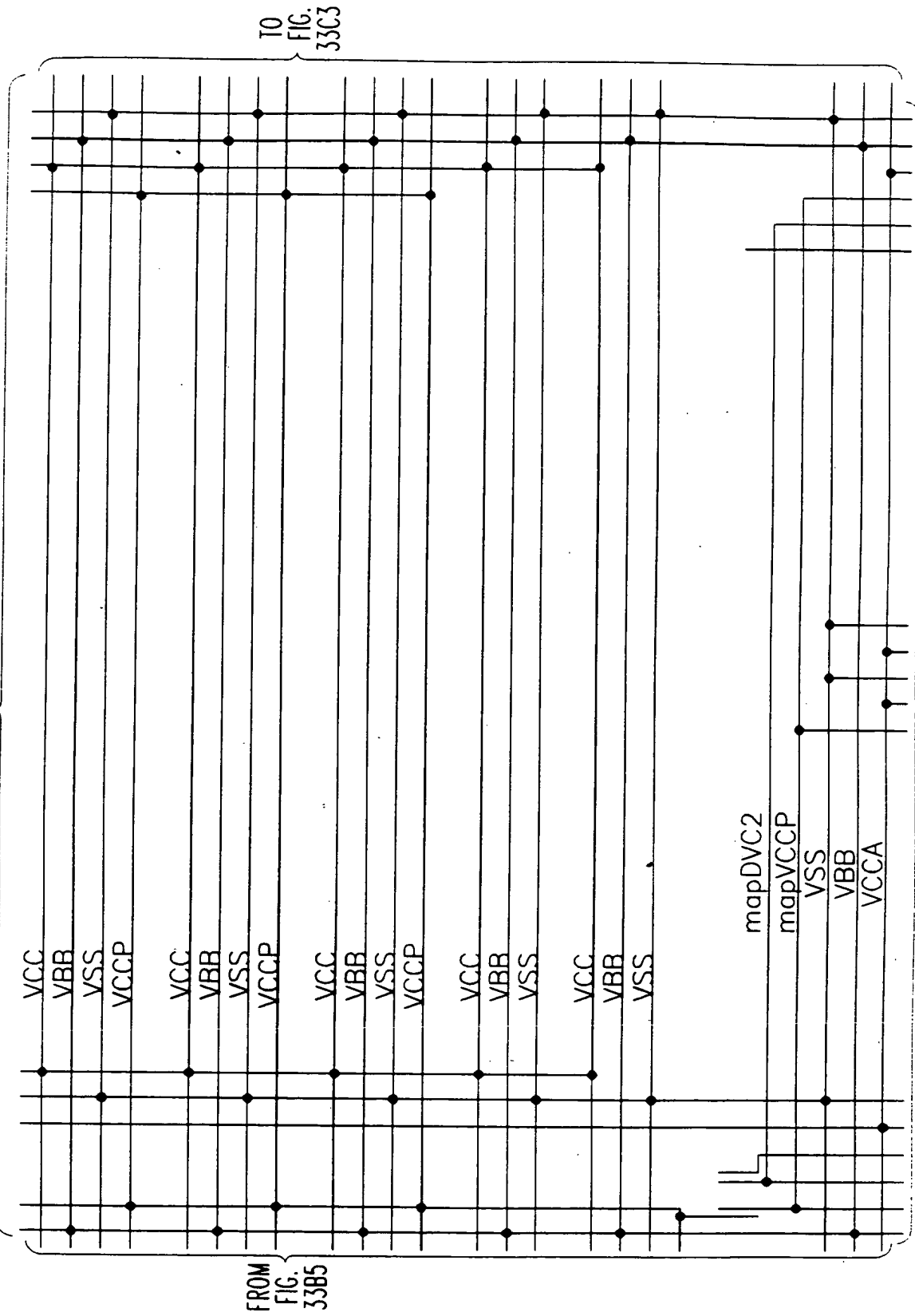


TO FIG. 33B7

FIG. 33B5

FIG. 33B4

FROM FIG. 33B4



TO FIG. 33B6

FIG. 33B6

FROM FIG. 33B5

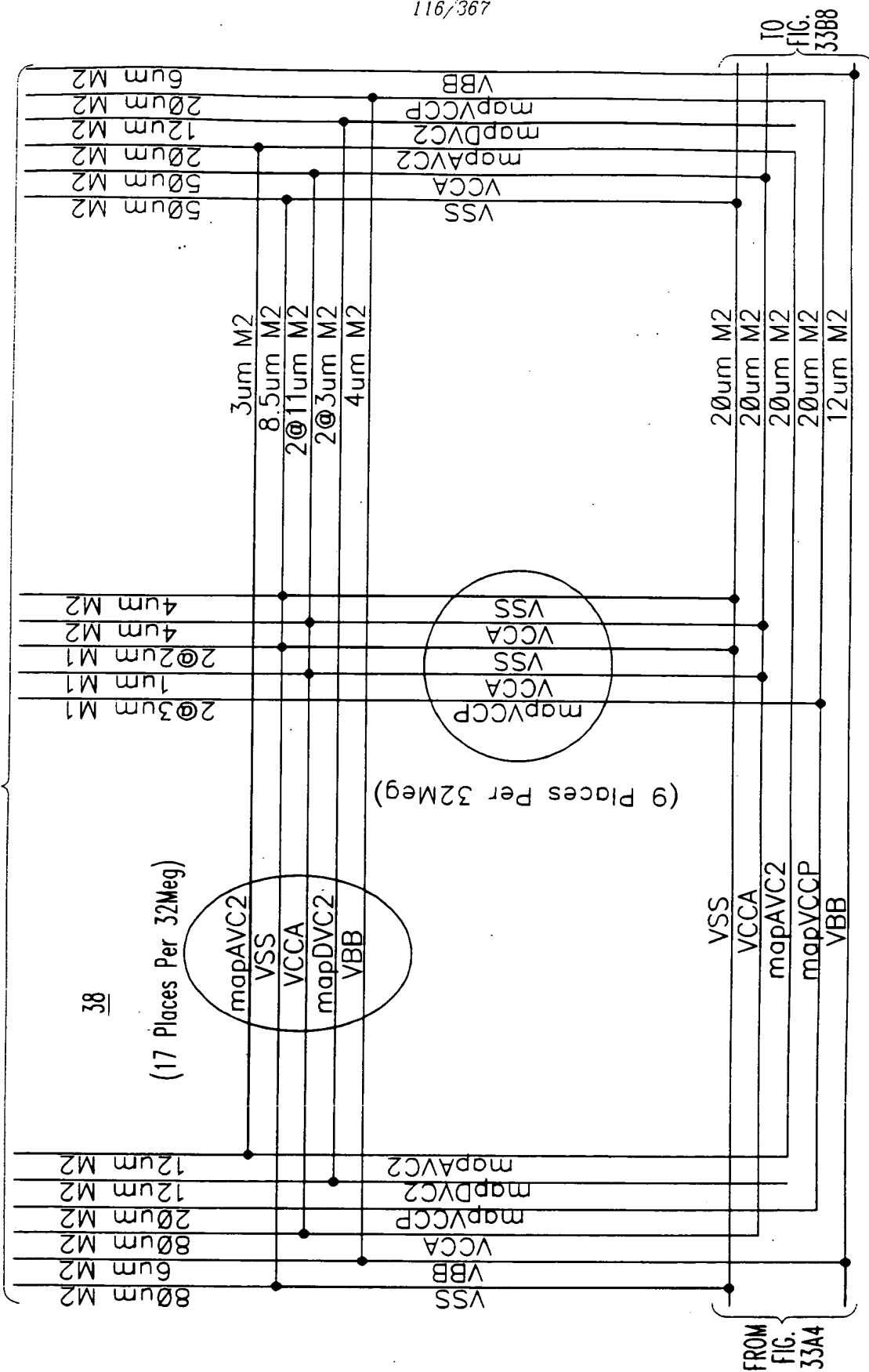


FIG. 33B7

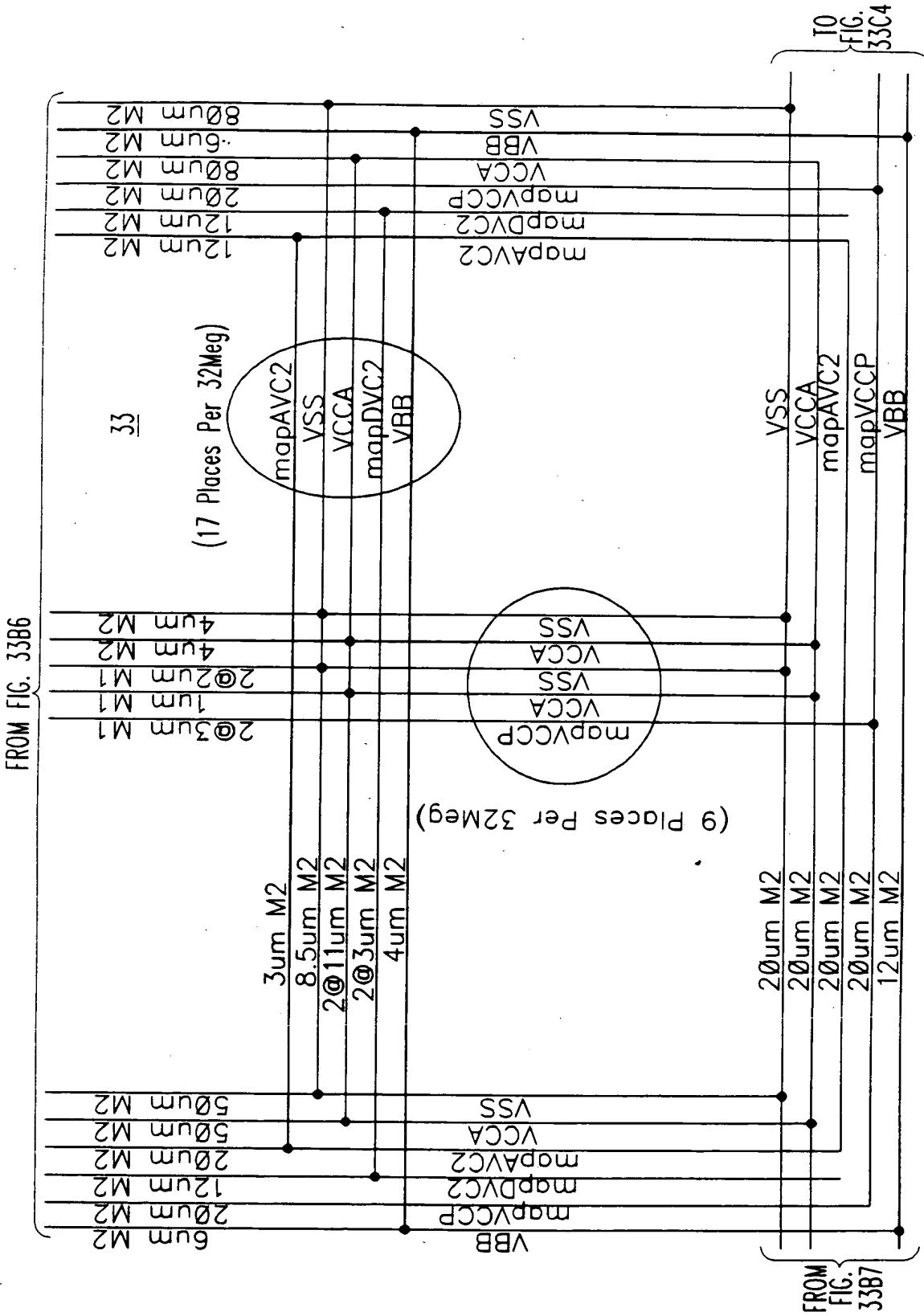
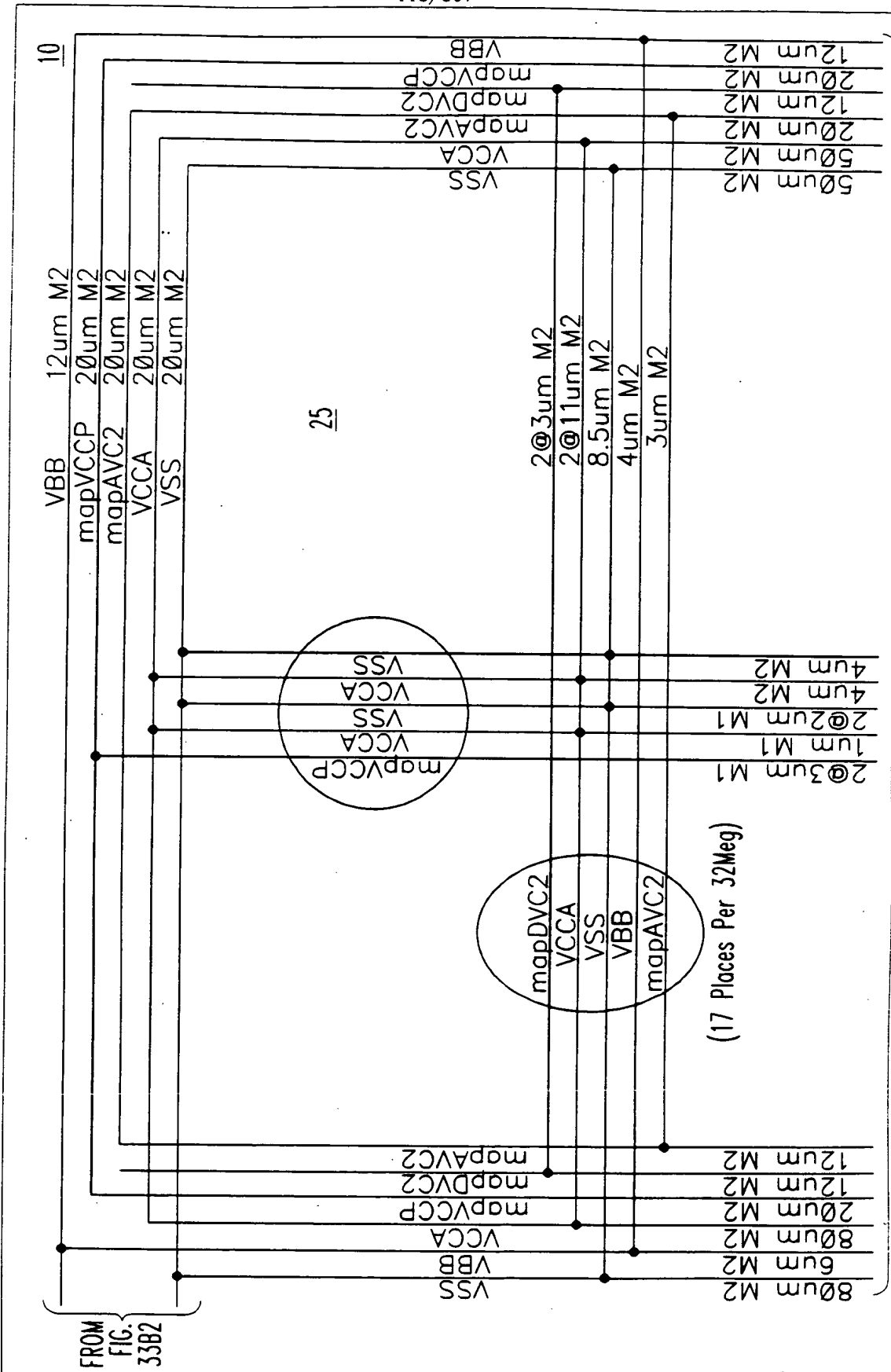


FIG. 33B8



TO FIG. 33C2

FIG. 33C1

FROM
FIG.
33B3



FIG. 33C2

FROM FIG. 33C2

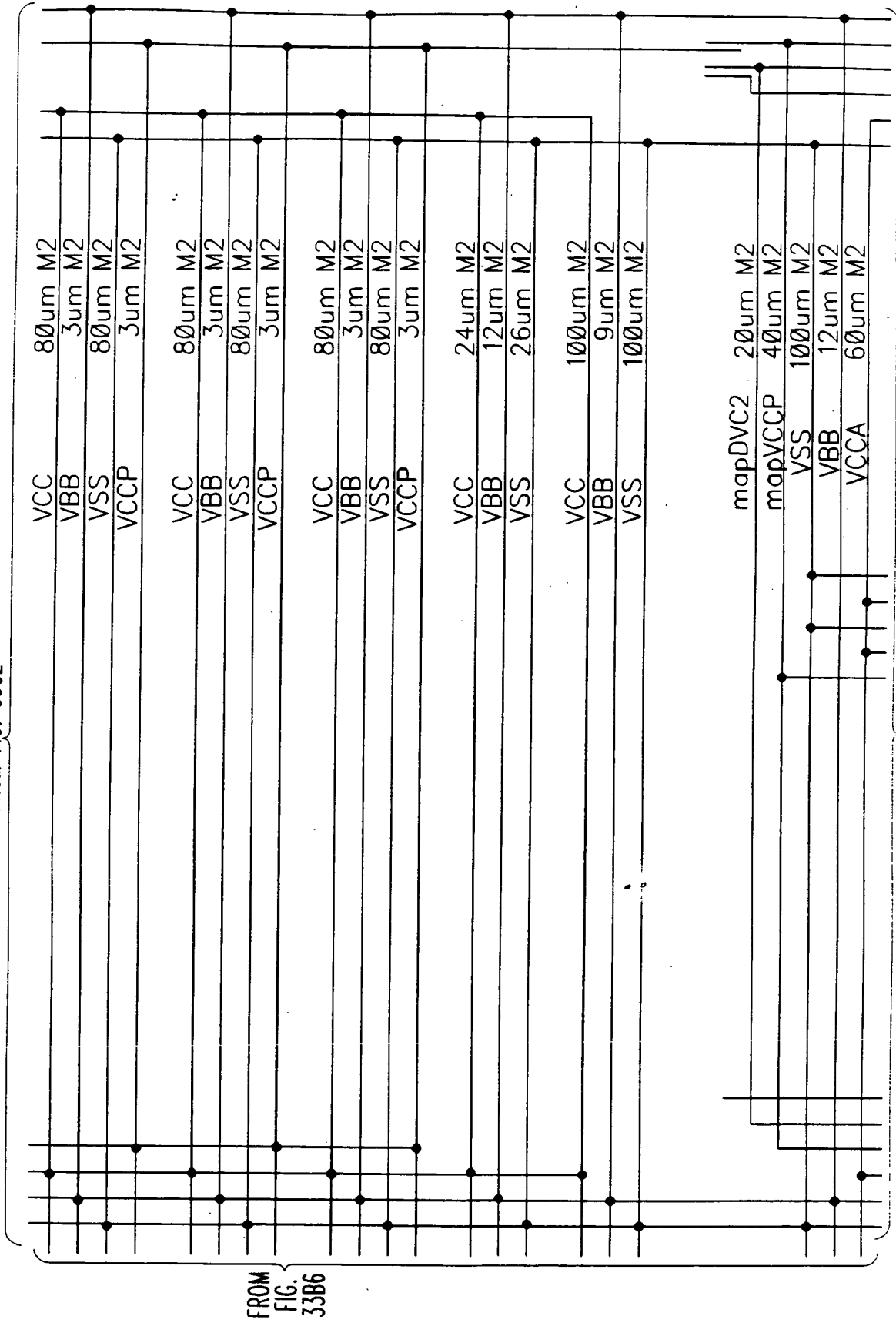
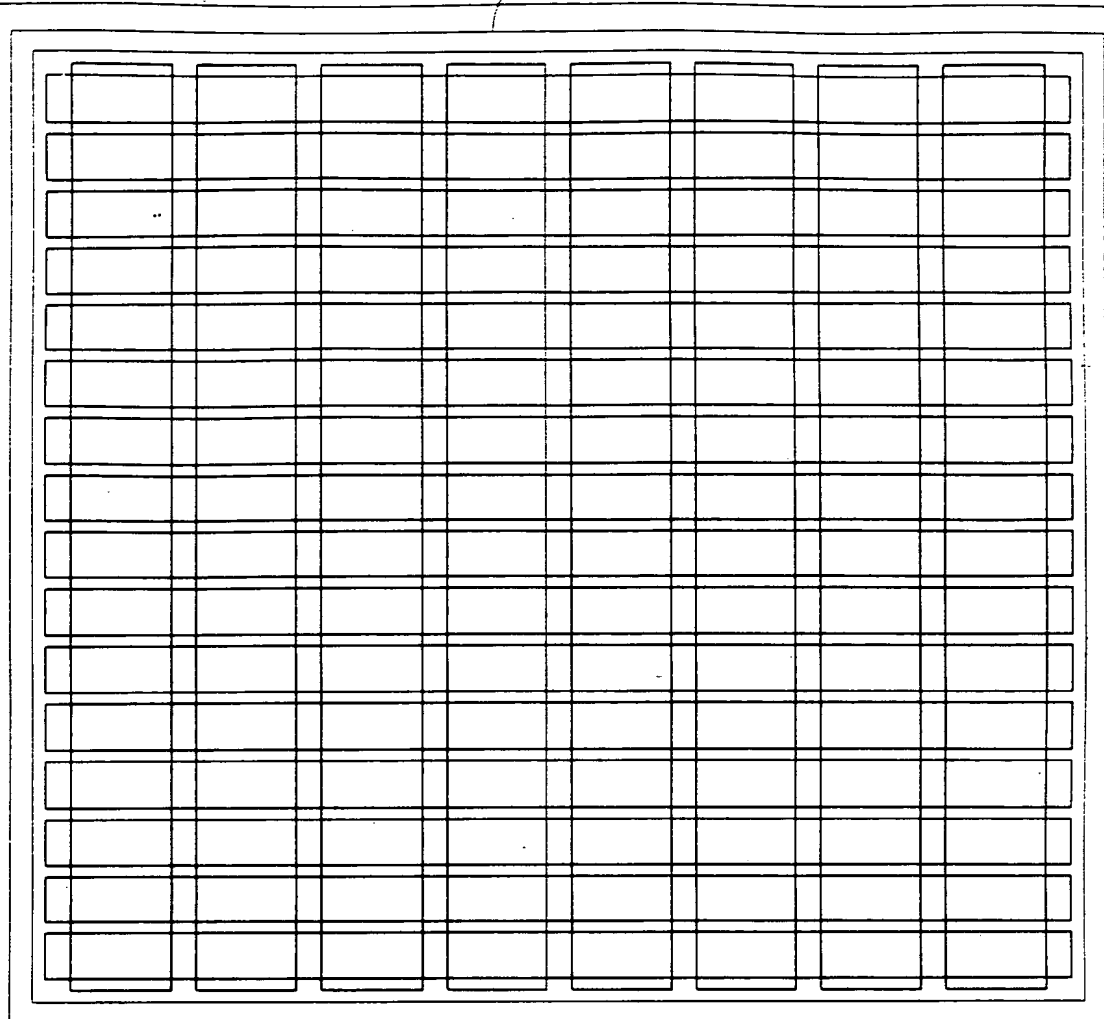


FIG. 33C3

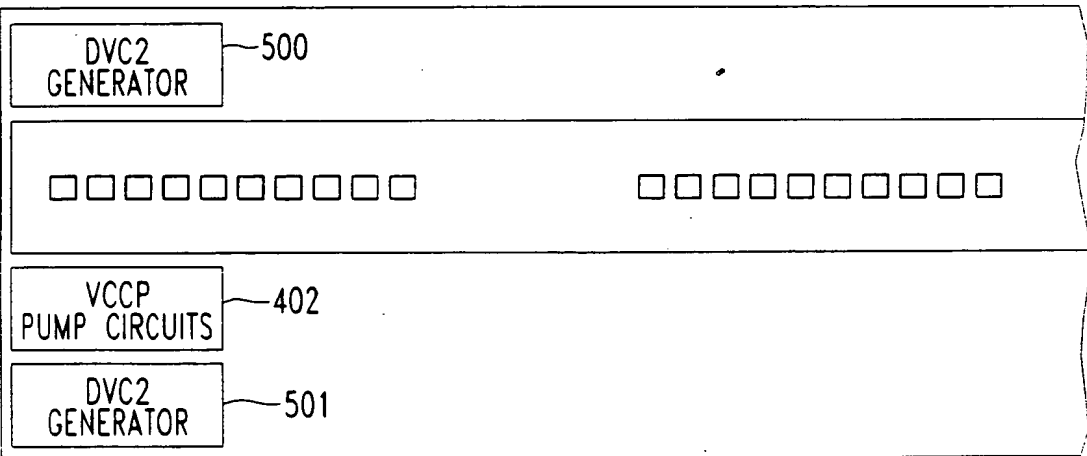
FIG. 33C4

10

45



200



TO FIG. 33D3

TO FIG. 33D2

FIG. 33D1

TO FIG. 33D1

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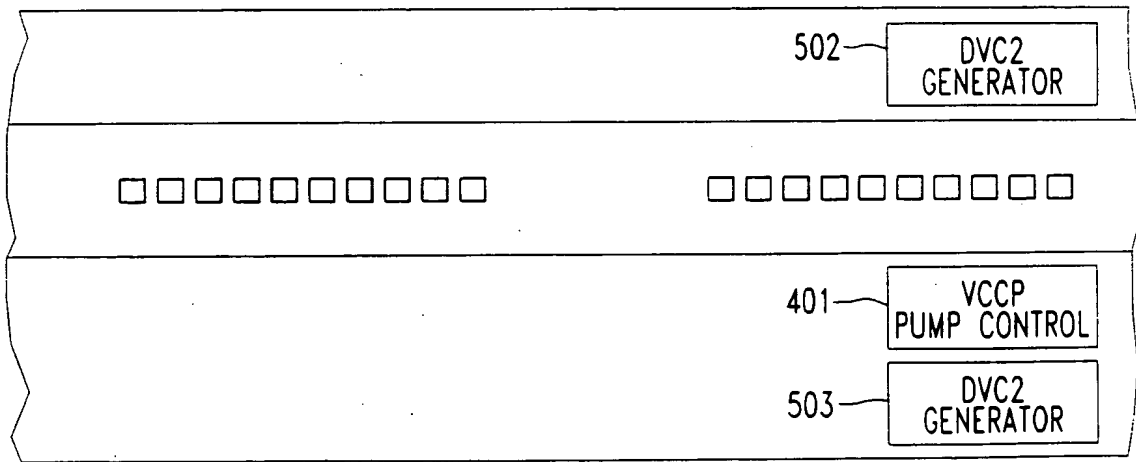
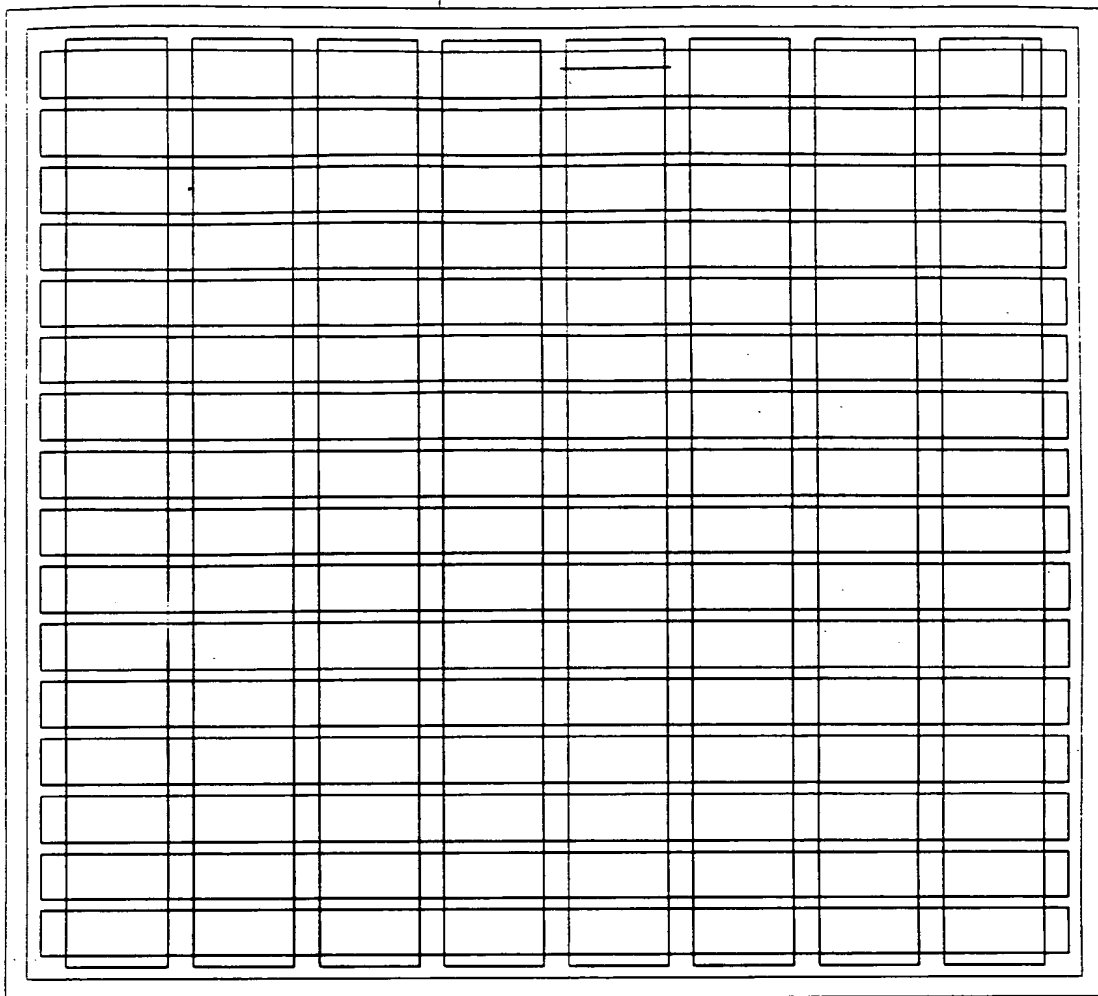
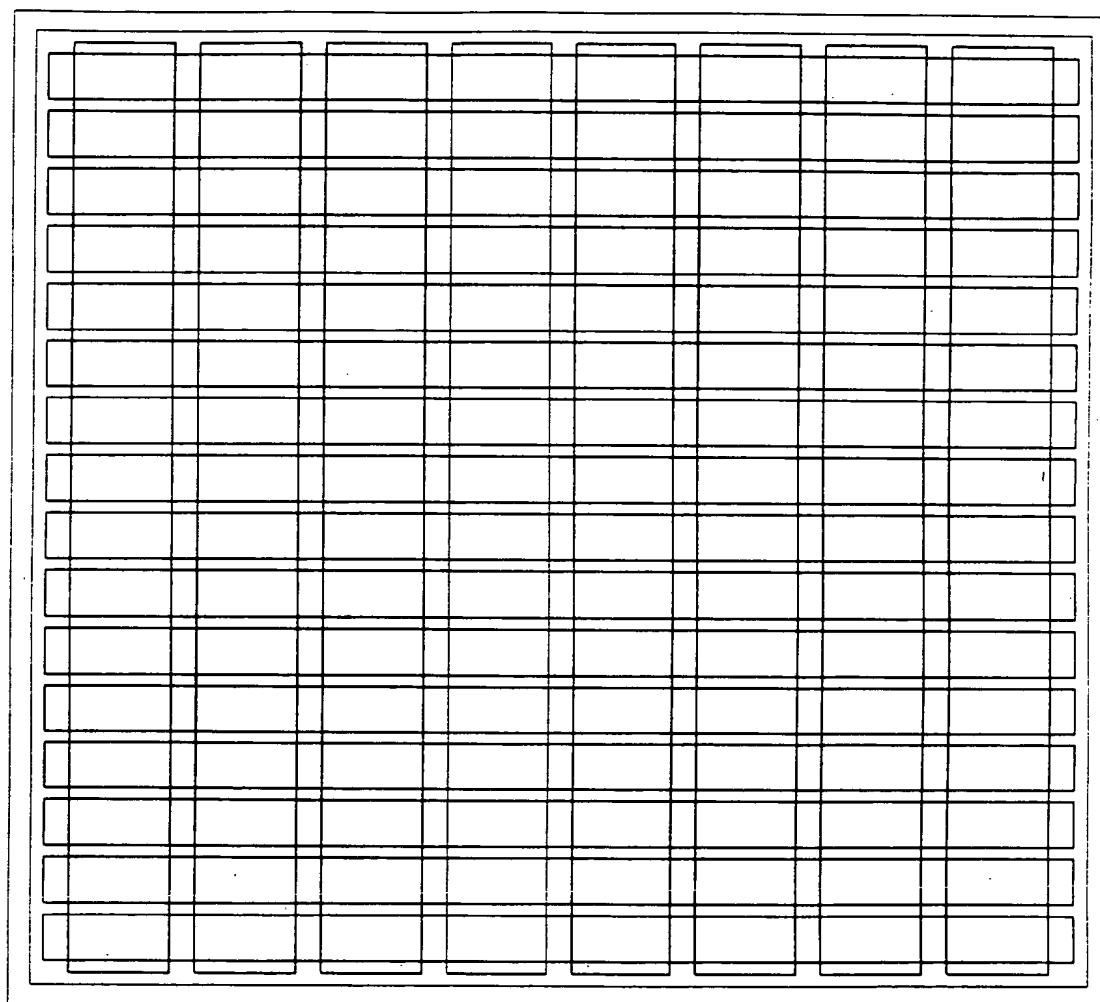


FIG. 33D2

TO
FIG.
33D4

TO
FIG.
33D1

(SEE FIG. 33E1)



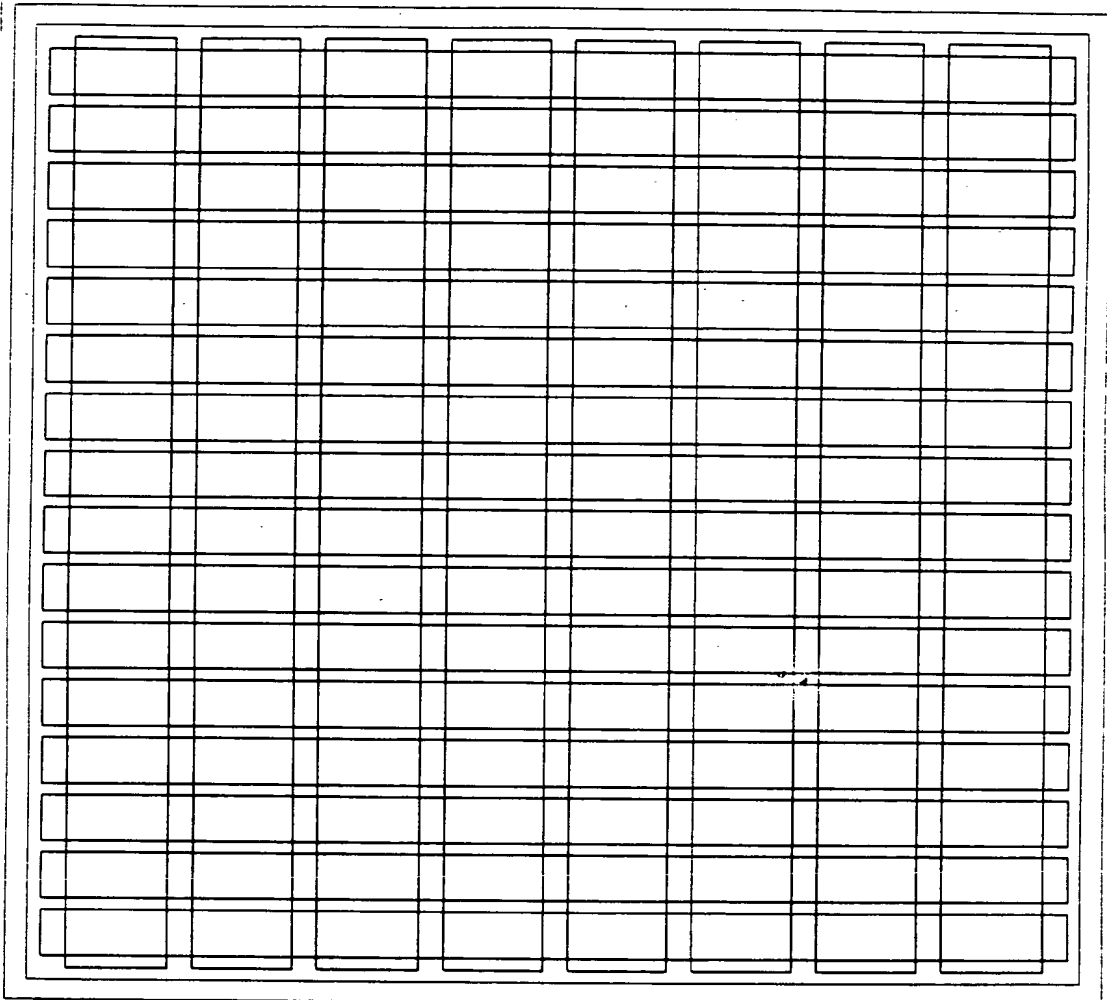
38

TO FIG. 33D4

FIG. 33D3

00034795-082204
TOP280-56/43000

TO
FIG.
33D2



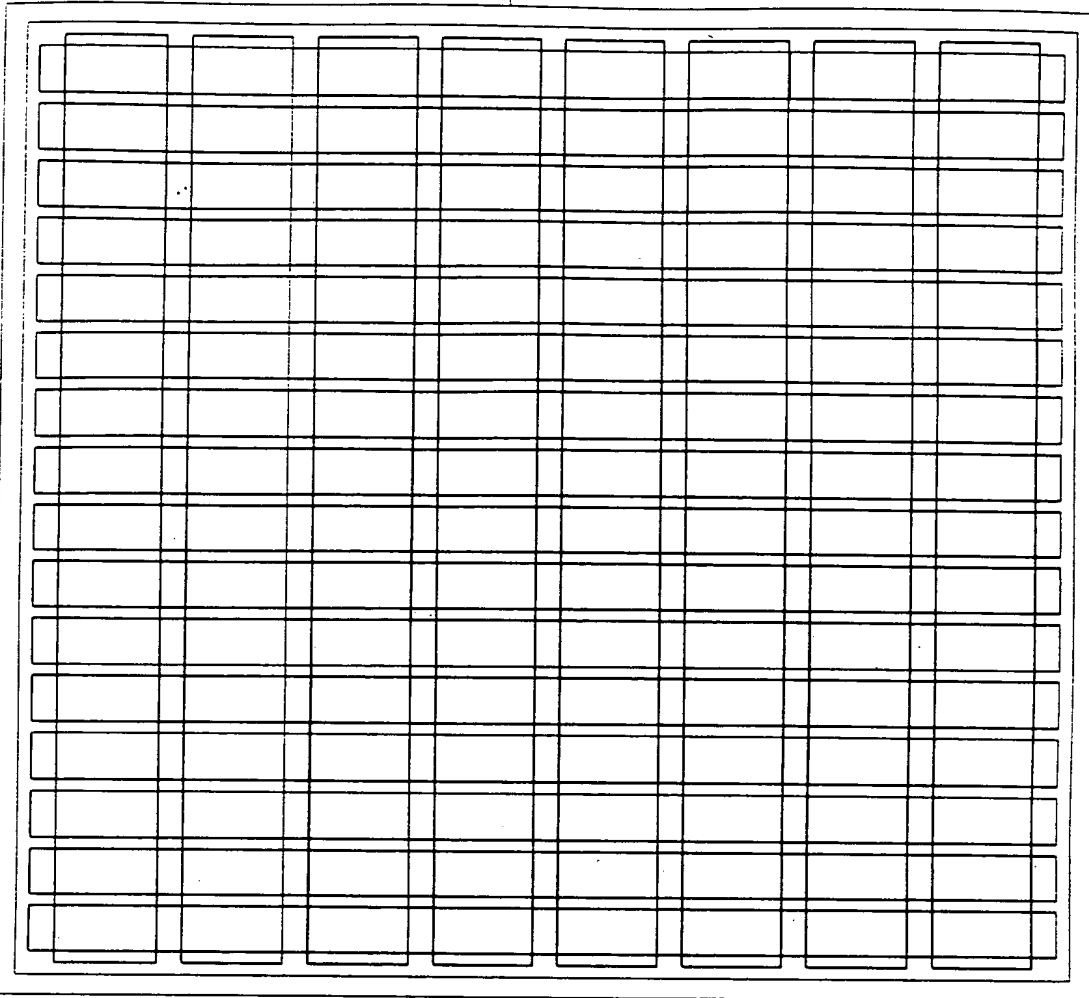
TO FIG. 33D3

FIG. 33D4

(SEE FIG. 33D2)

25

TO FIG. 33E2



DVC2
GENERATOR 504

□ □ □ □ □ □ □ □ □ □

□ □ □ □ □ □ □ □ □ □

VCCP
REGULATOR 220

DVC2
GENERATOR 505

TO
FIG.
33E3

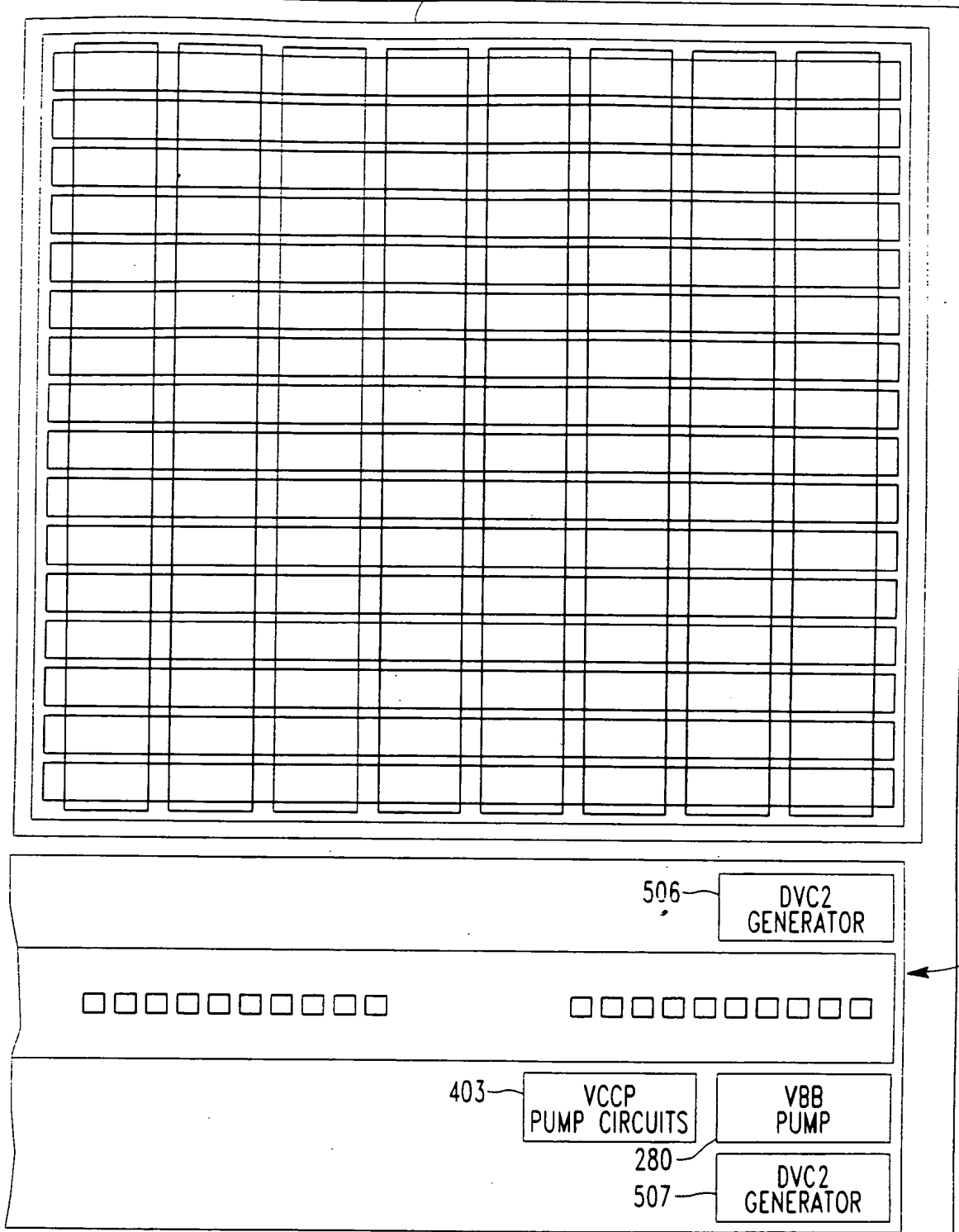
FIG. 33E1

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TO FIG. 33E1

27

10



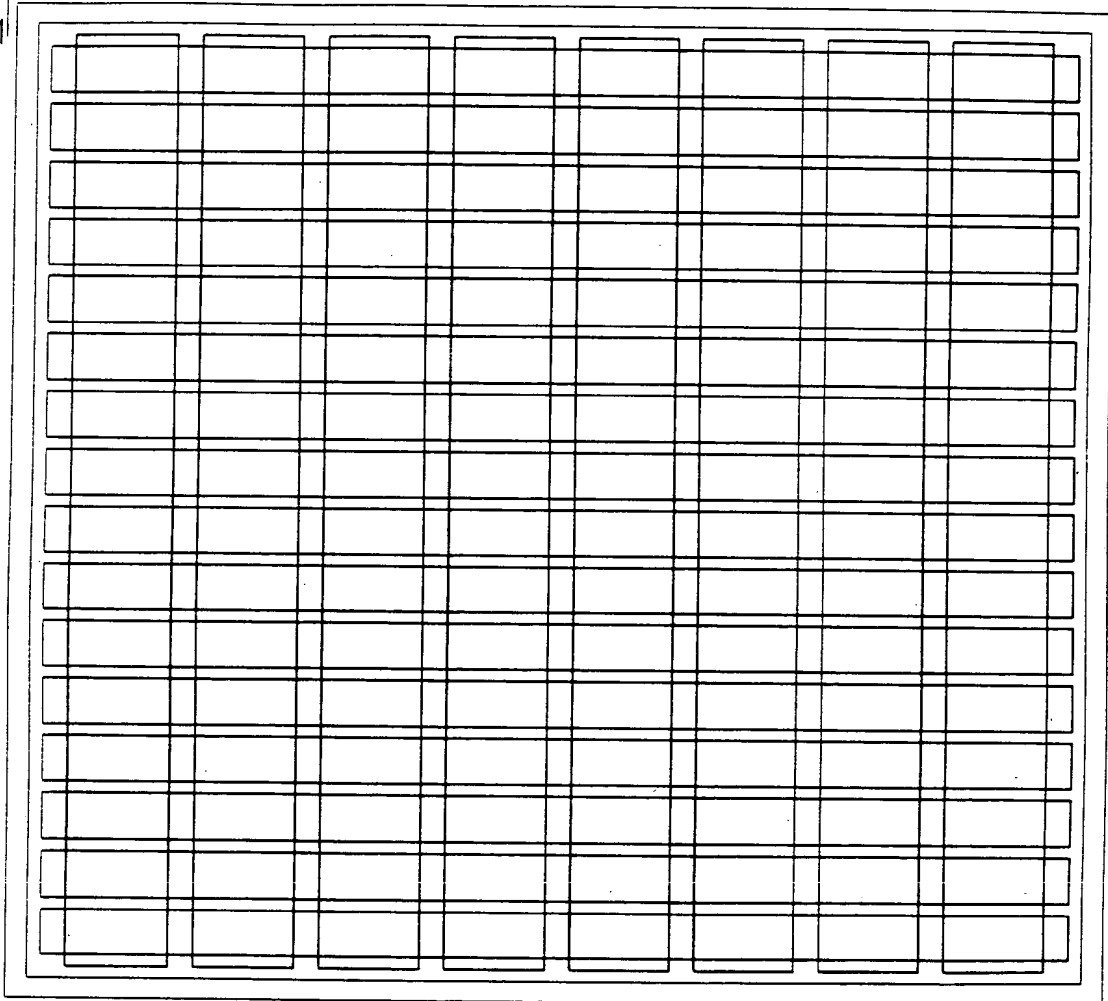
200

FIG. 33E2

TO
FIG.
33E4

FIG. 33E3

TO
FIG.
33E1

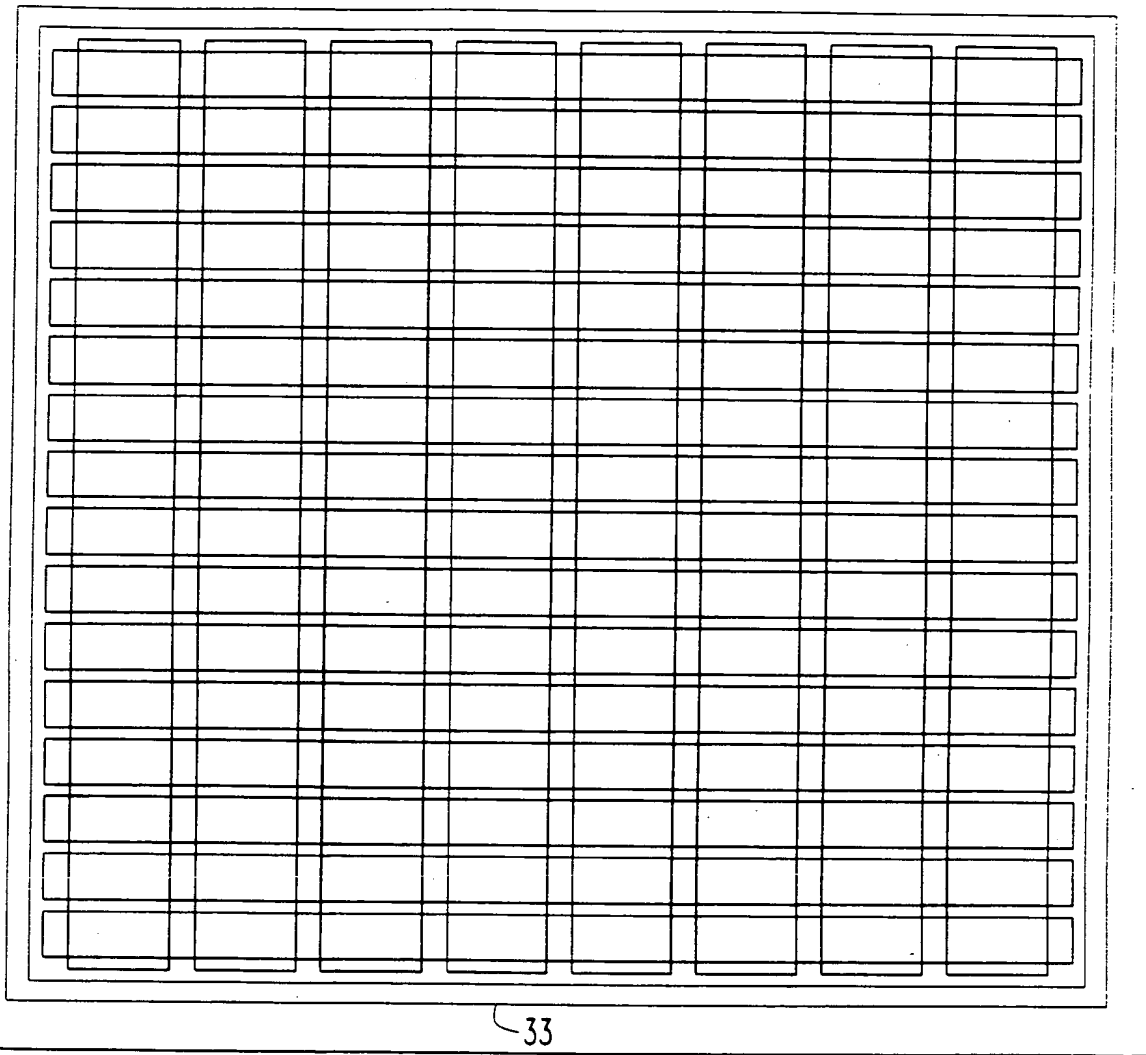


31

FIG. 33E3

TO FIG. 33E4

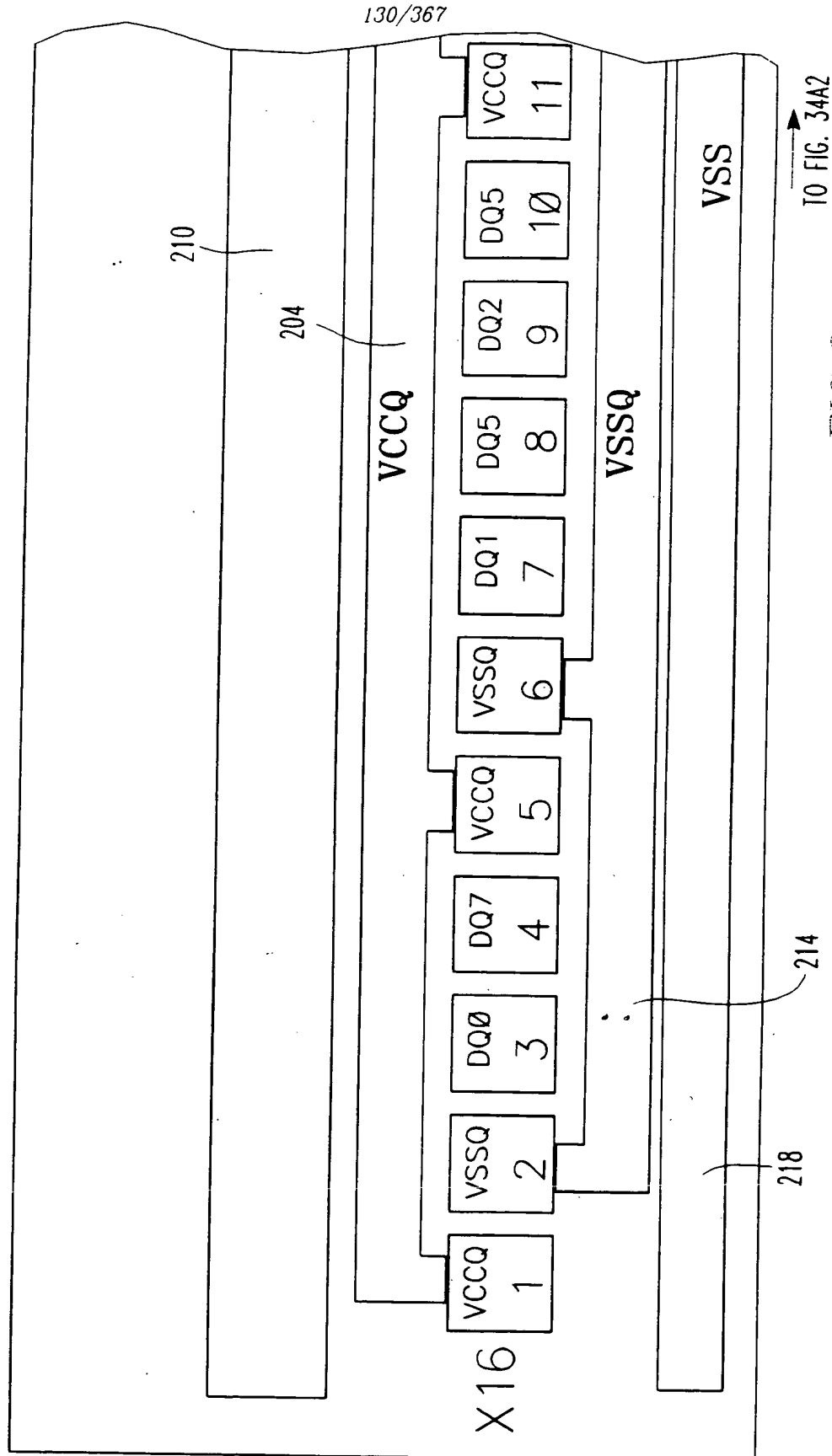
00034755-08201
T02200-56/4E600



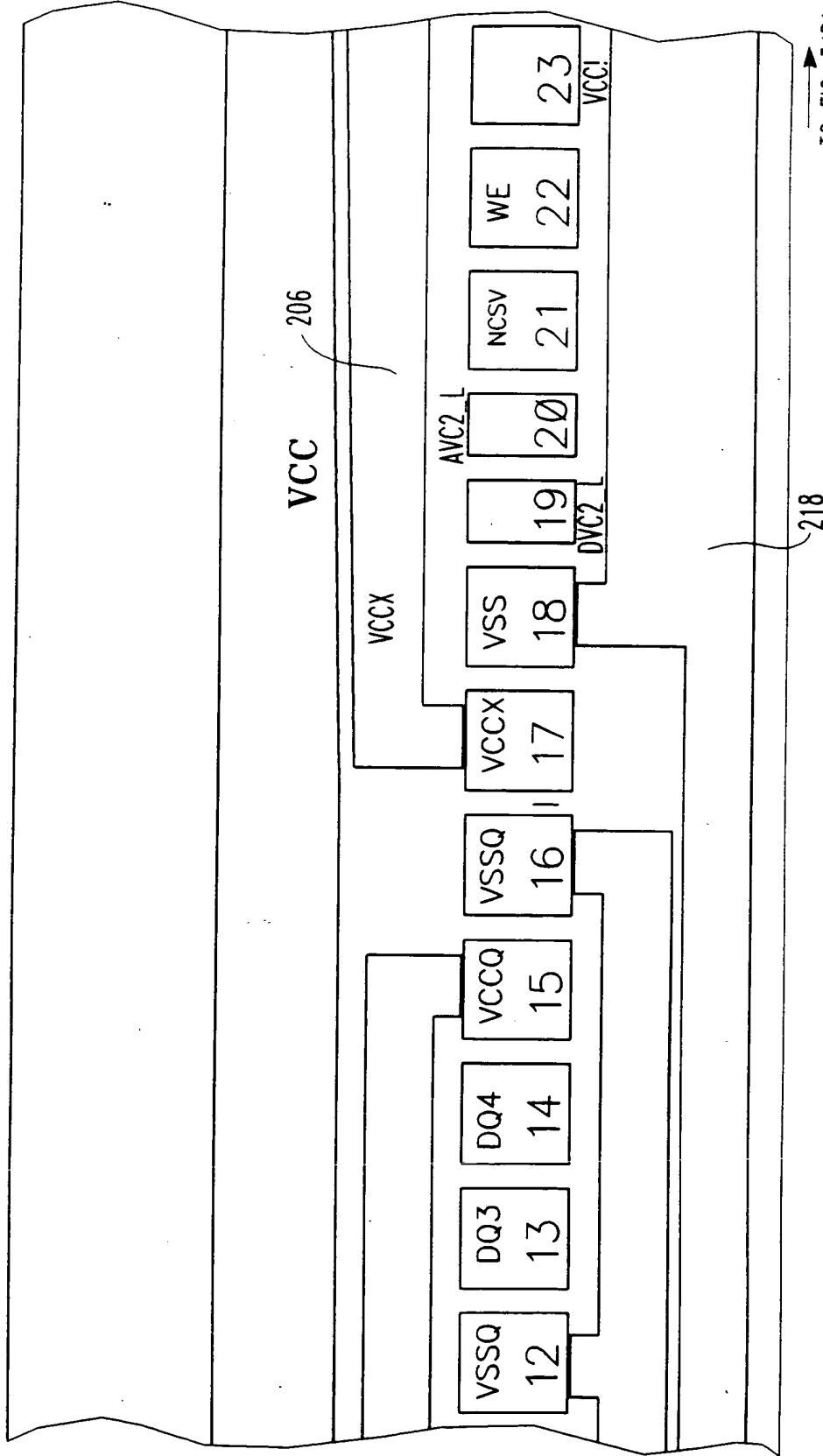
TO FIG. 33E3

FIG. 33E4

TO
FIG.
33E2



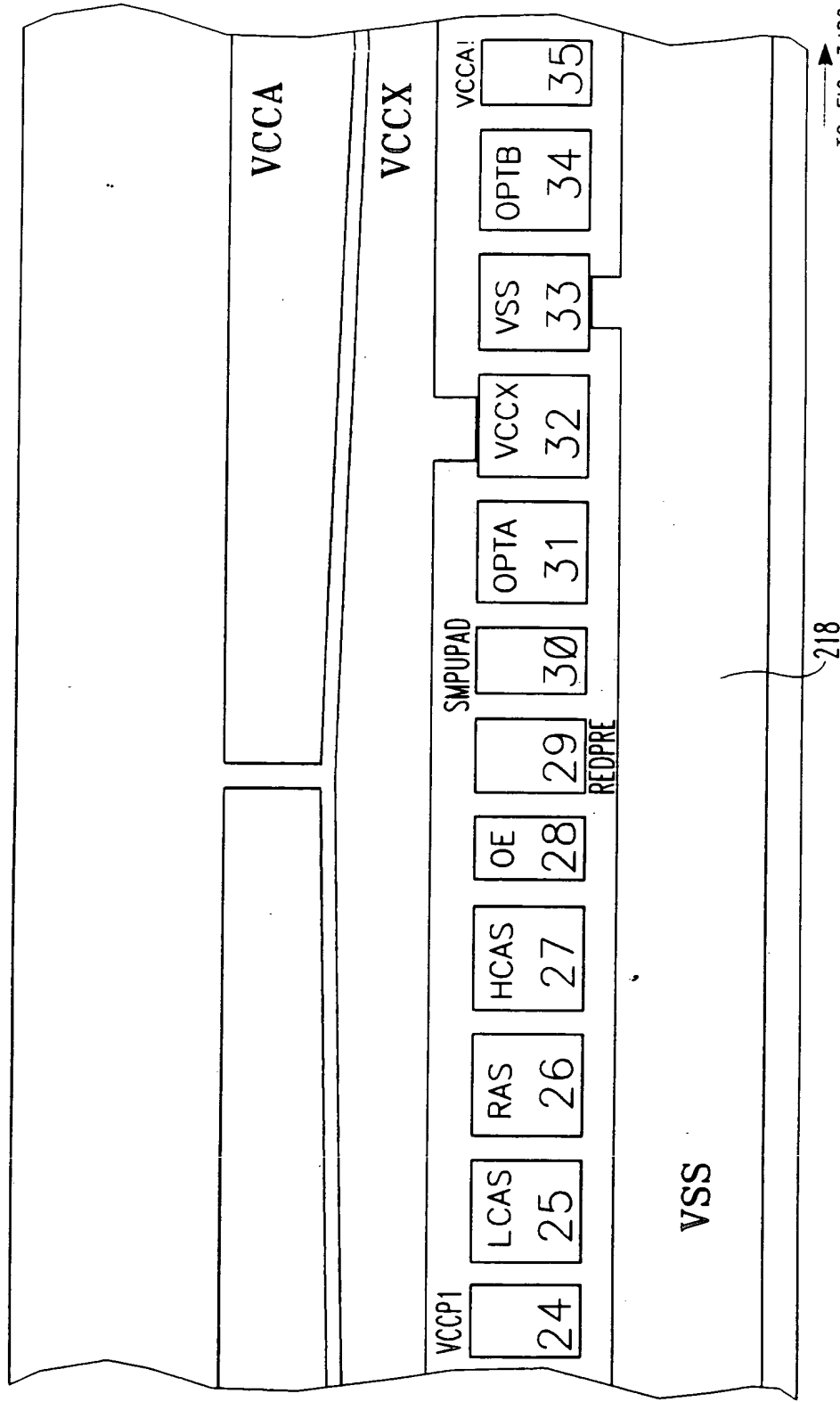
TO FIG. 34A1



TO FIG. 34B1

FIG. 34A2

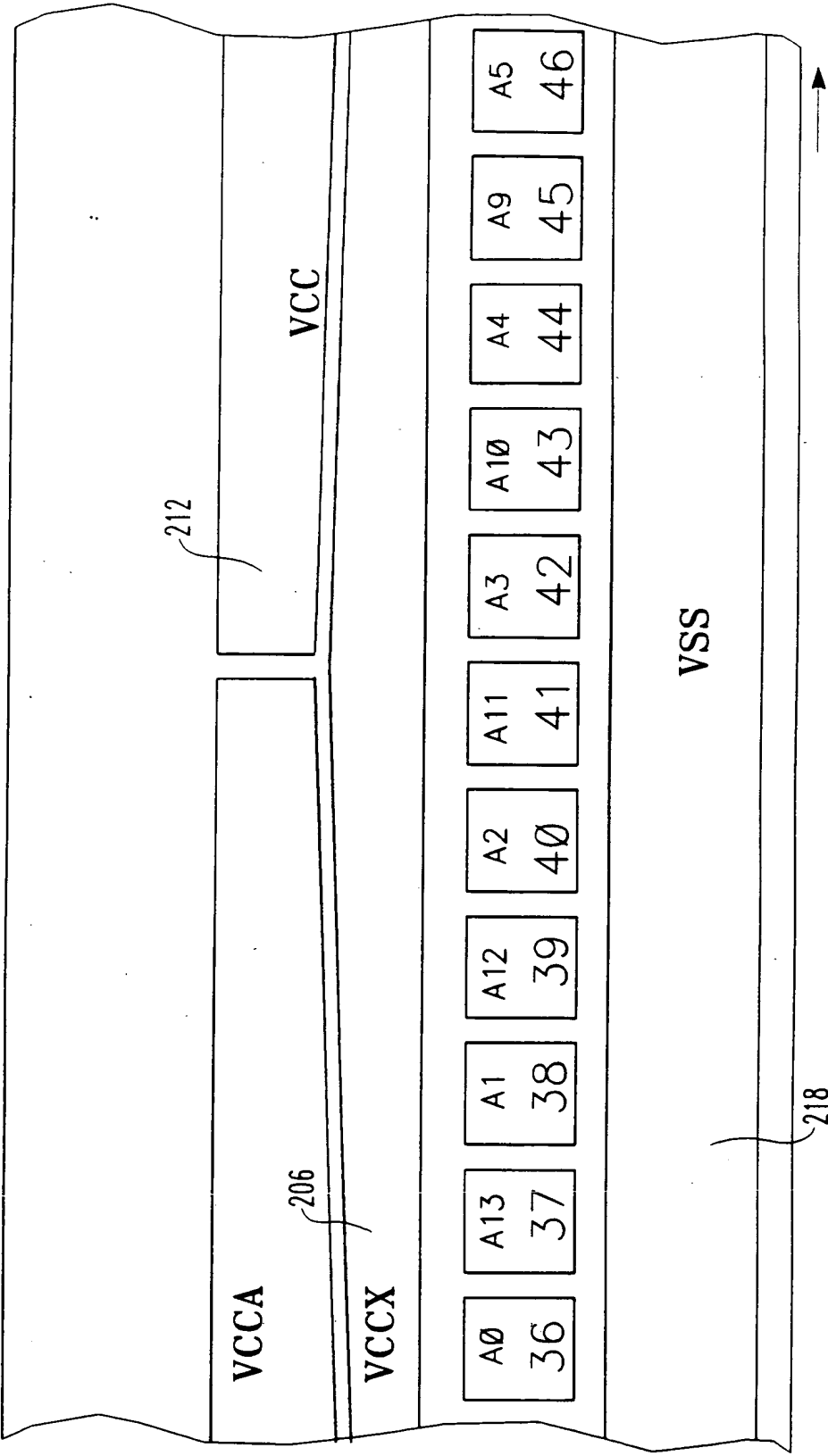
TO FIG. 34A2



TO FIG. 34B2

FIG. 34B1

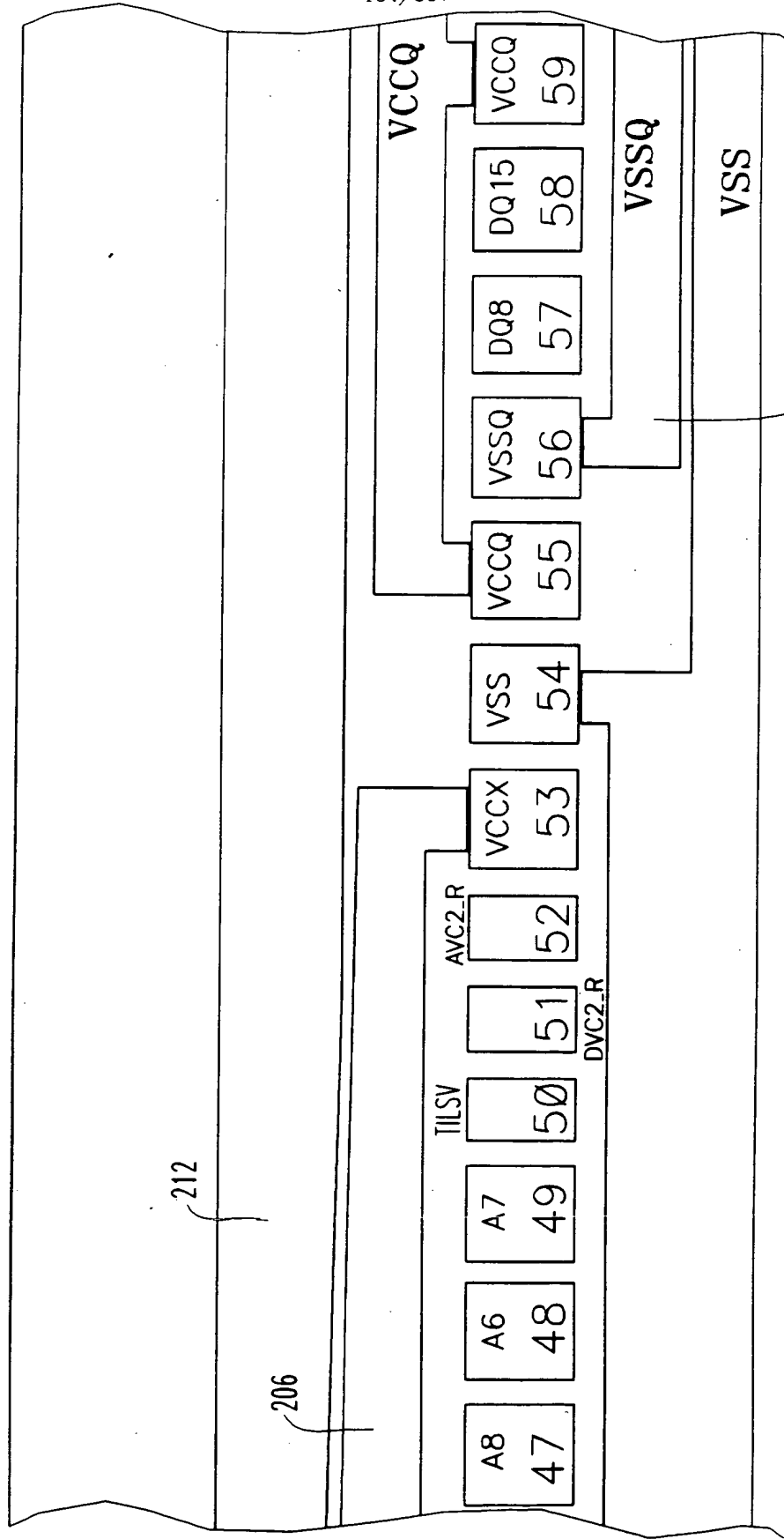
TO FIG. 34B1



TO FIG. 34C1

FIG. 34B2

TO FIG. 34B2



TO FIG. 34C2

TO FIG. 34C1

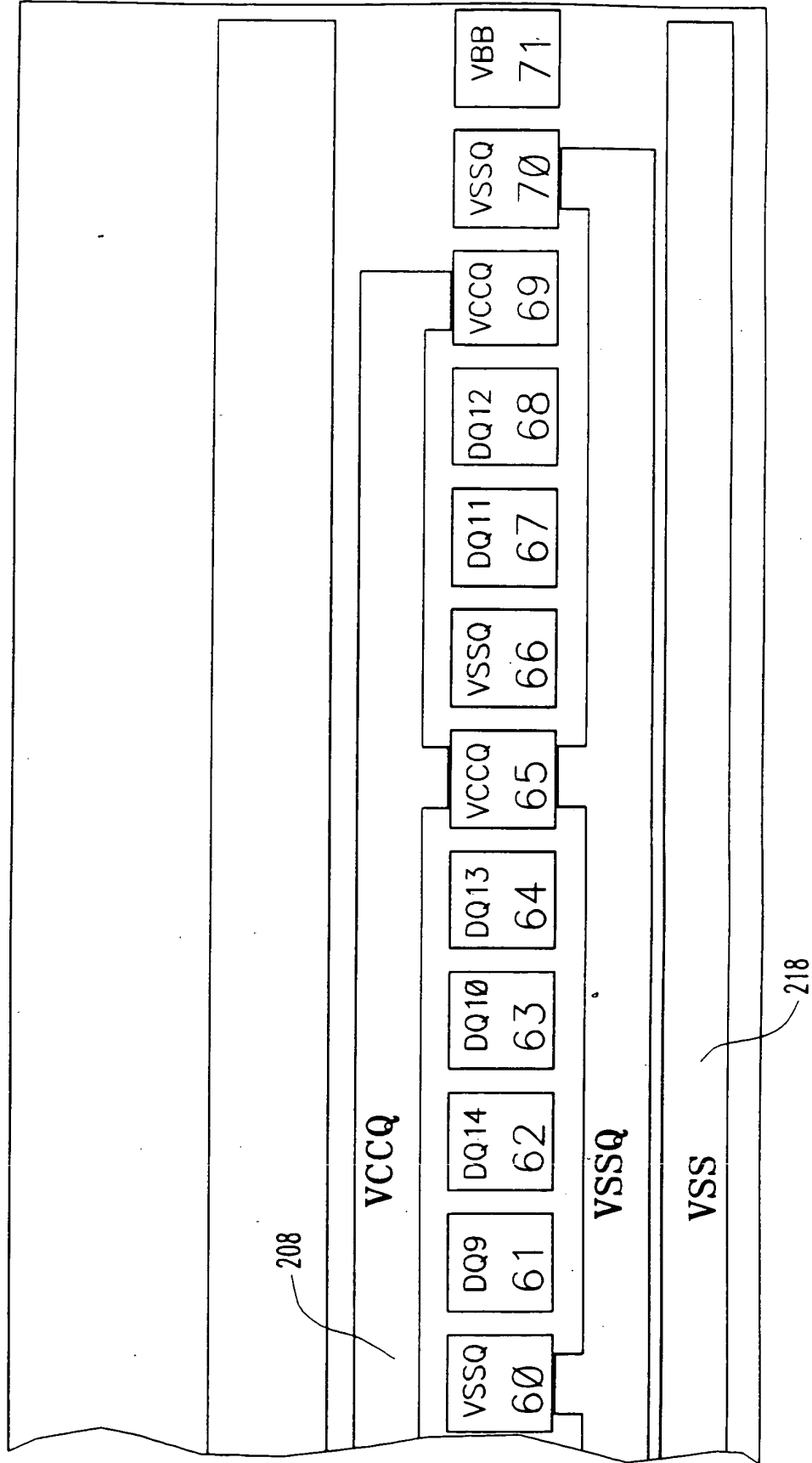


FIG. 34C2

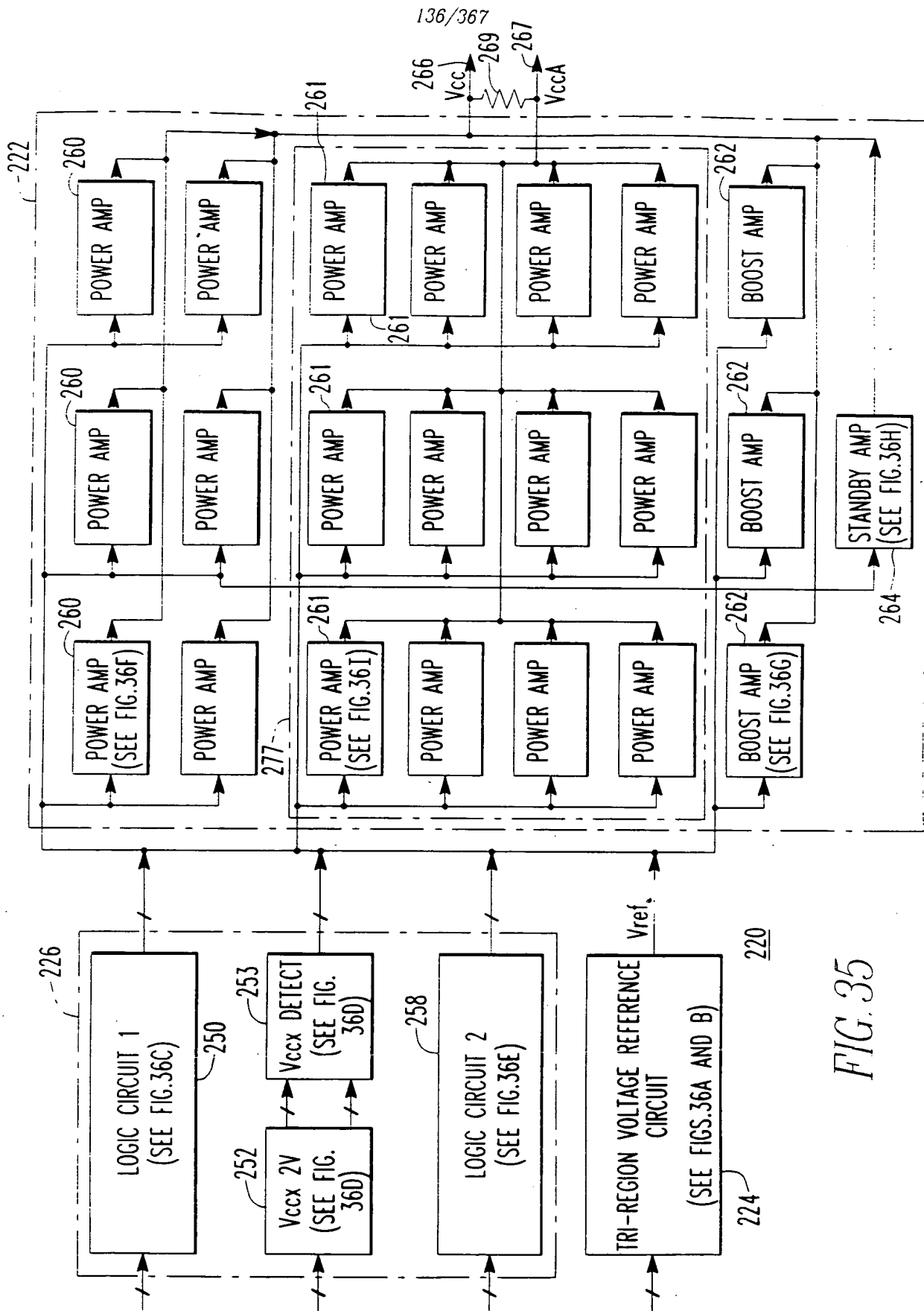


FIG. 35

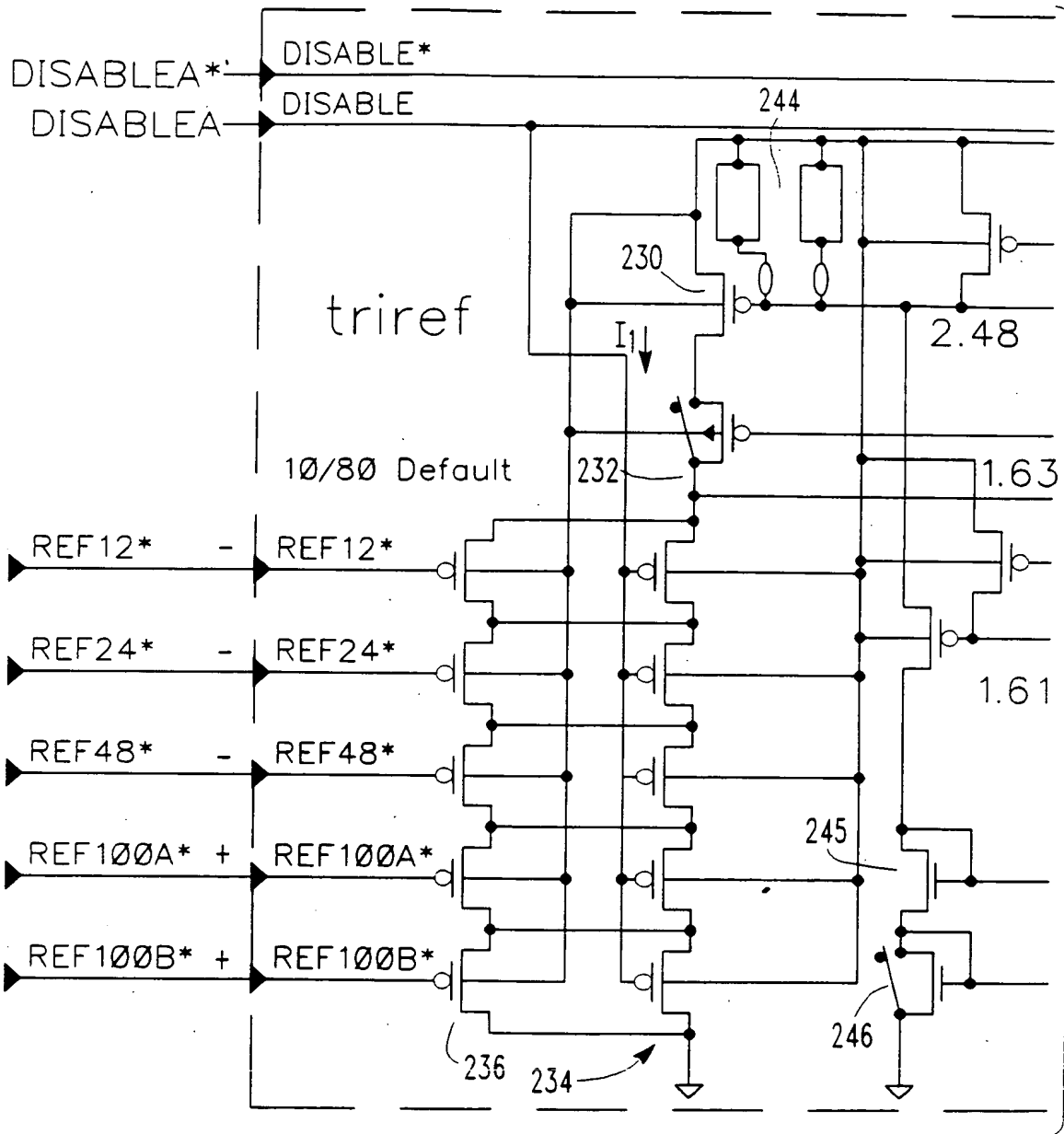
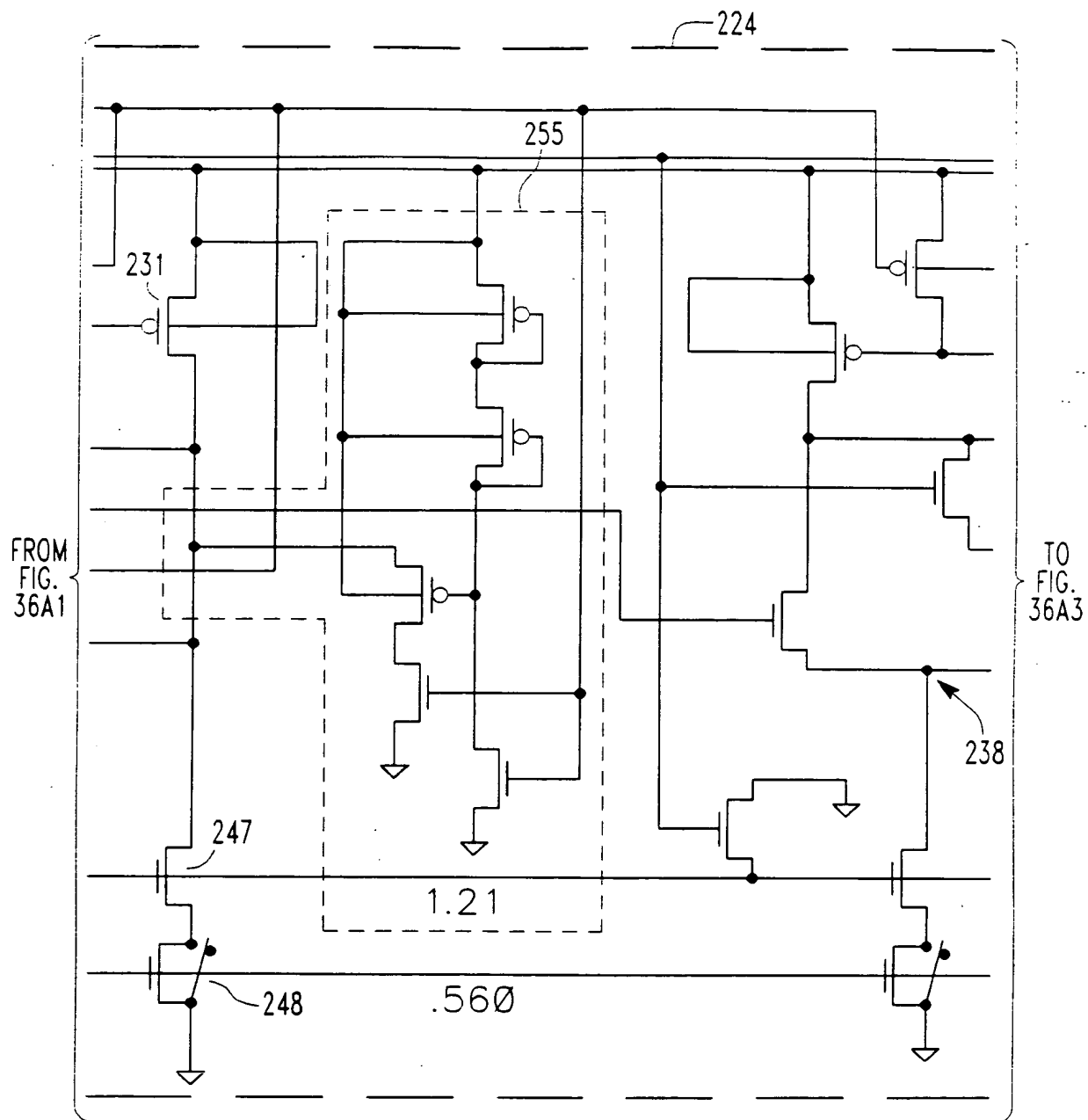
TO
FIG.
36A2

FIG. 36A1



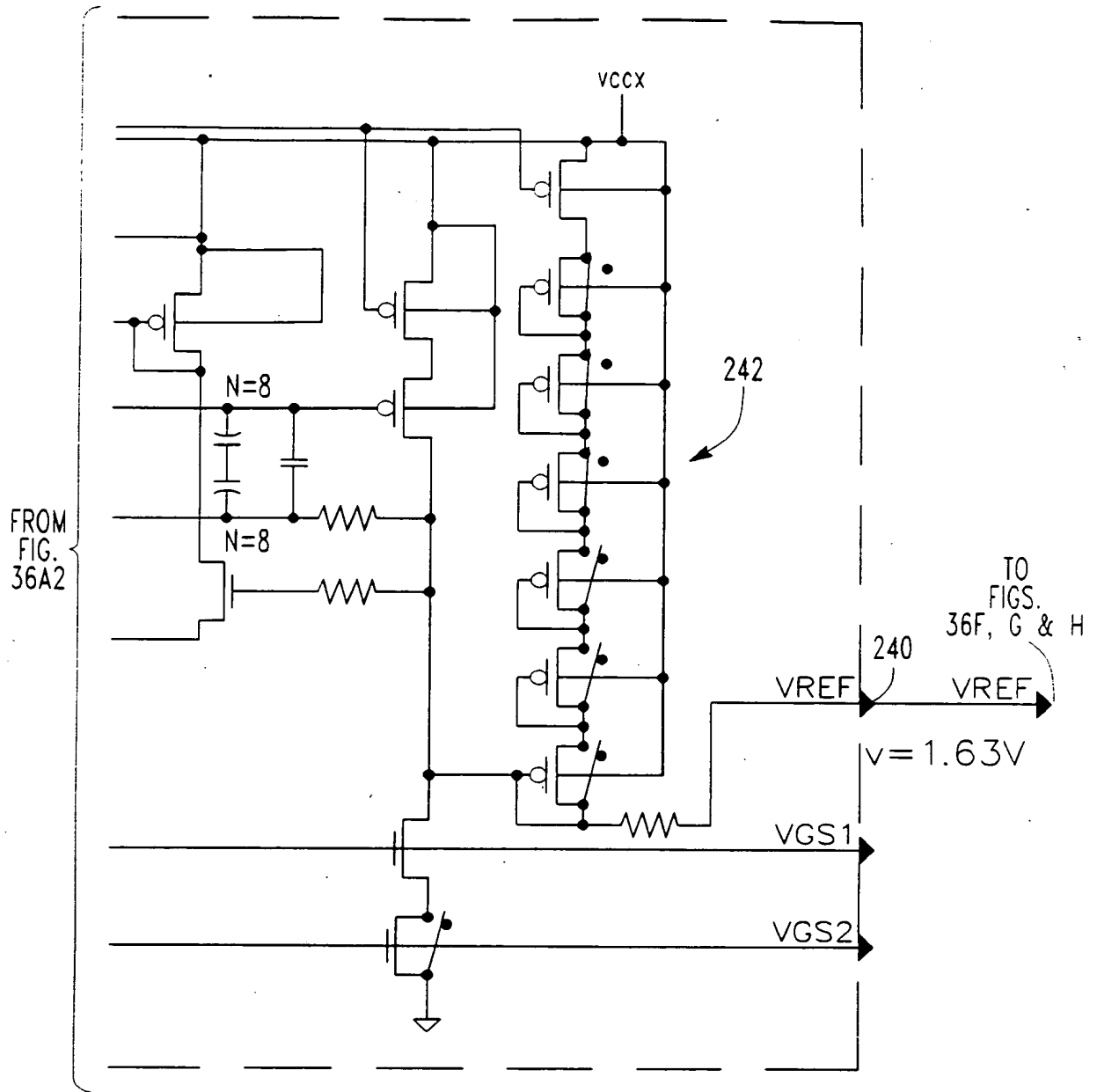


FIG. 36A3

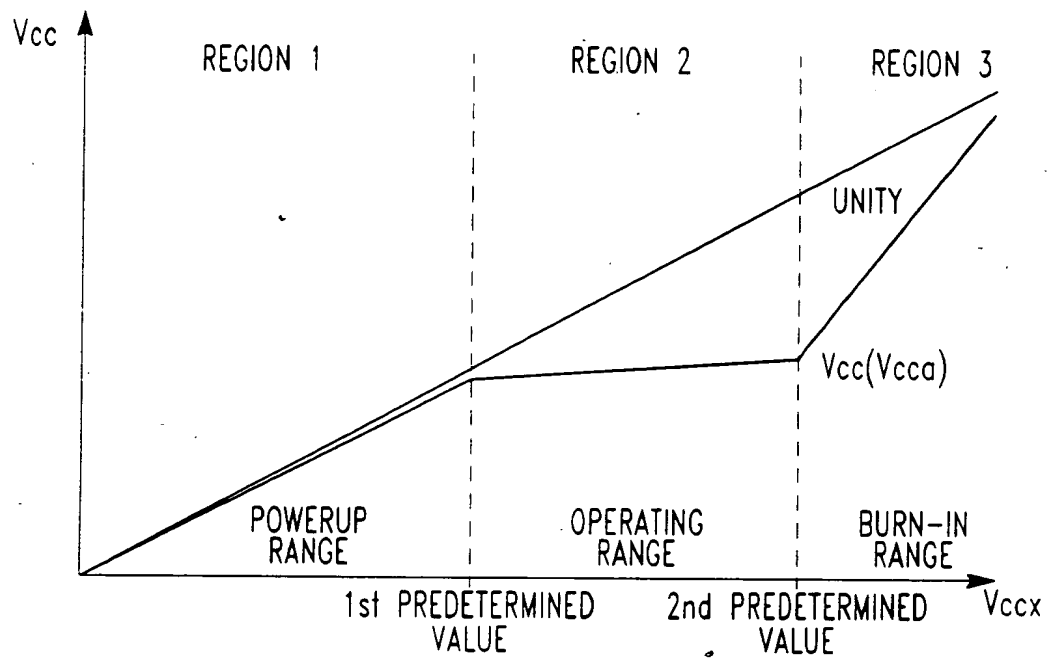


FIG. 36B

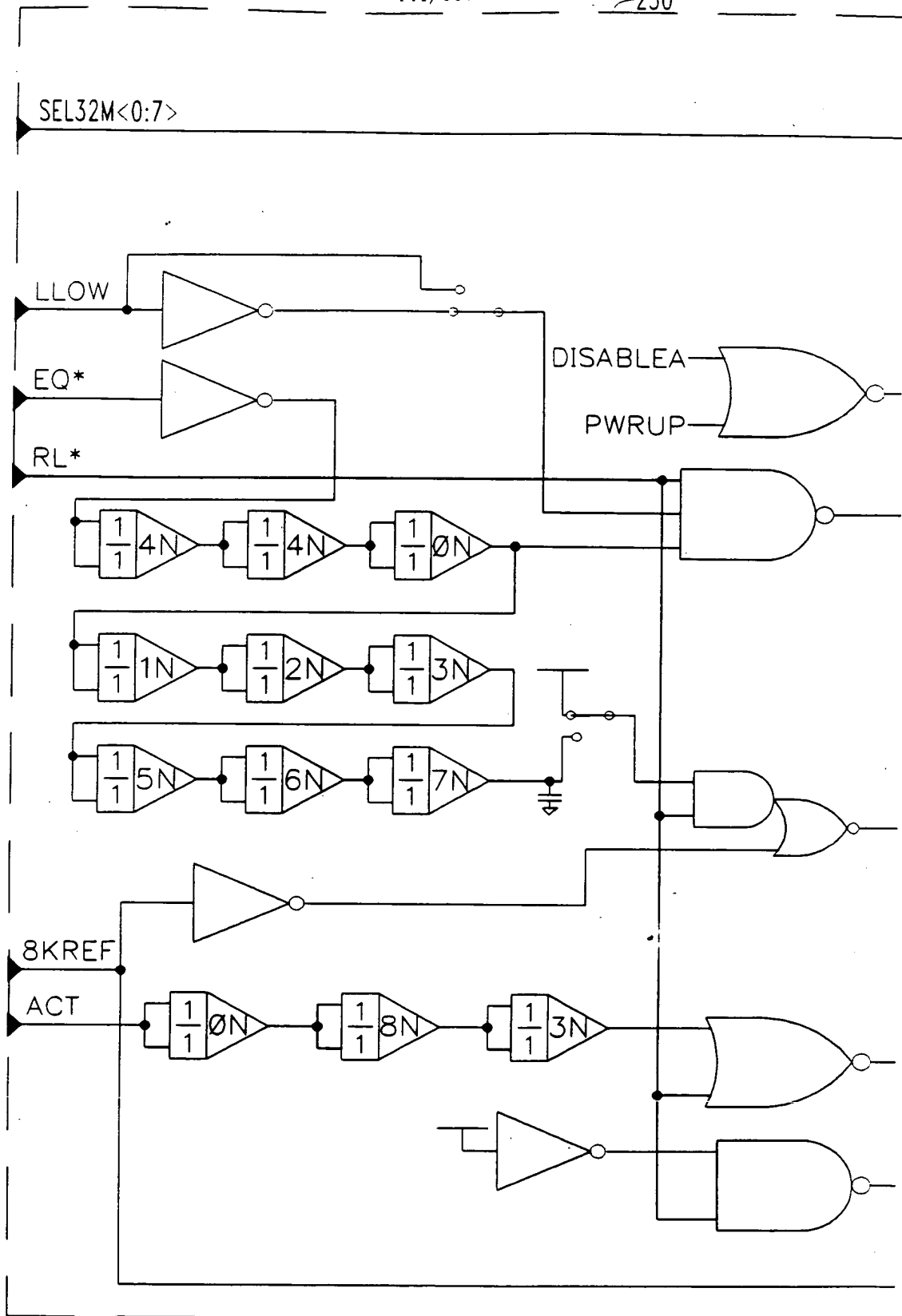


FIG. 36C1

0004795-00001

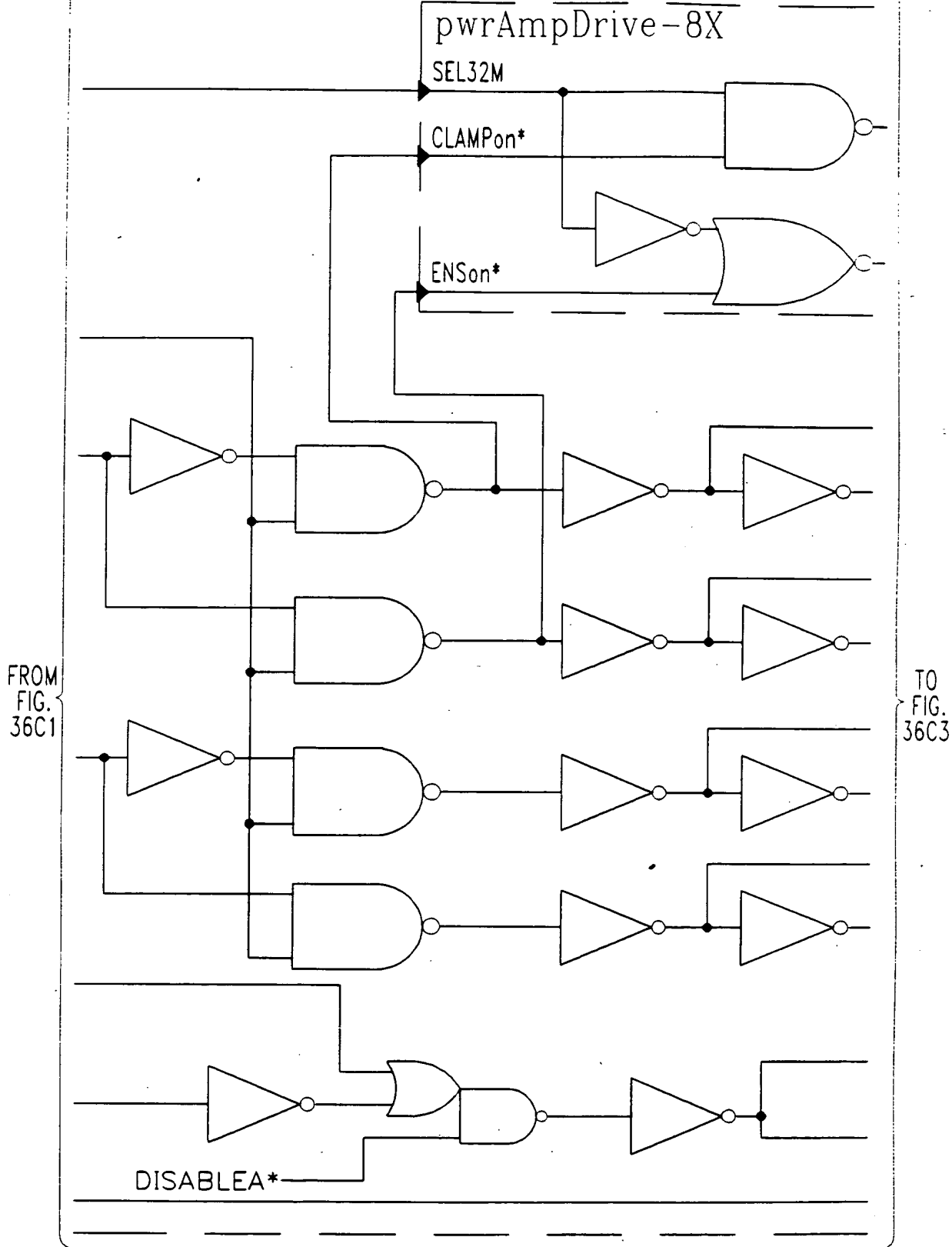


FIG. 36C2

FROM
FIG.
36C2

TO
FIG.
36F

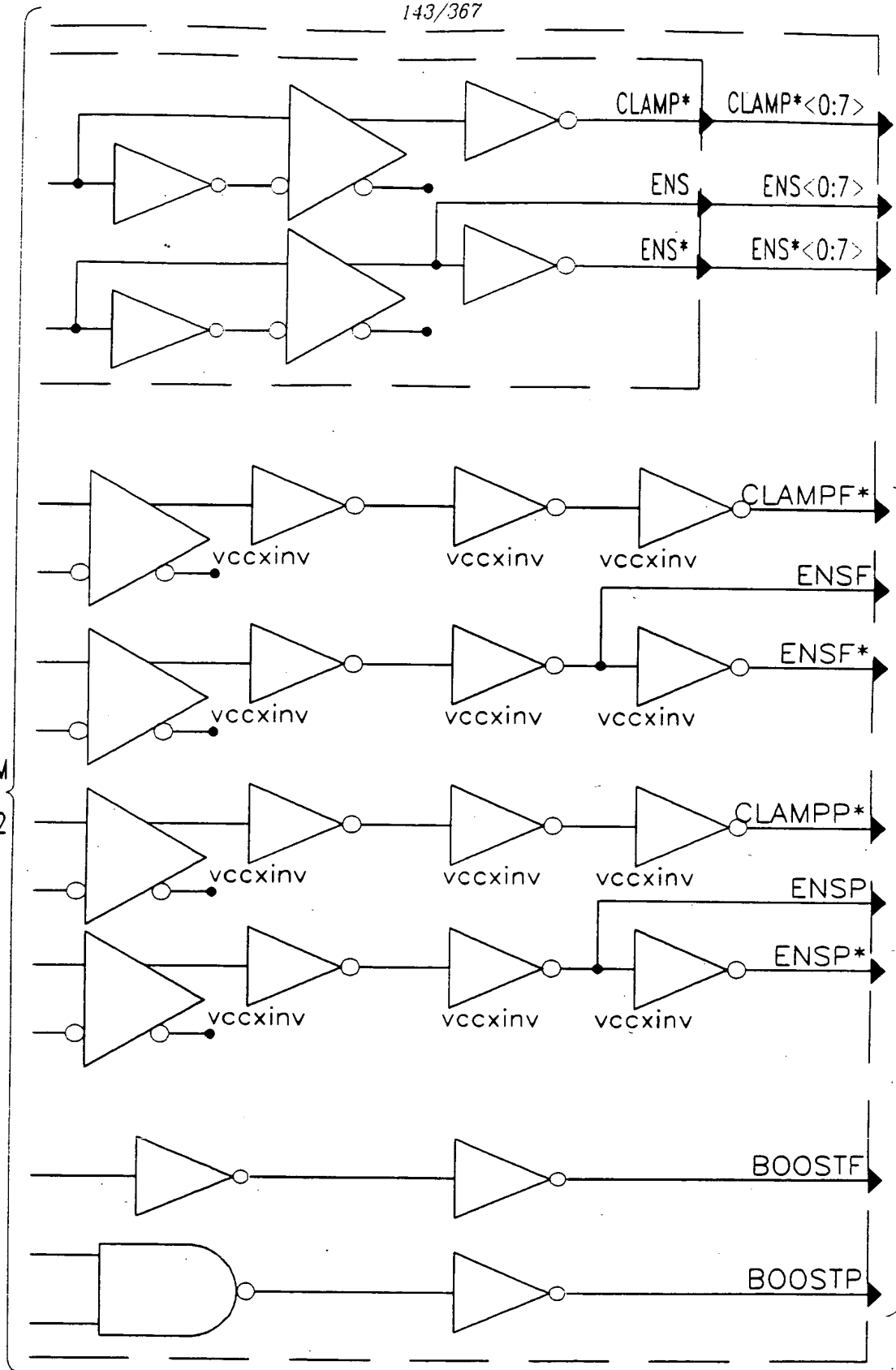


FIG. 36C3

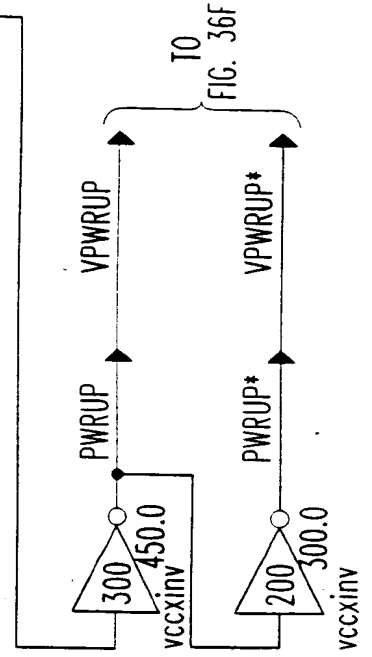
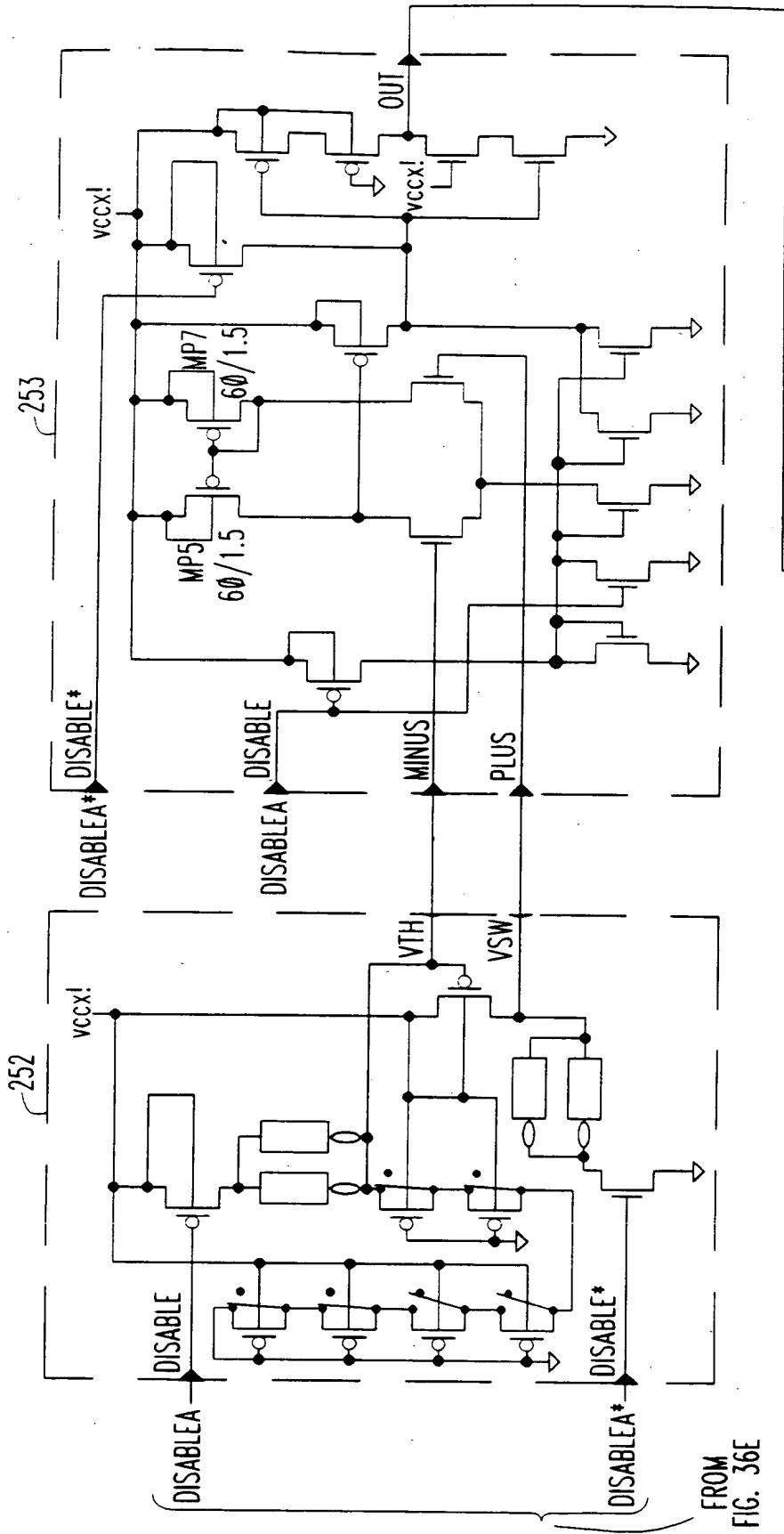
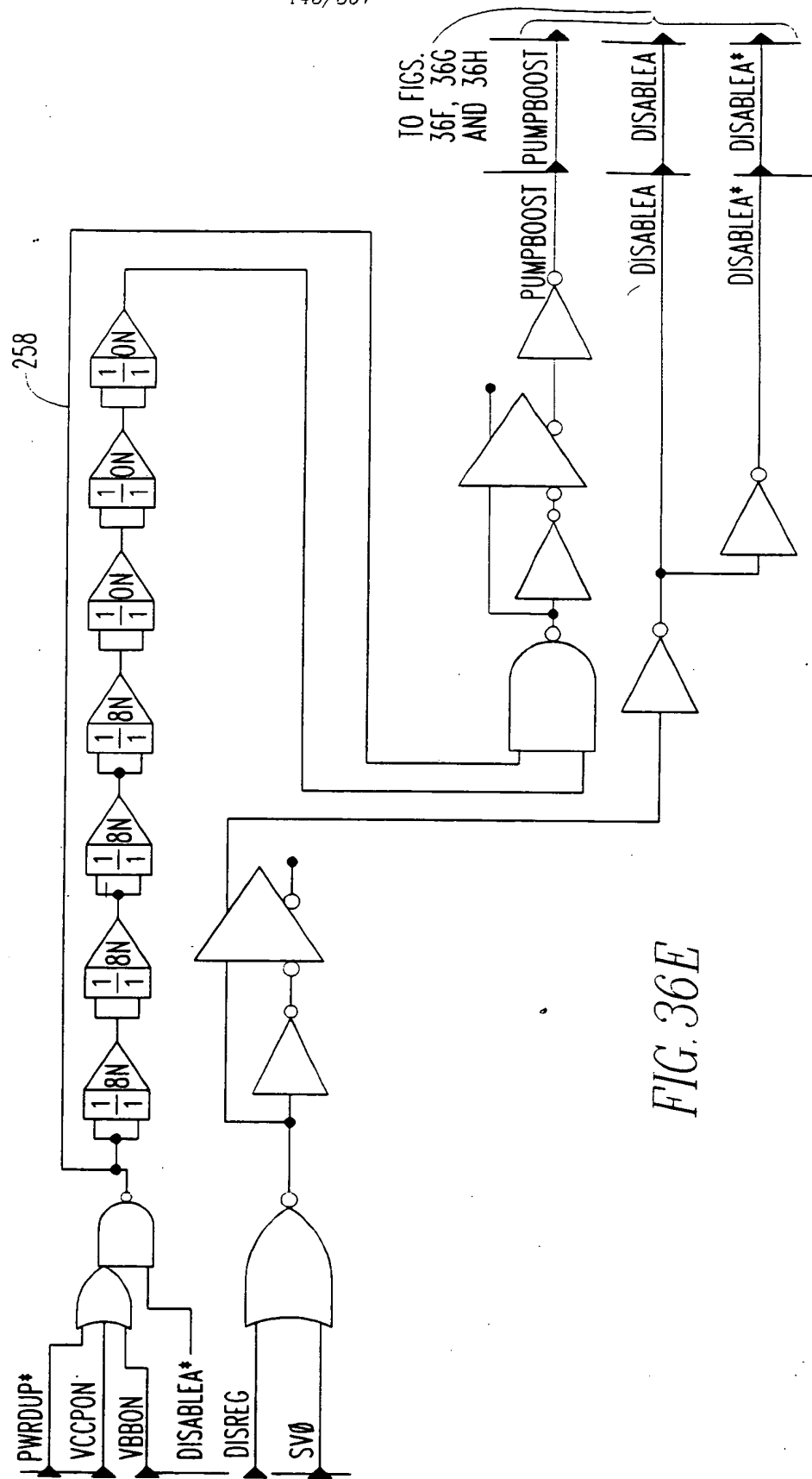


FIG. 36D



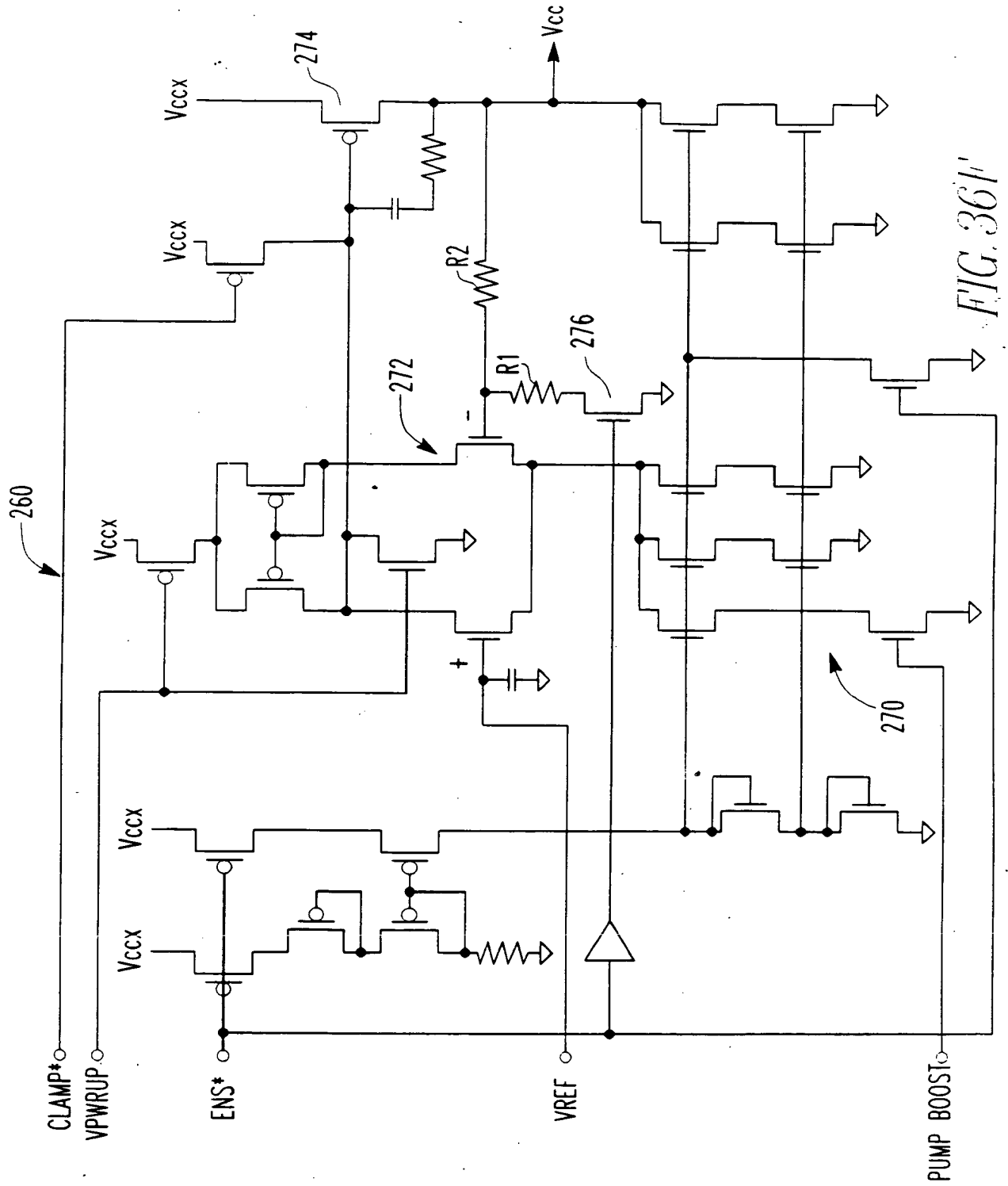


FIG. 36A

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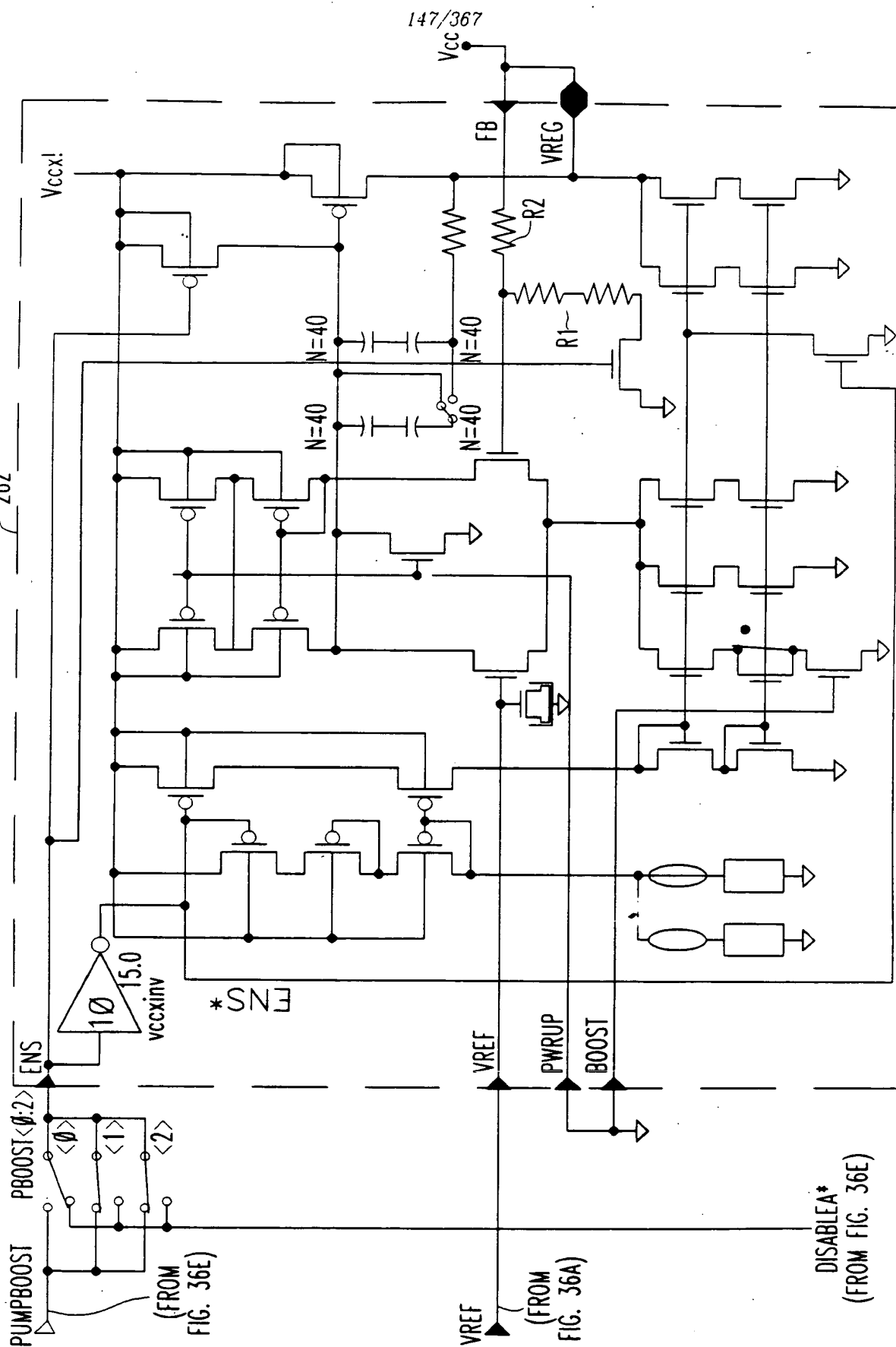


FIG. 36G

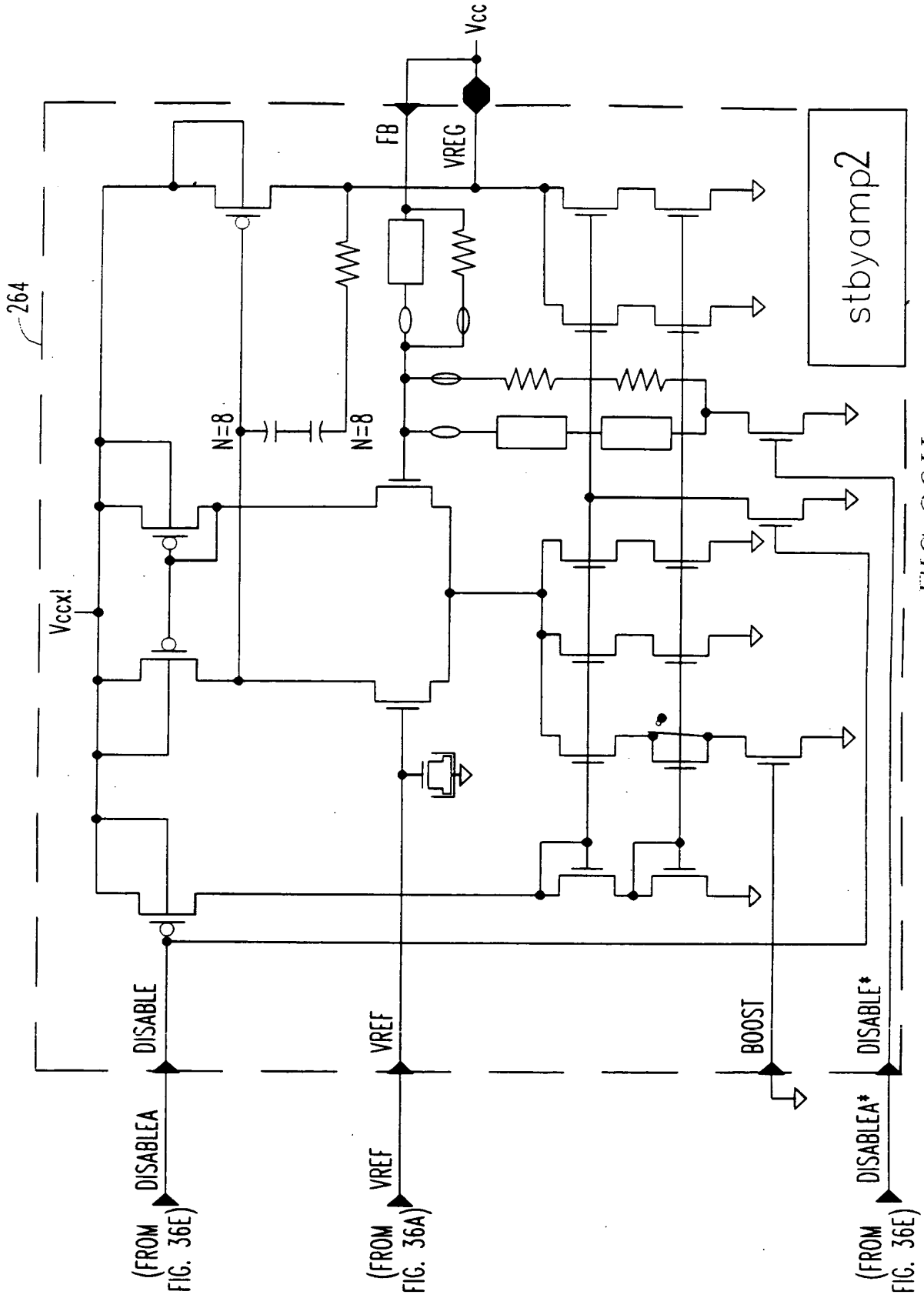


FIG. 36H

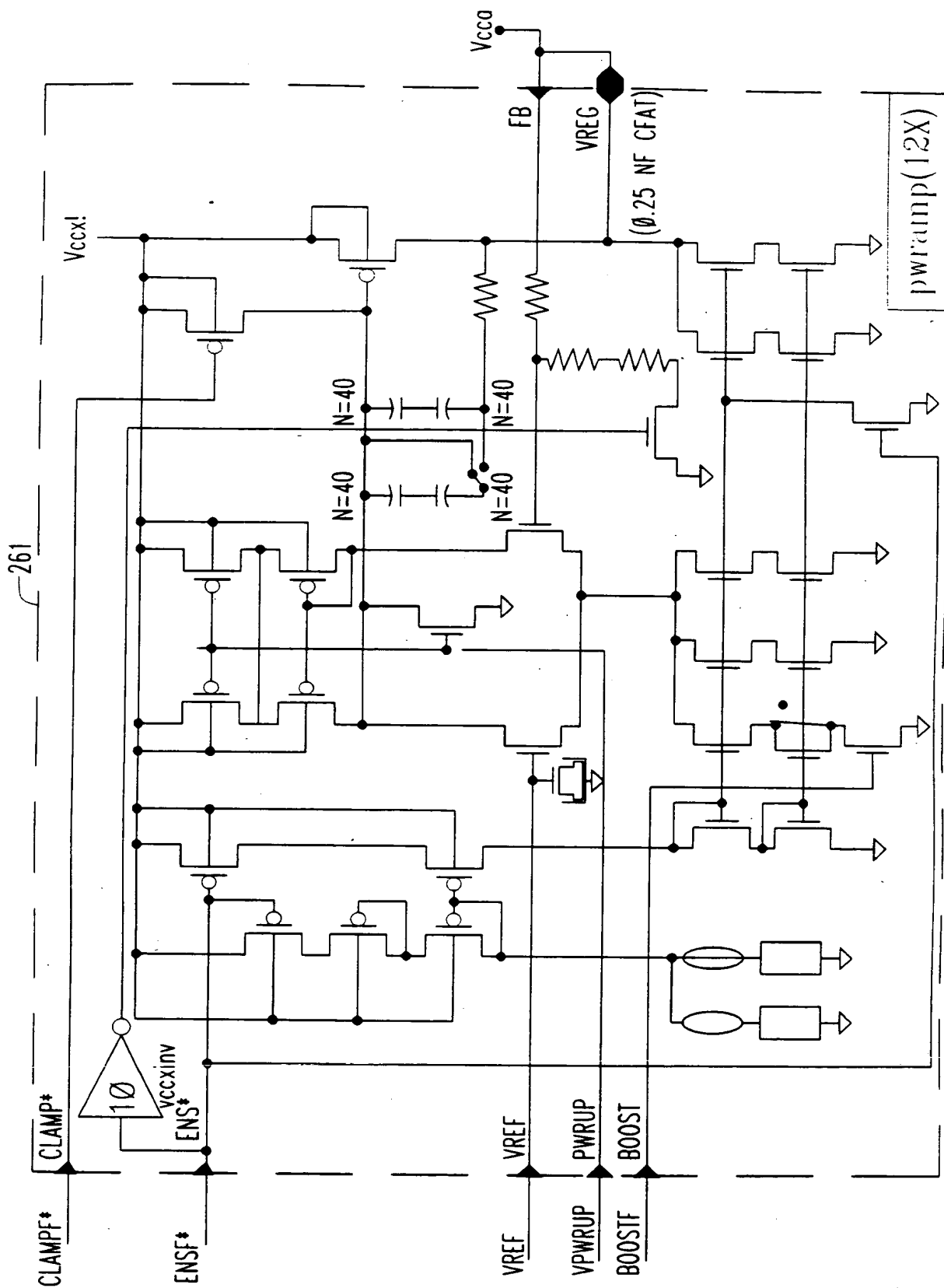


FIG. 361

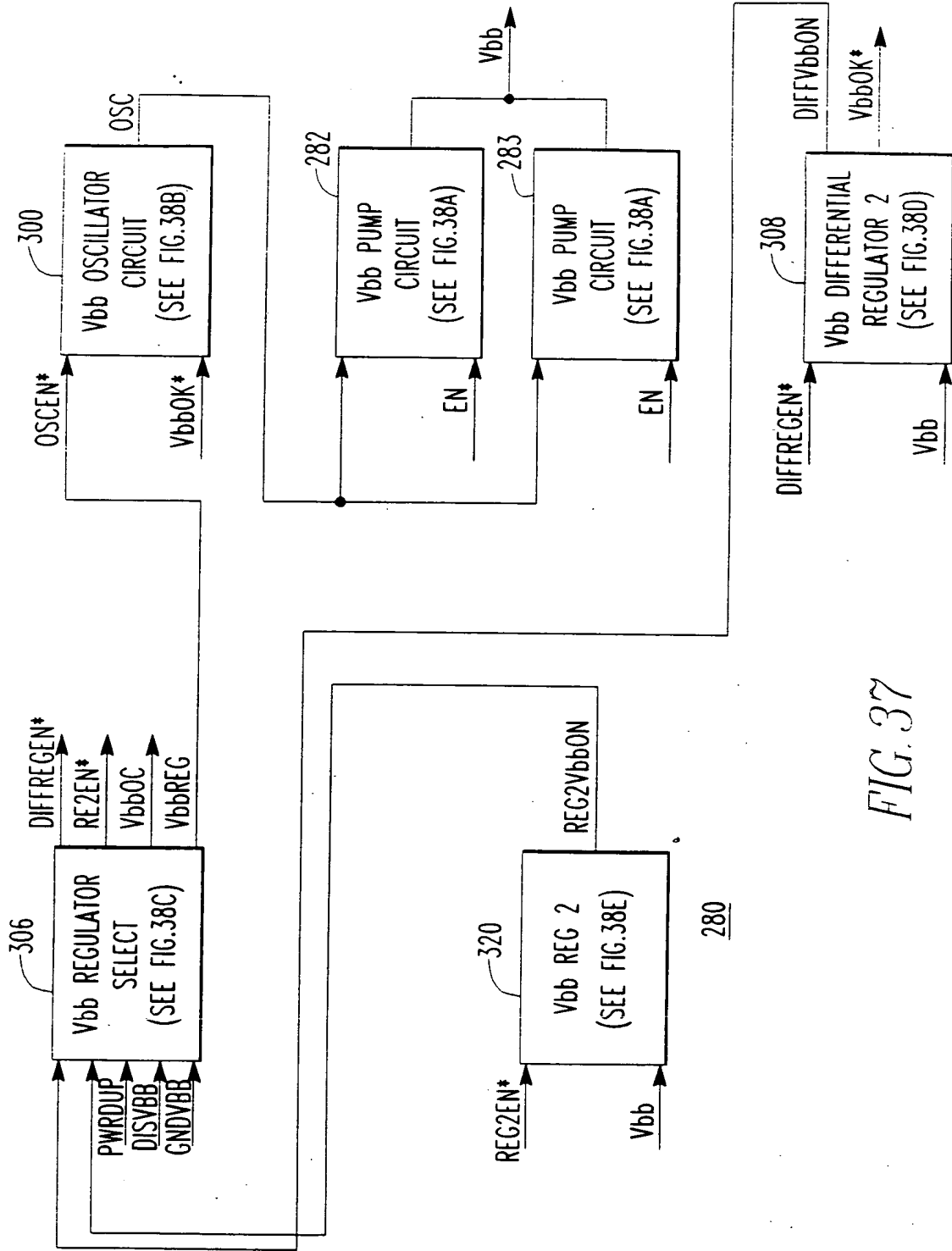


FIG. 37

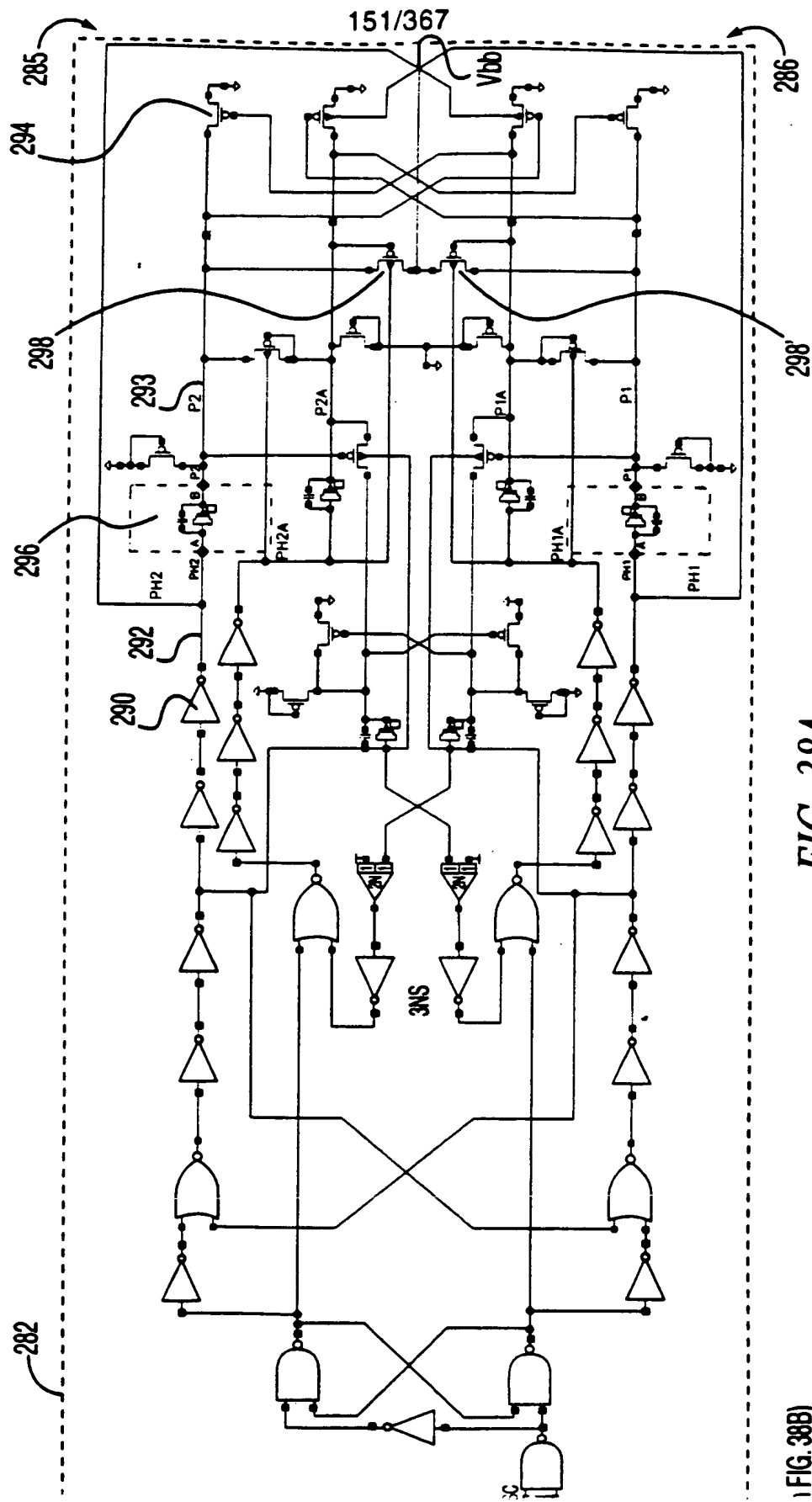
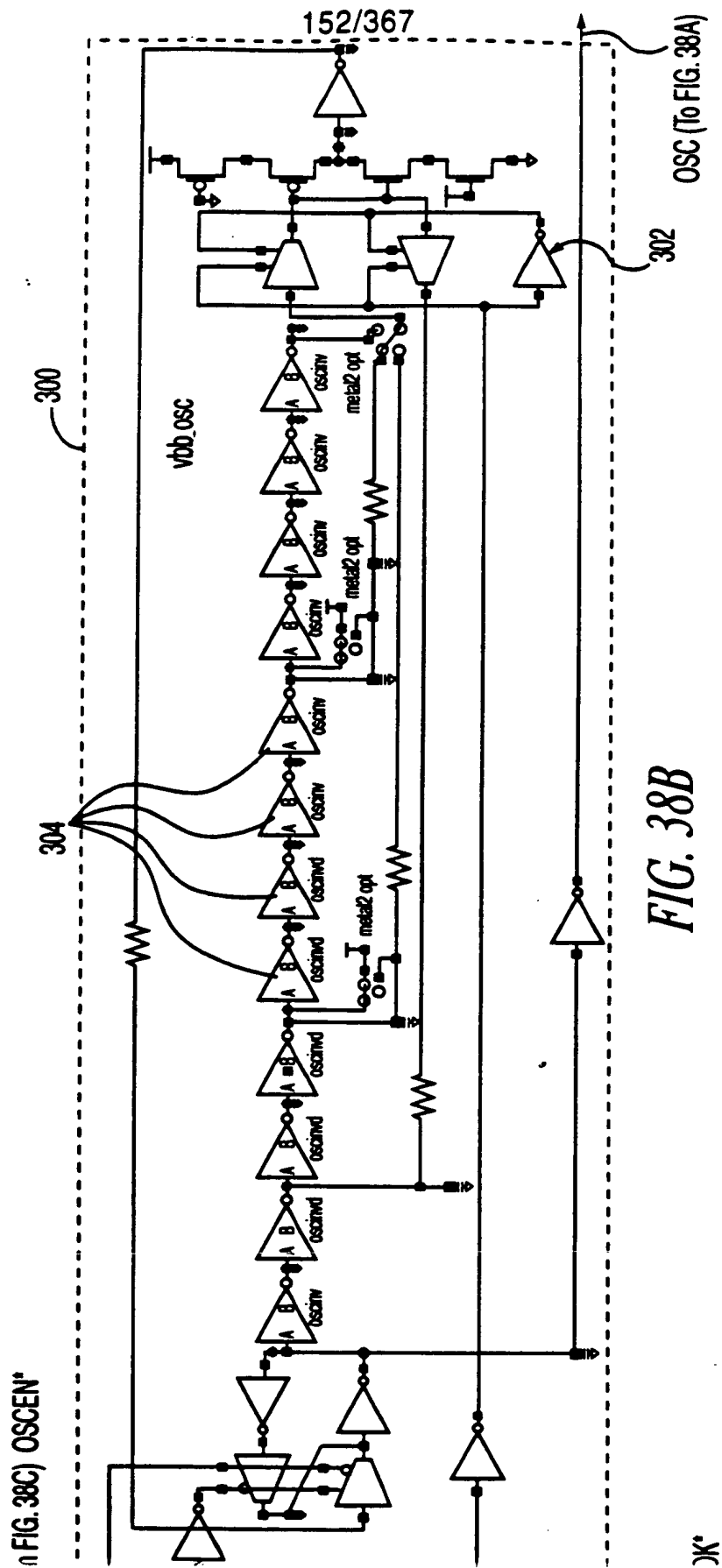


FIG. 38A

FIG. 38B



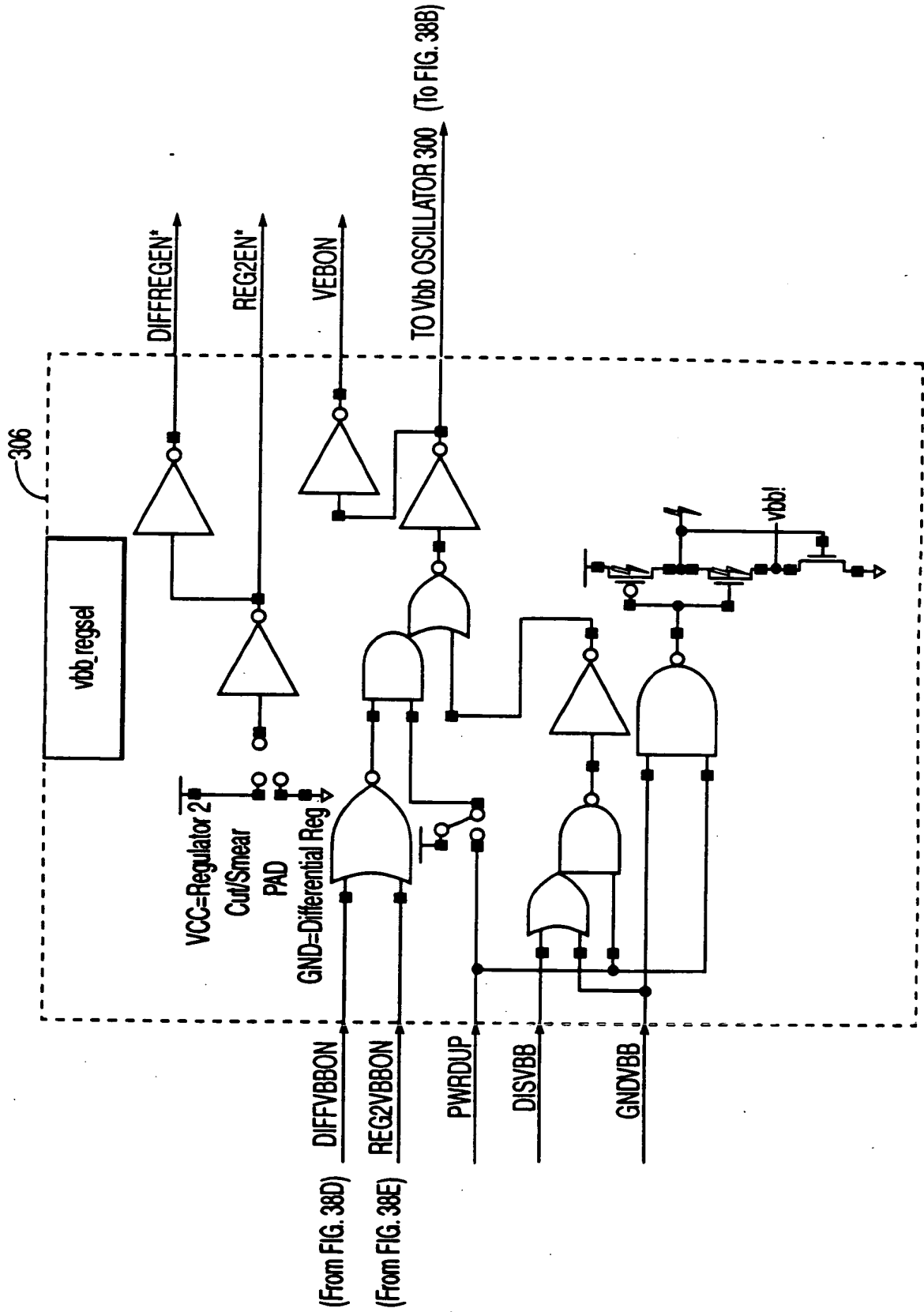
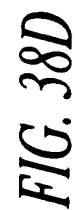


FIG. 38C



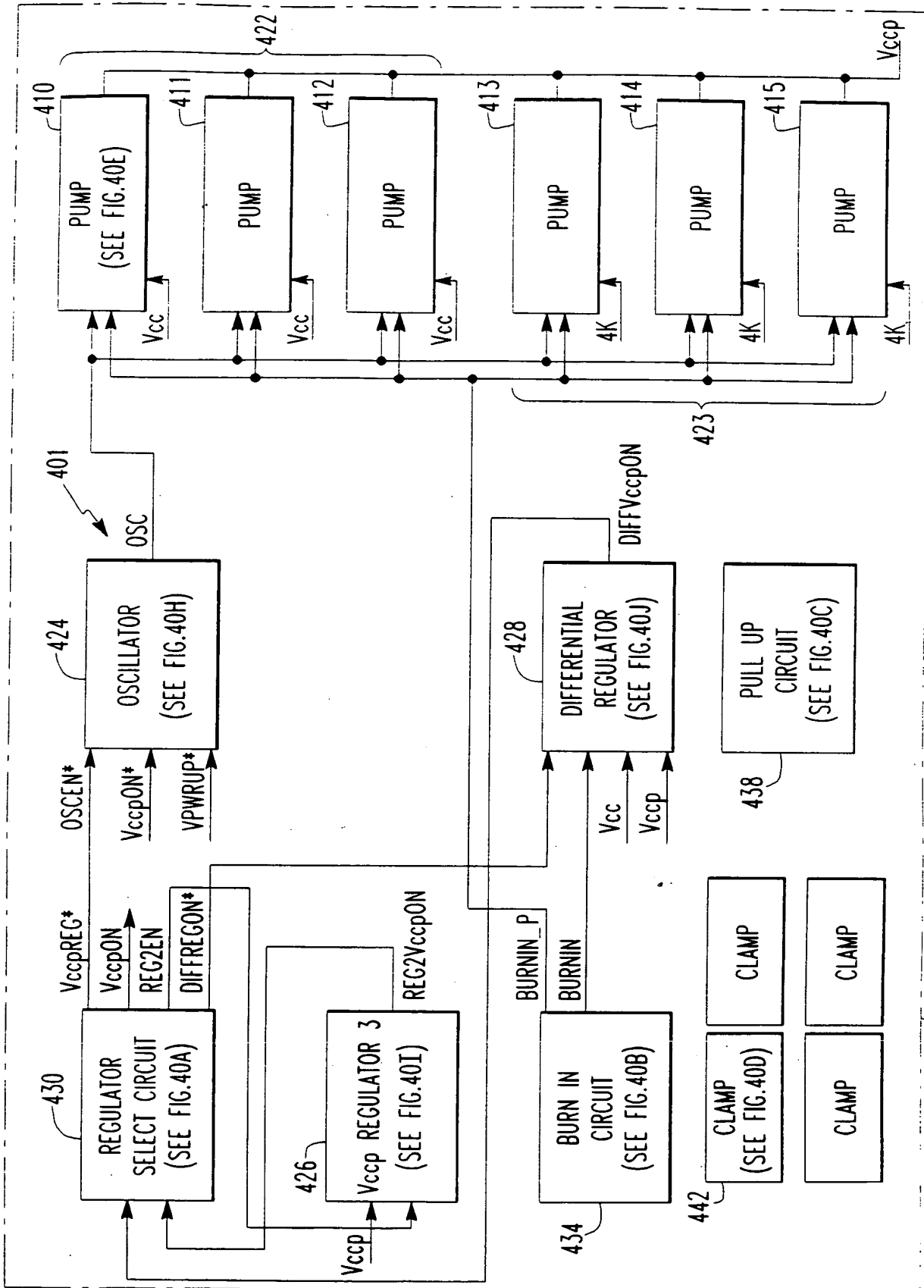


FIG. 39

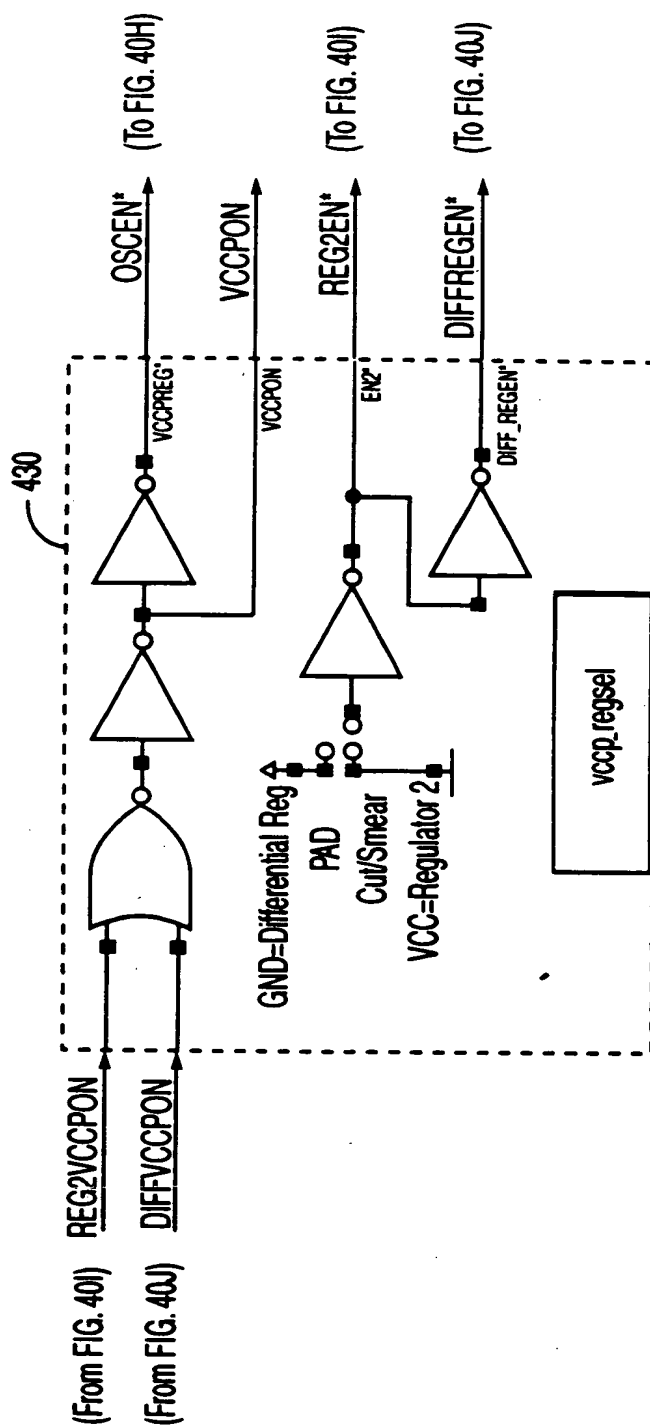


FIG. 40A

FIG. 40B

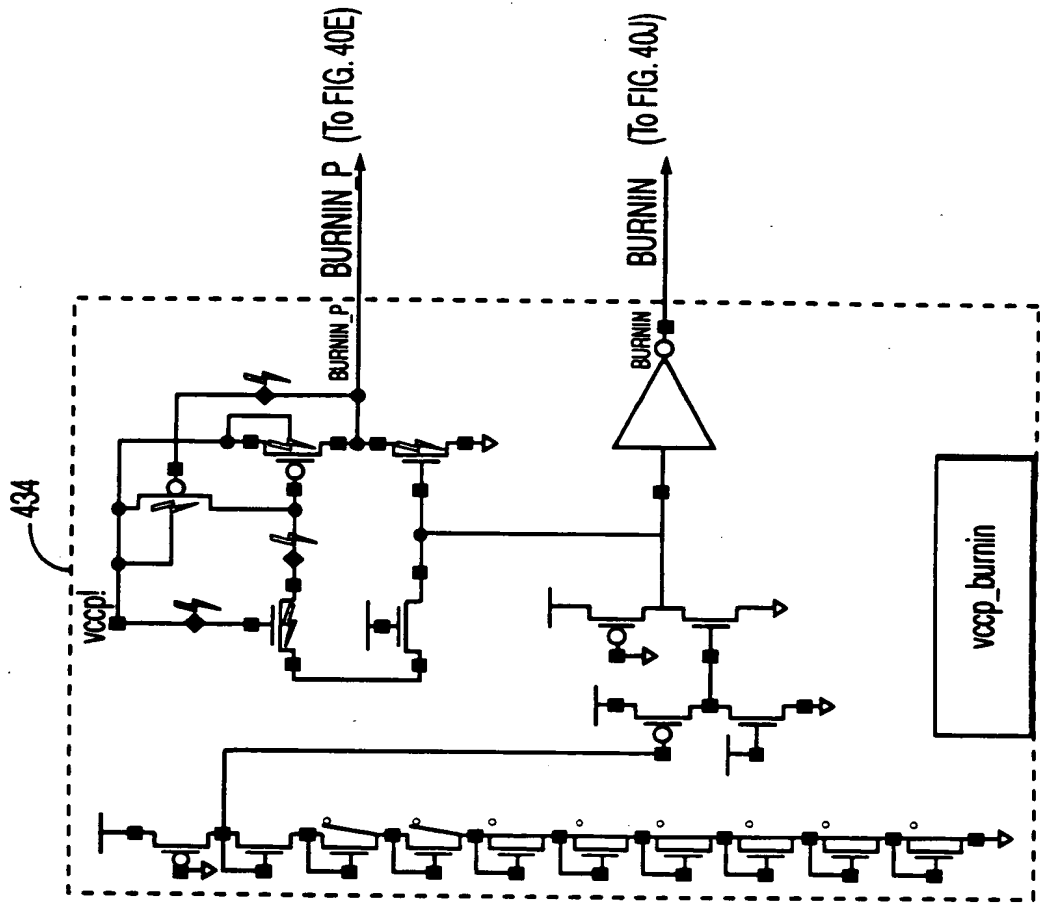


FIG. 40B

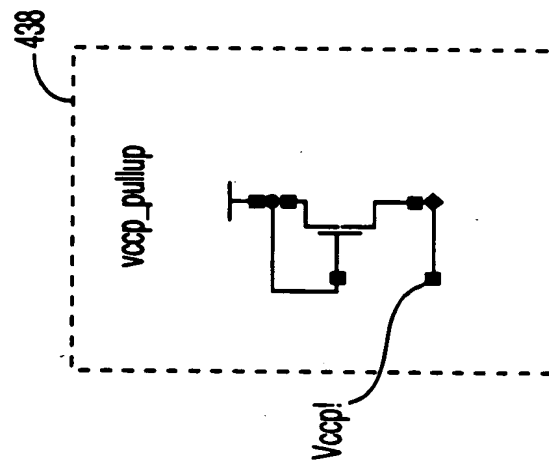


FIG. 40C

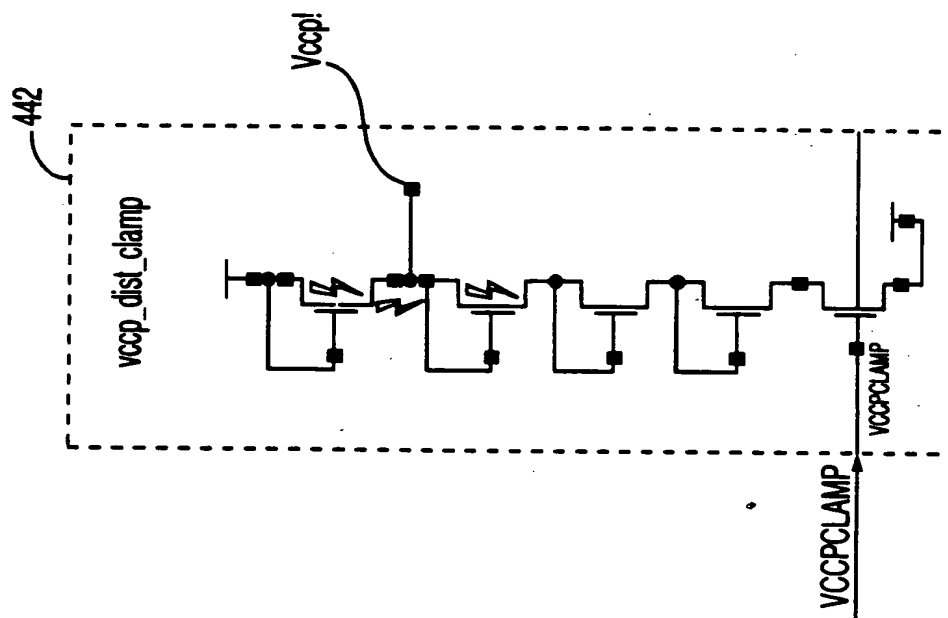
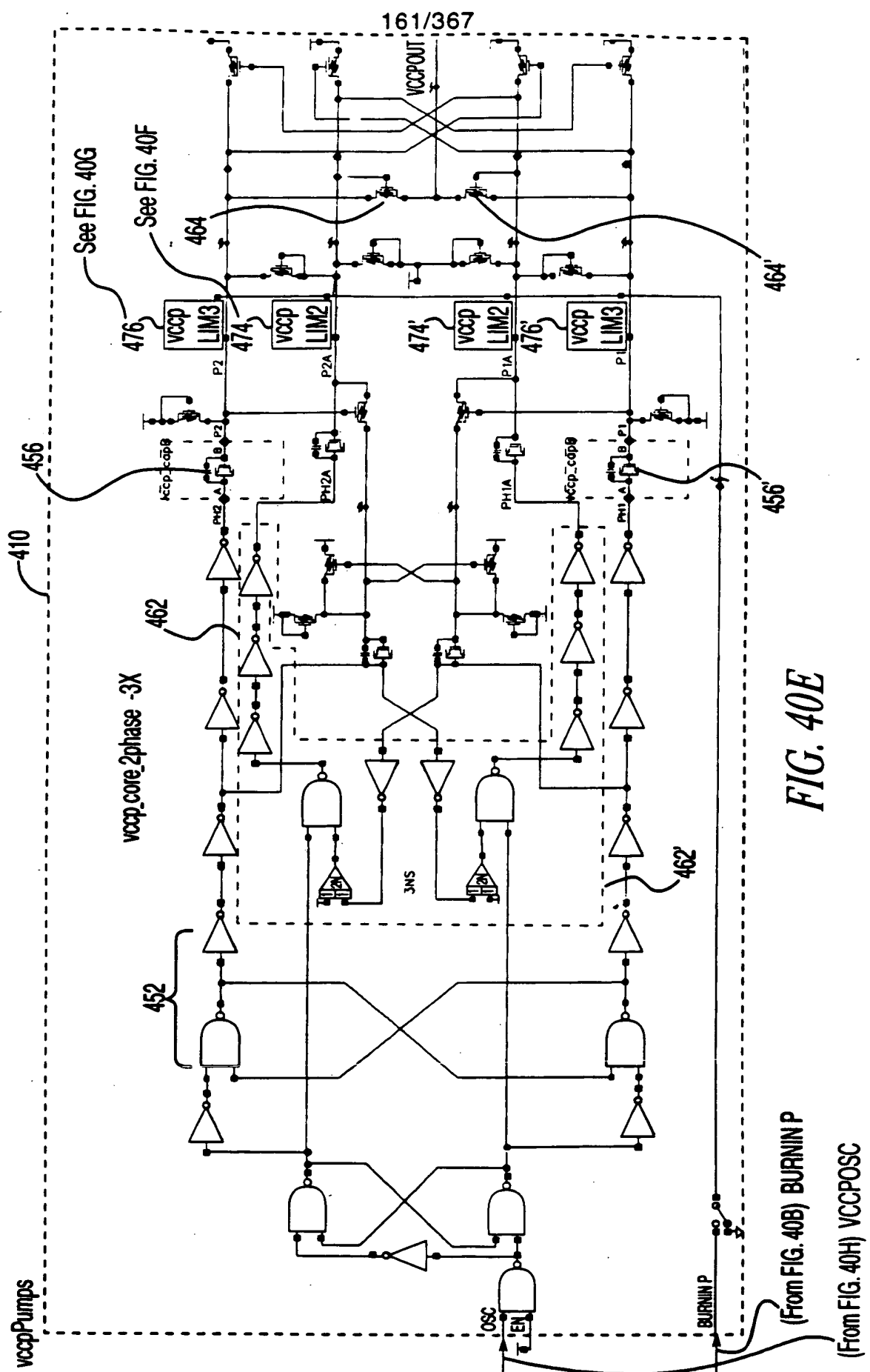


FIG. 40D



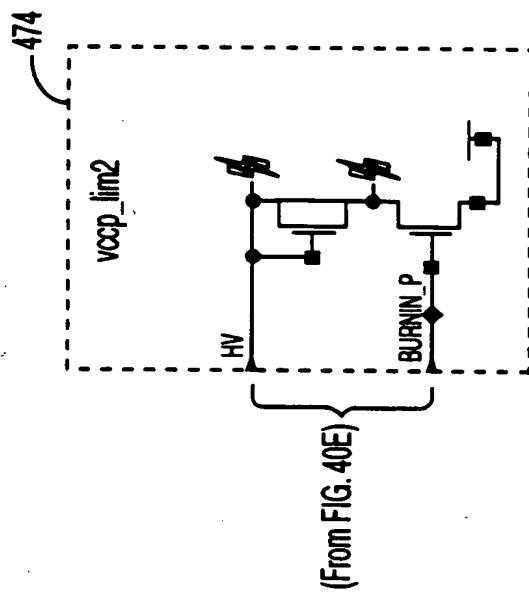


FIG. 40F

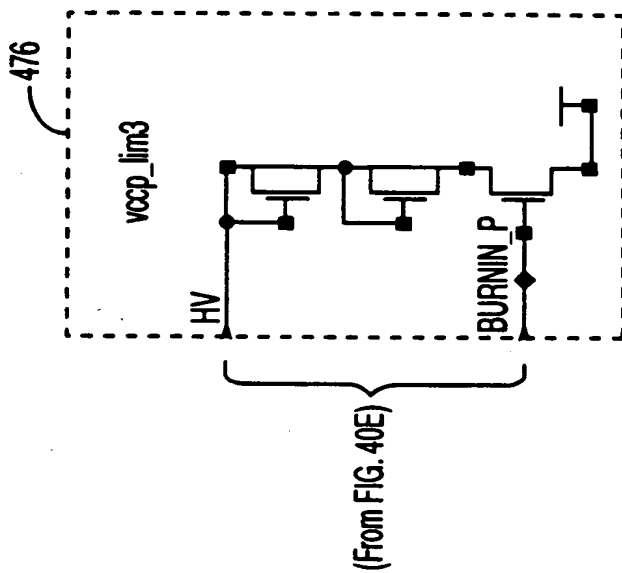
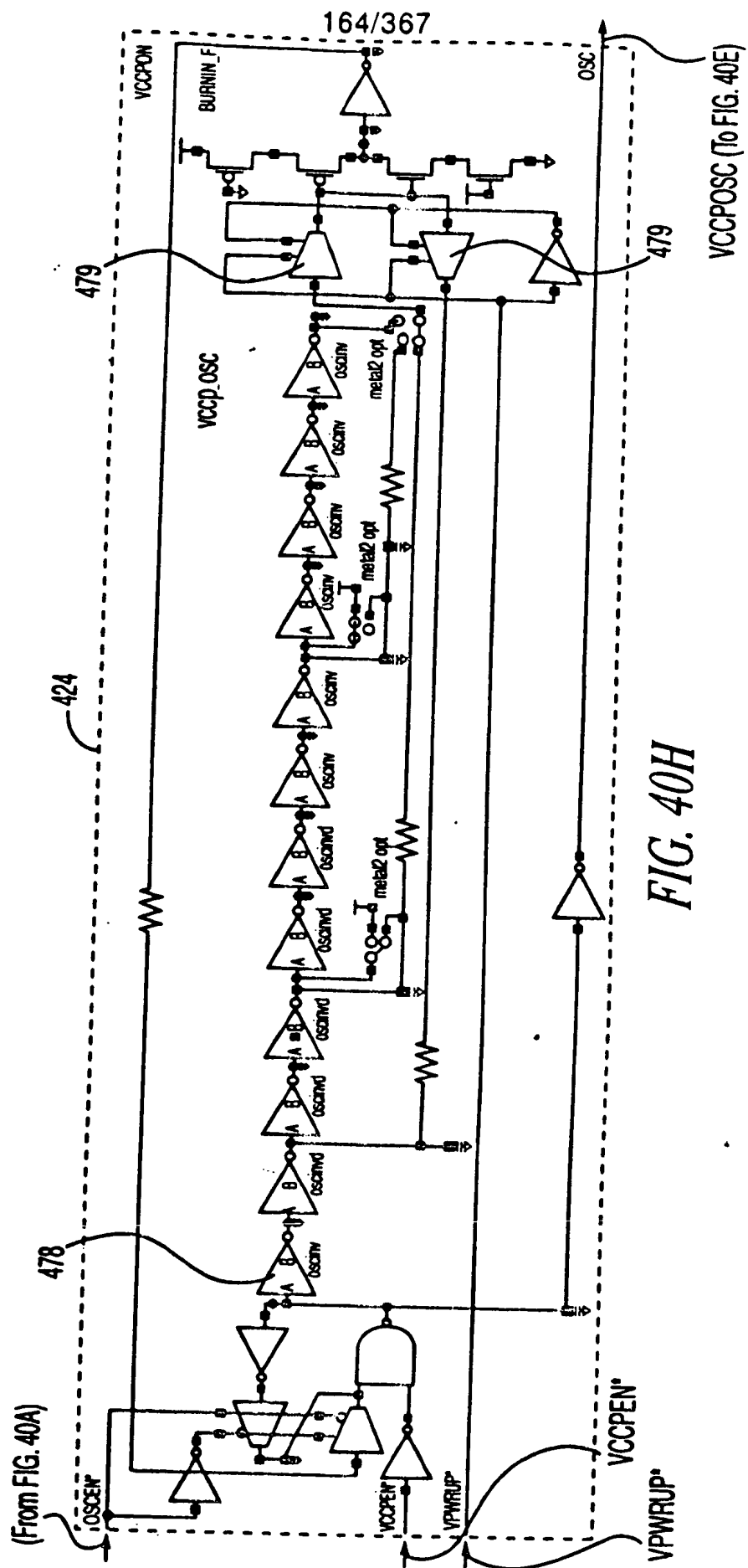


FIG. 40G



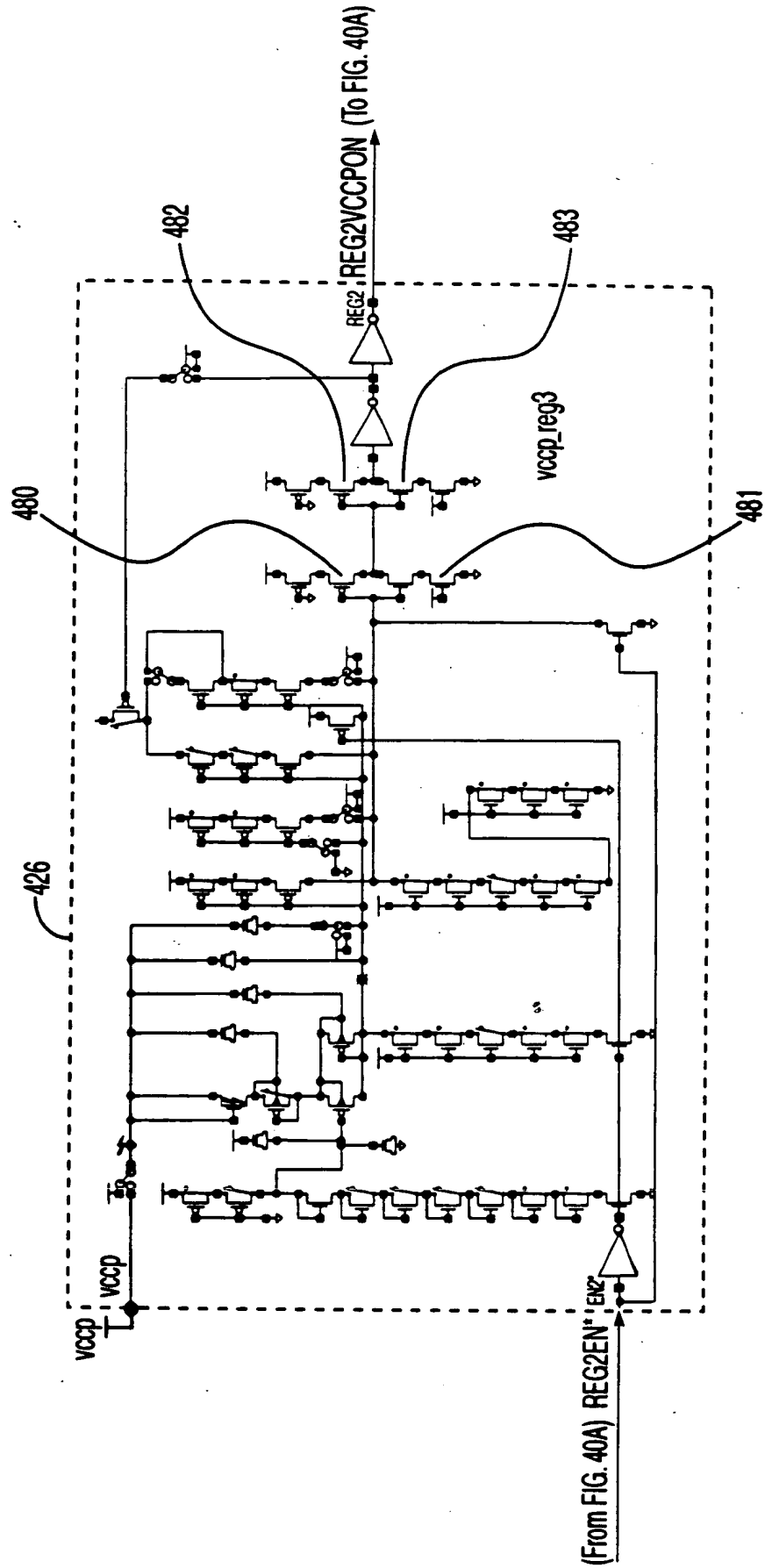


FIG. 401

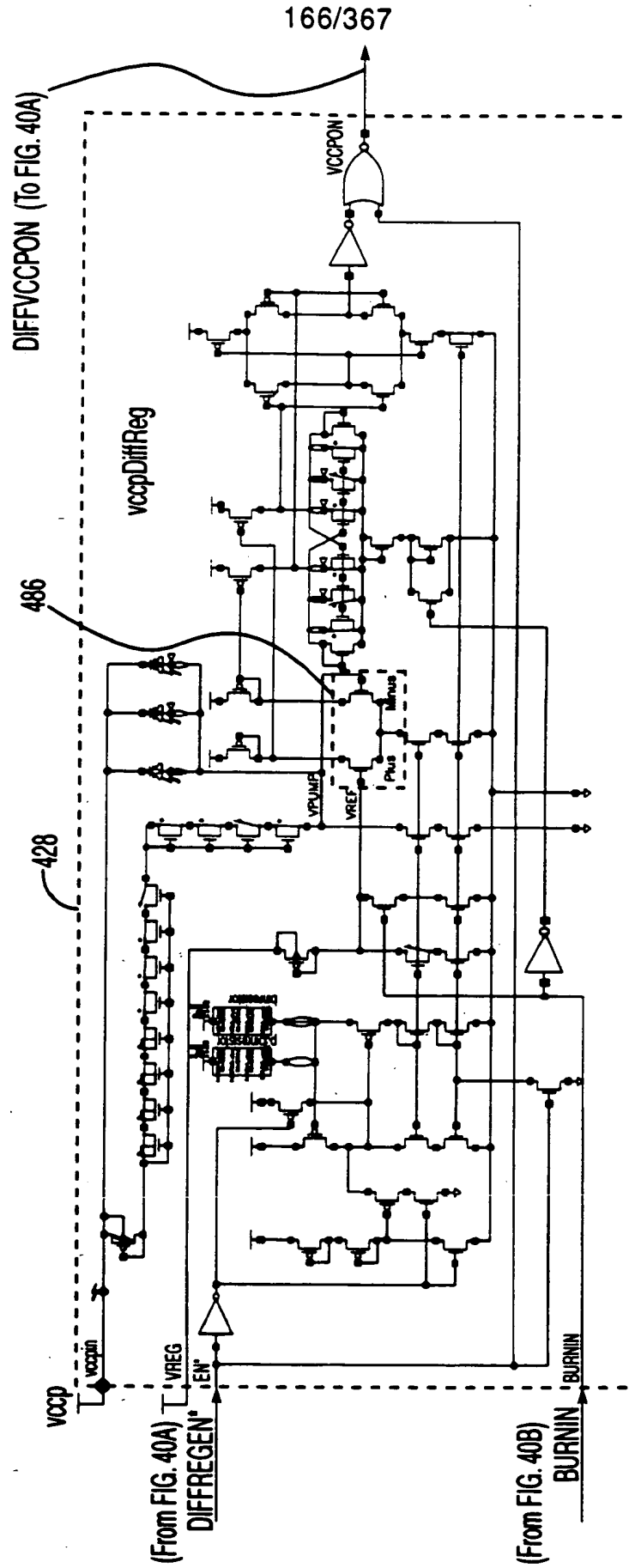
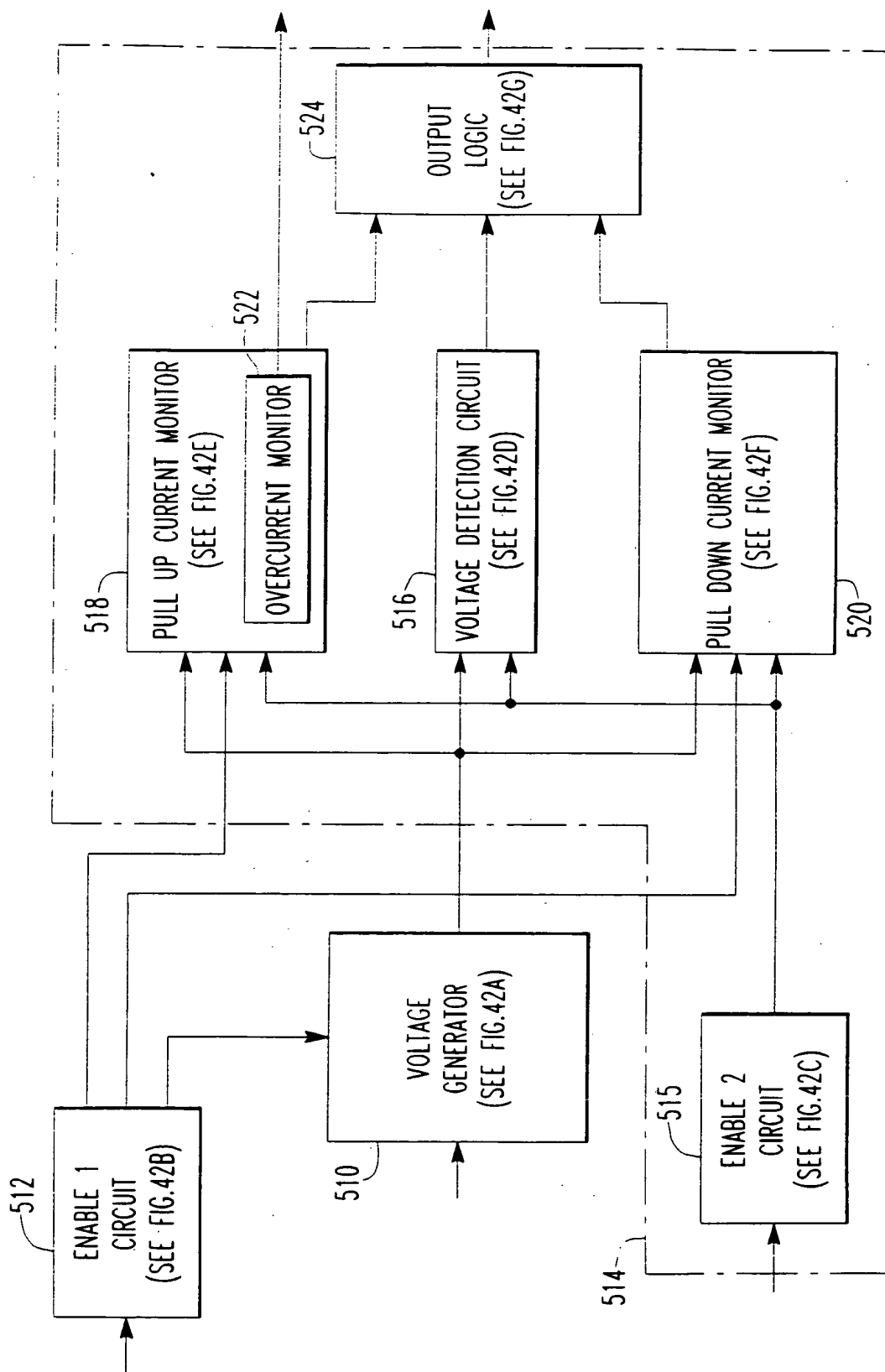


FIG. 40J



500

FIG. 41

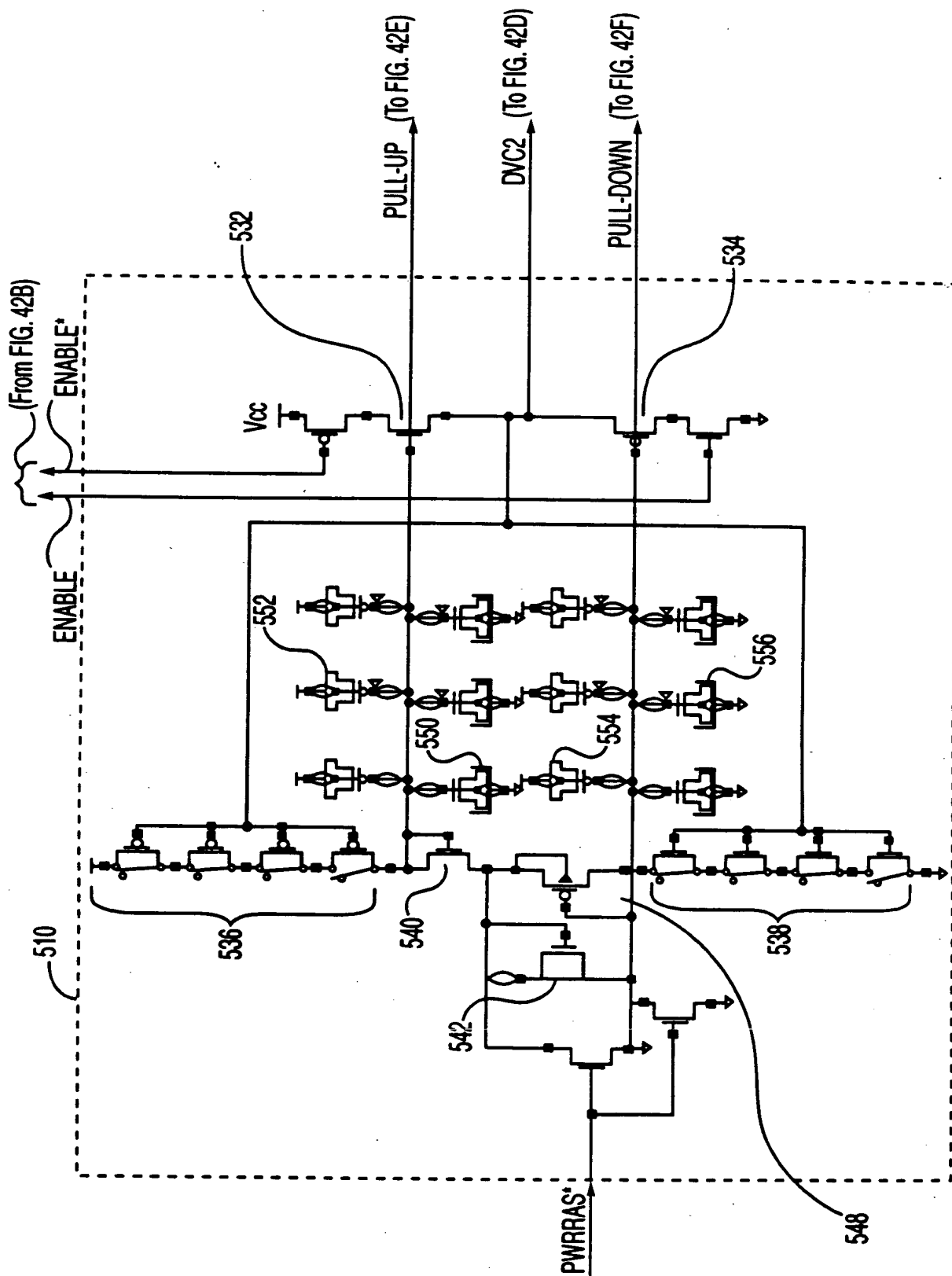


FIG. 42A

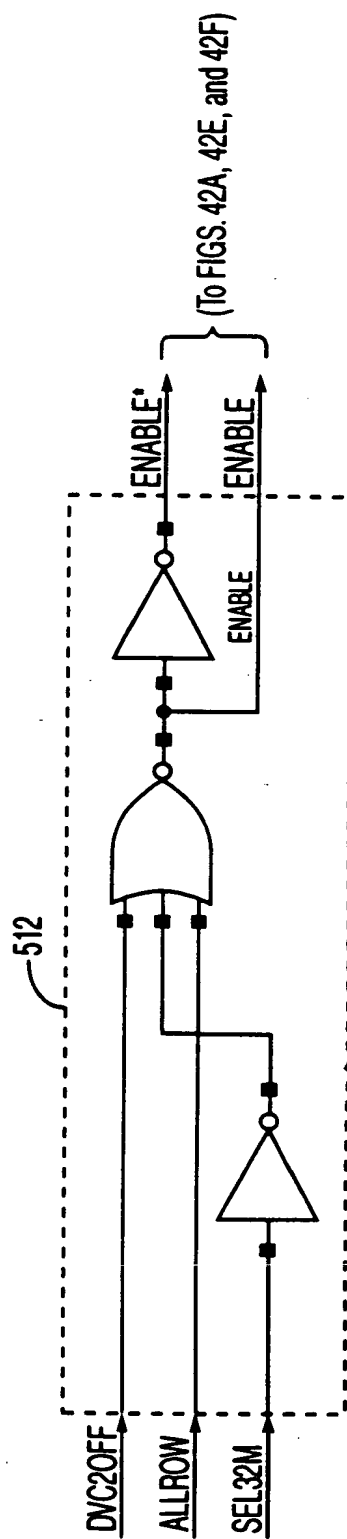


FIG. 42B

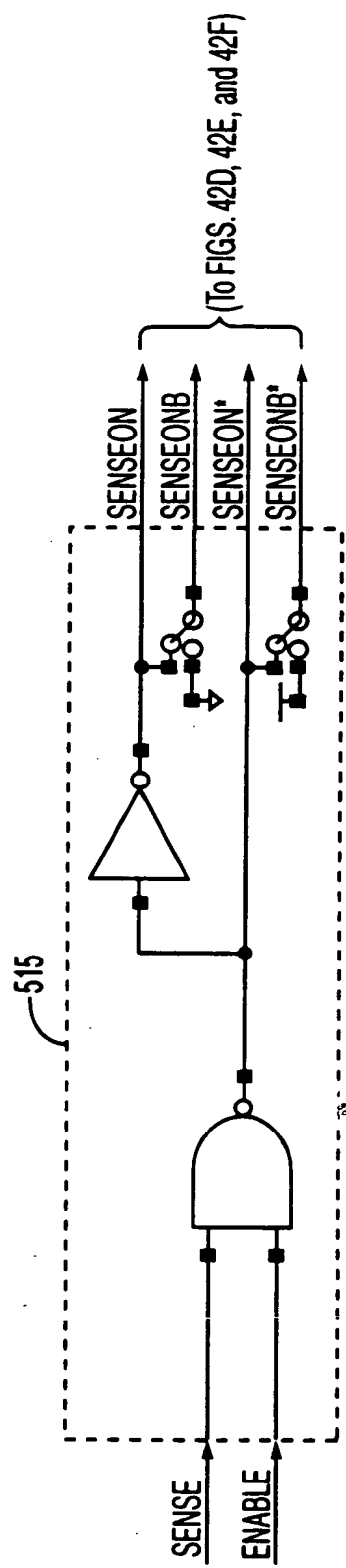


FIG. 42C

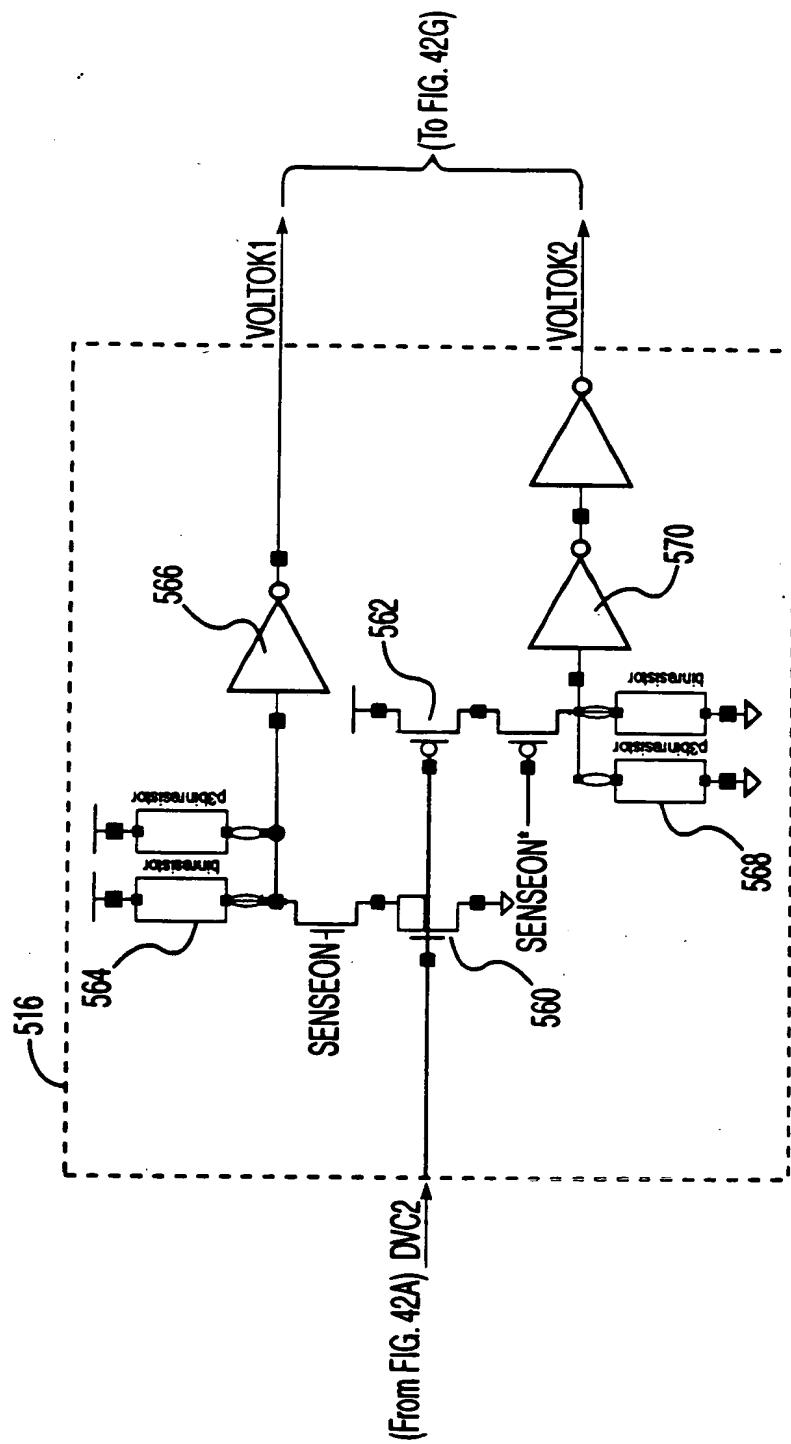


FIG. 42D

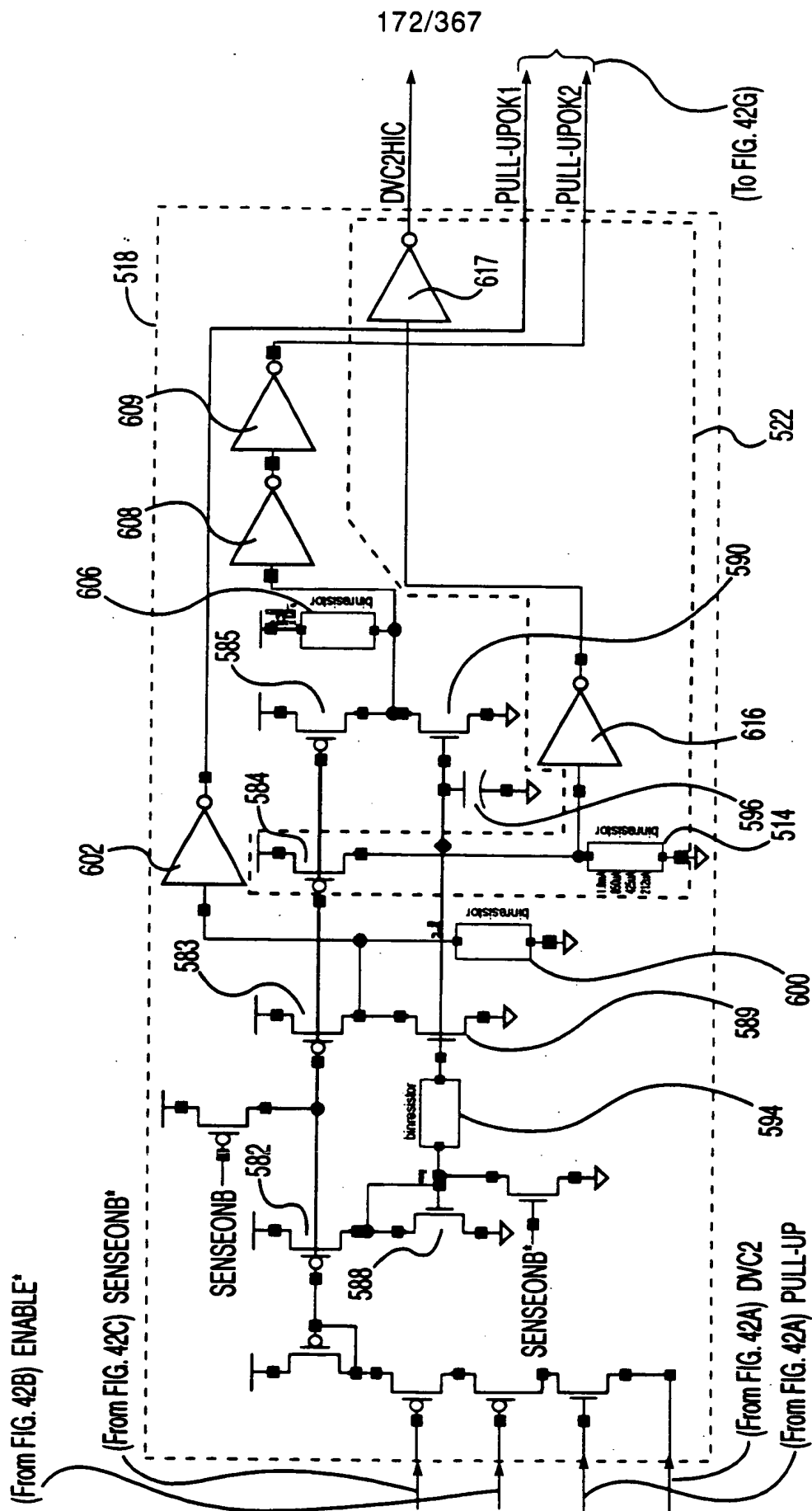


FIG. 42E

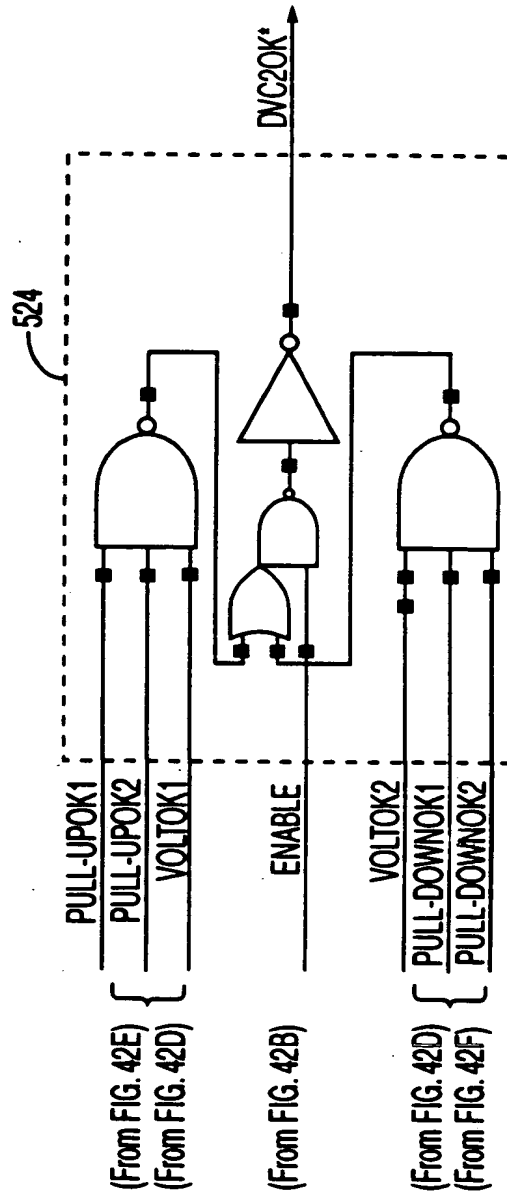


FIG. 42G

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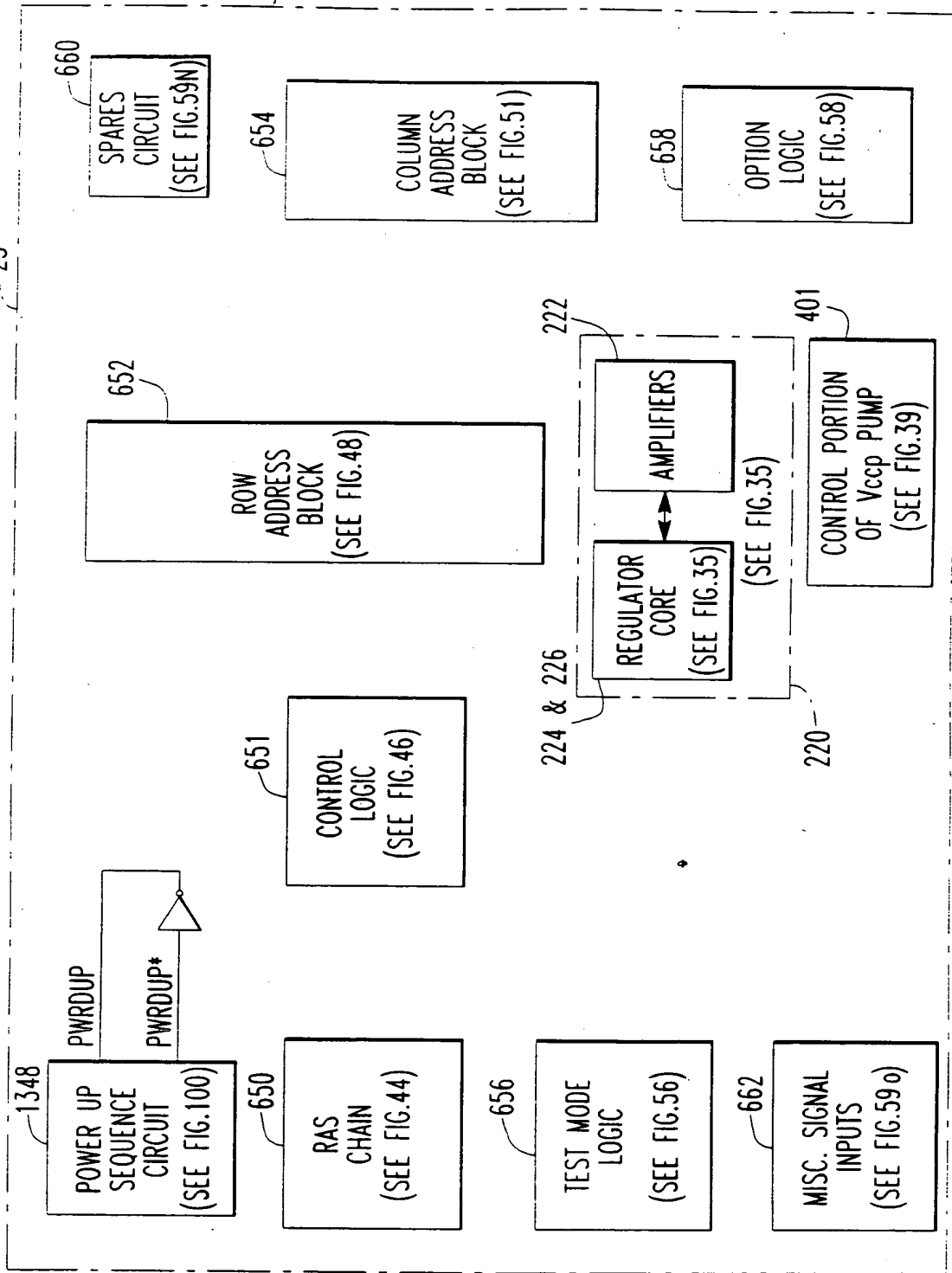


FIG. 43

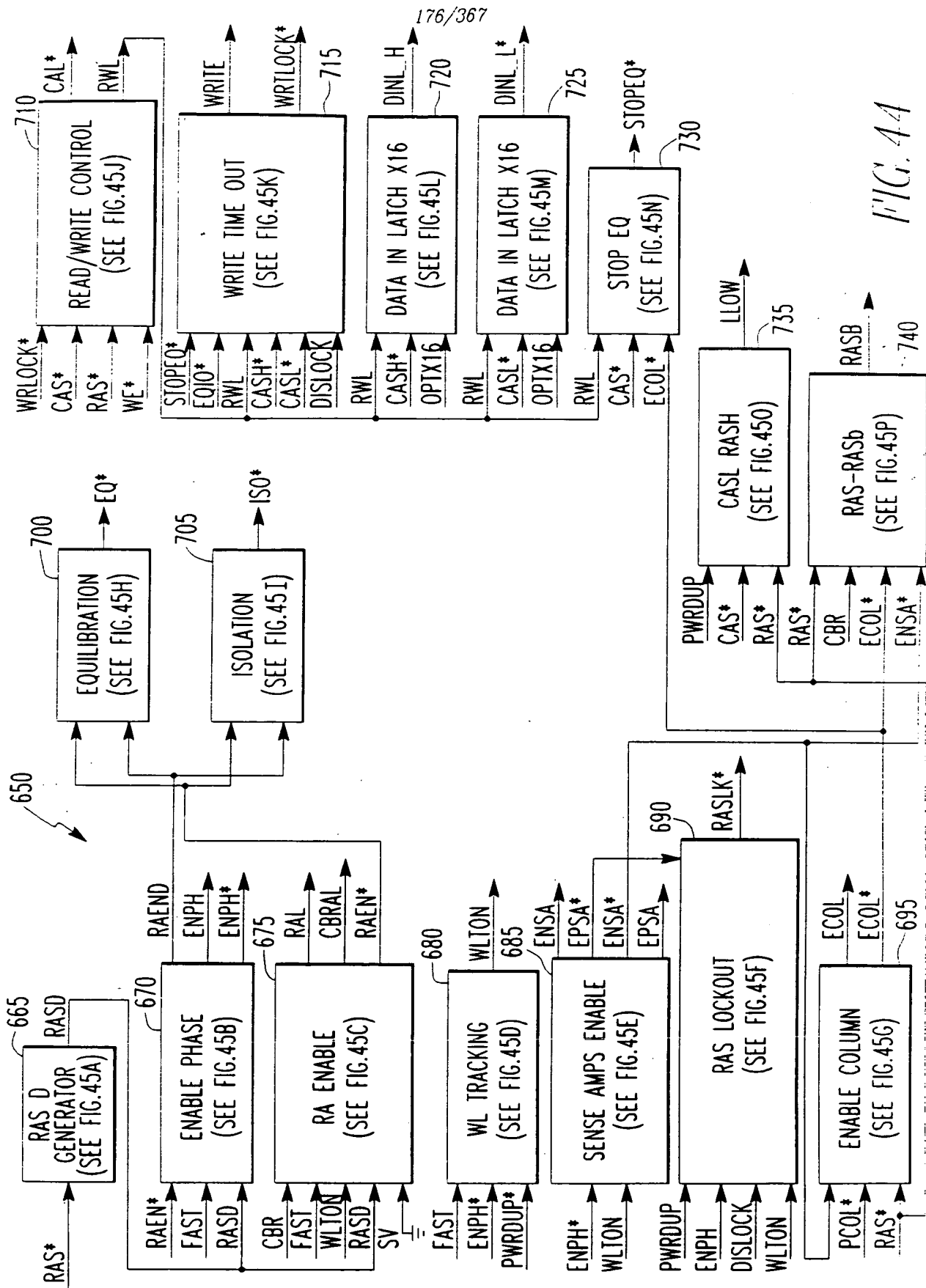


FIG. 44

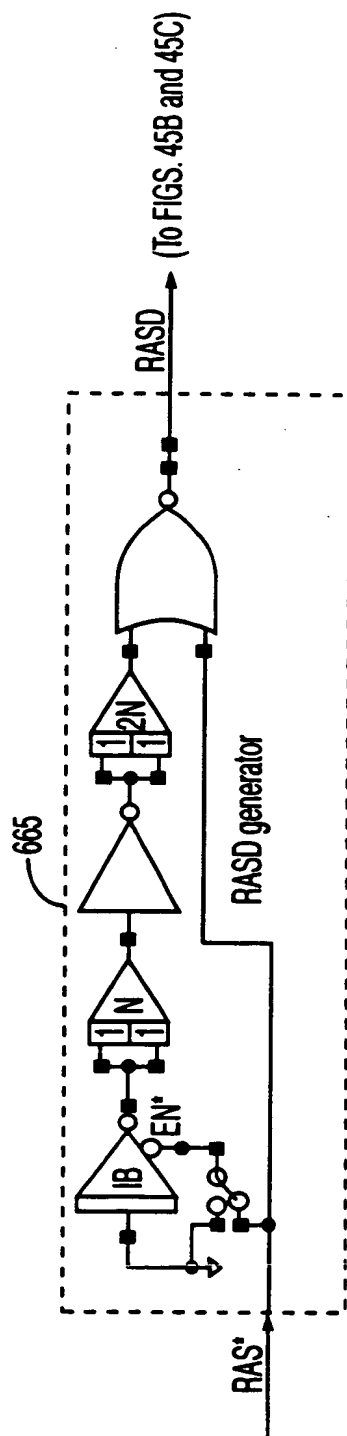


FIG. 45A



FIG. 45B

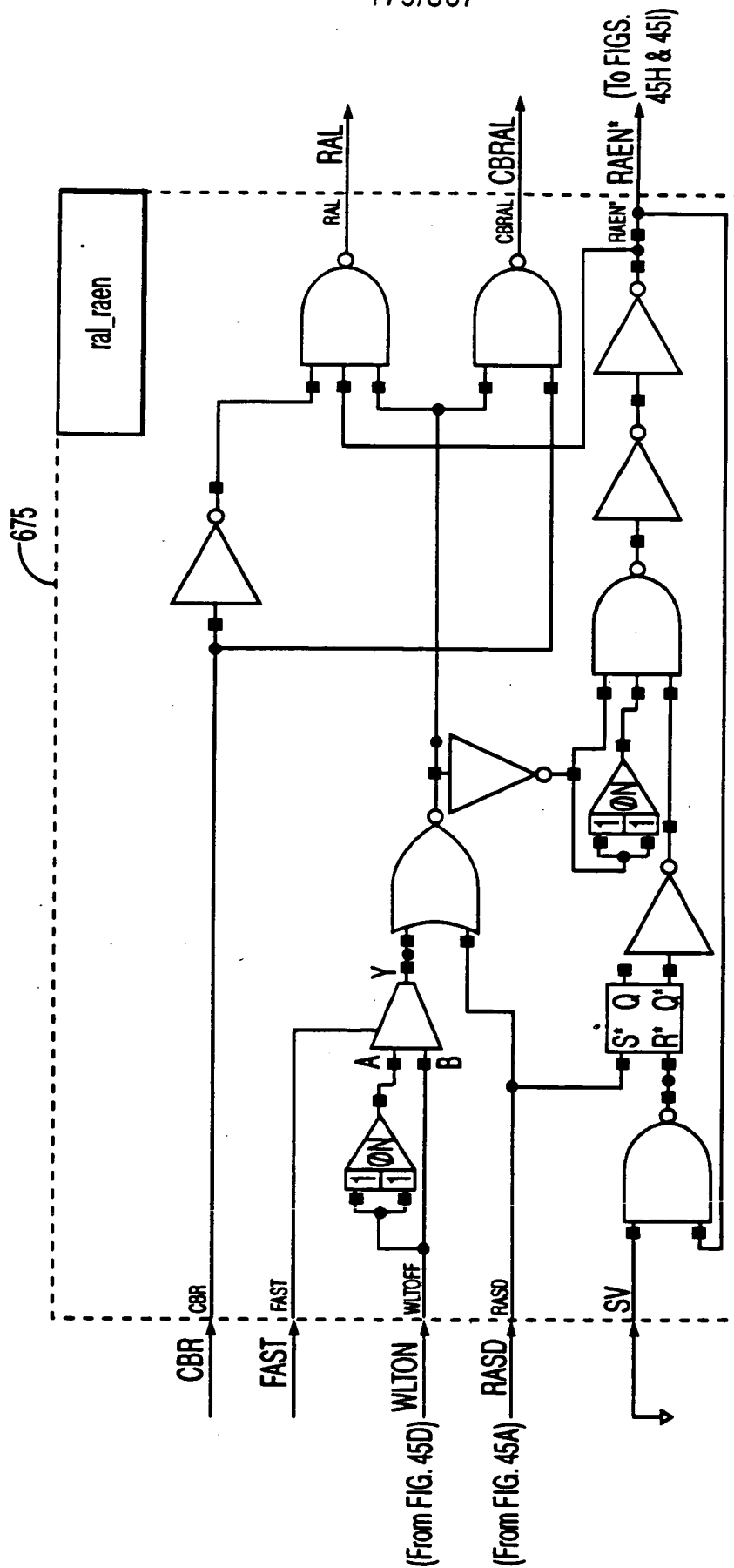


FIG. 45C

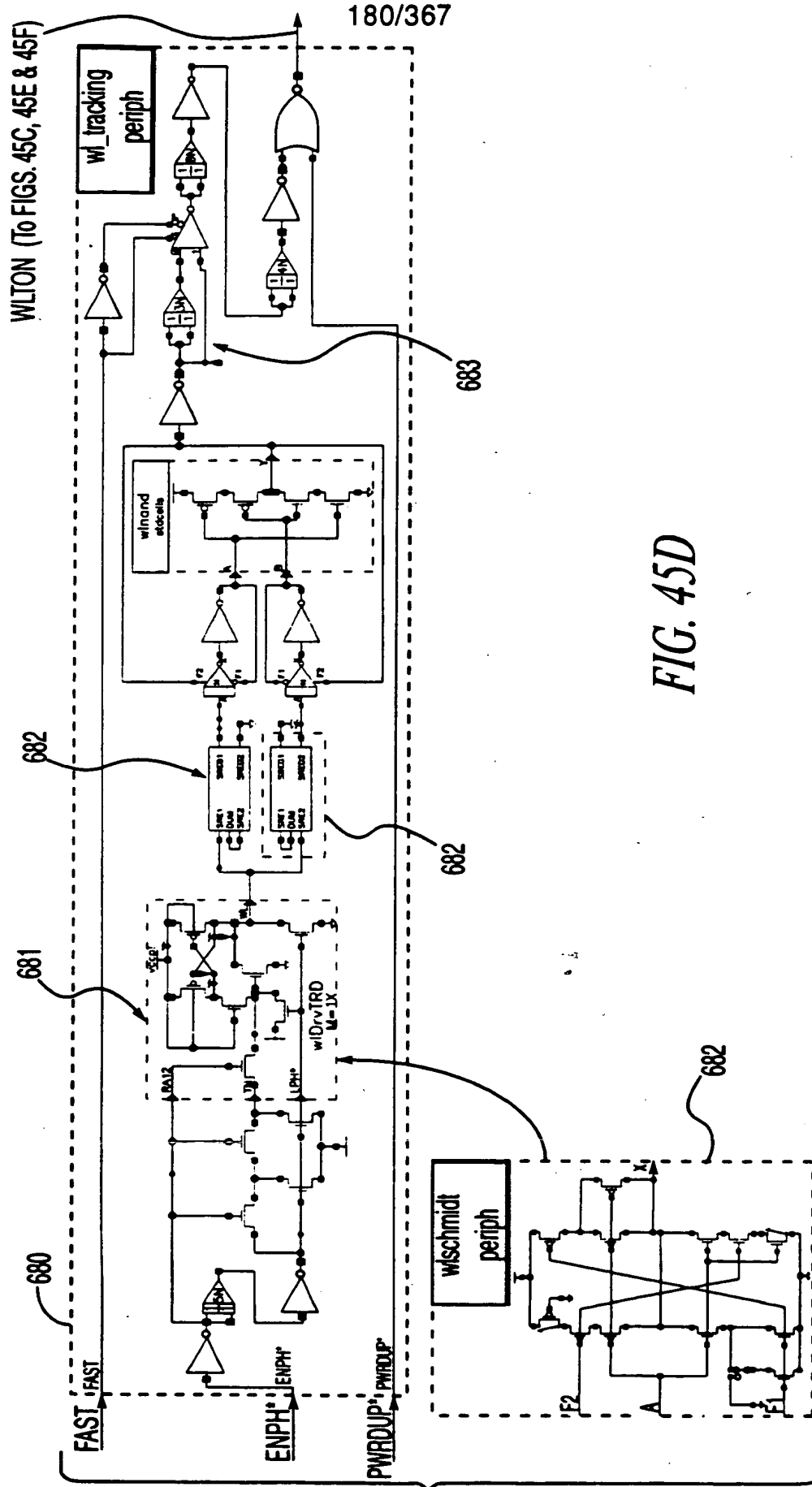


FIG. 45D

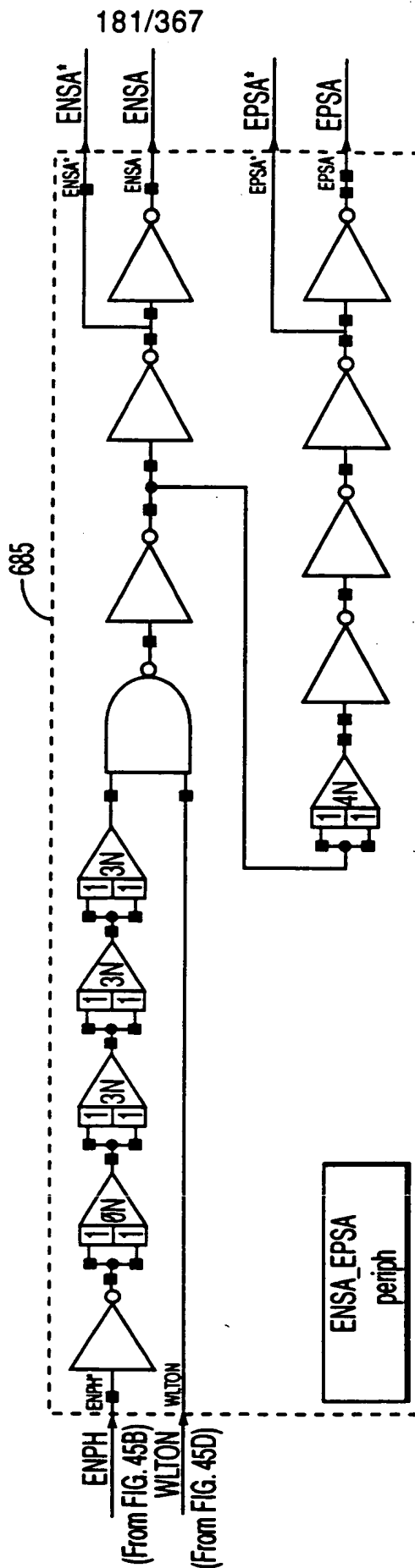


FIG. 45E

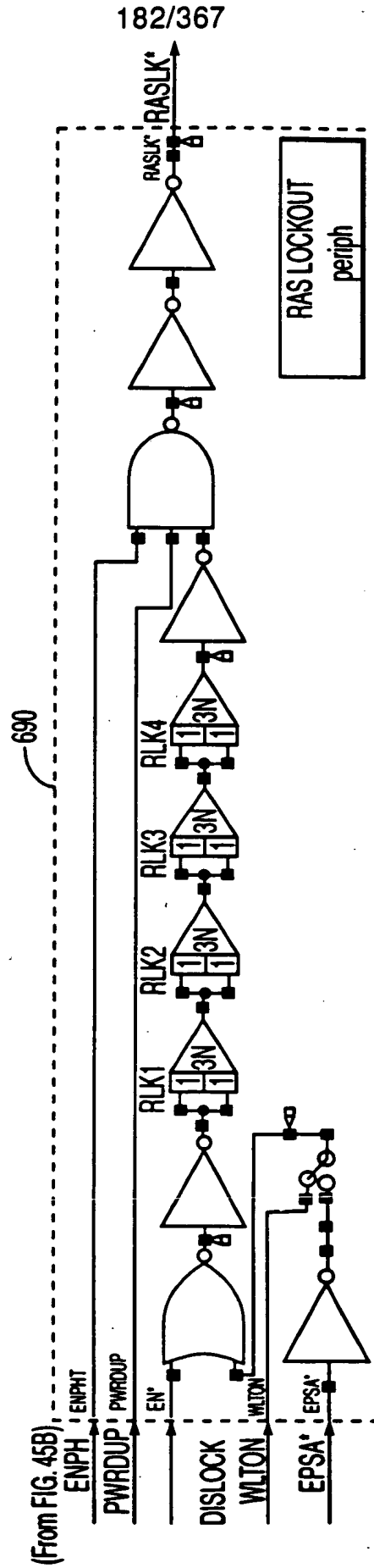


FIG. 45F

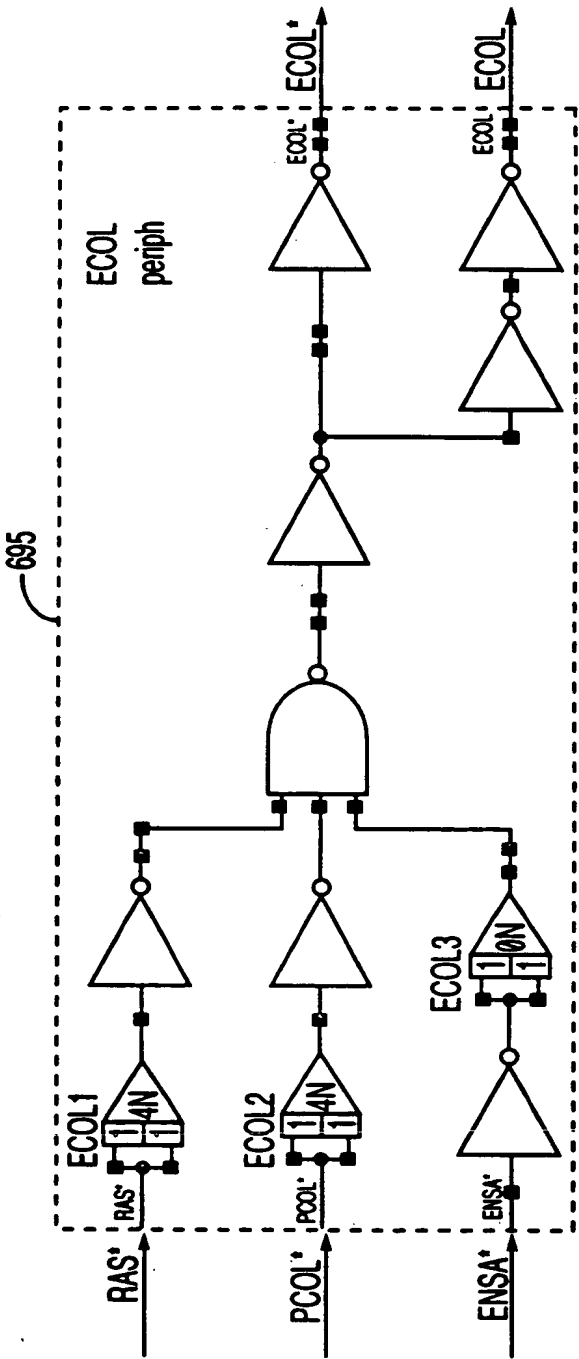


FIG. 45G

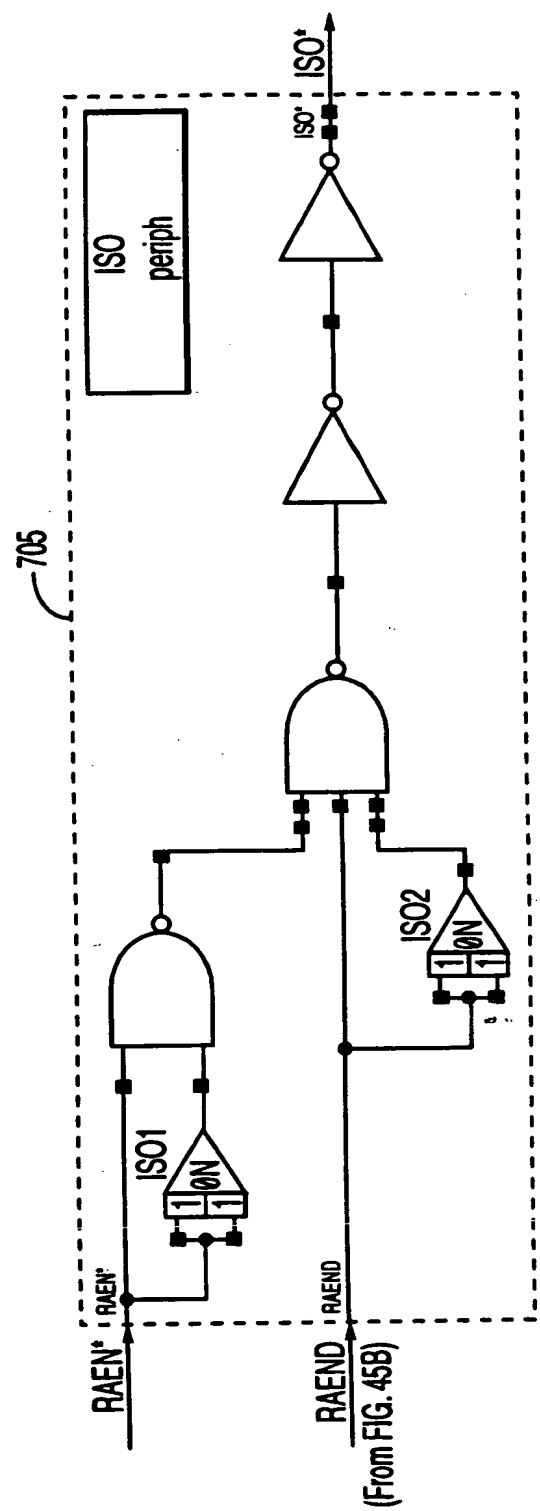


FIG. 45I

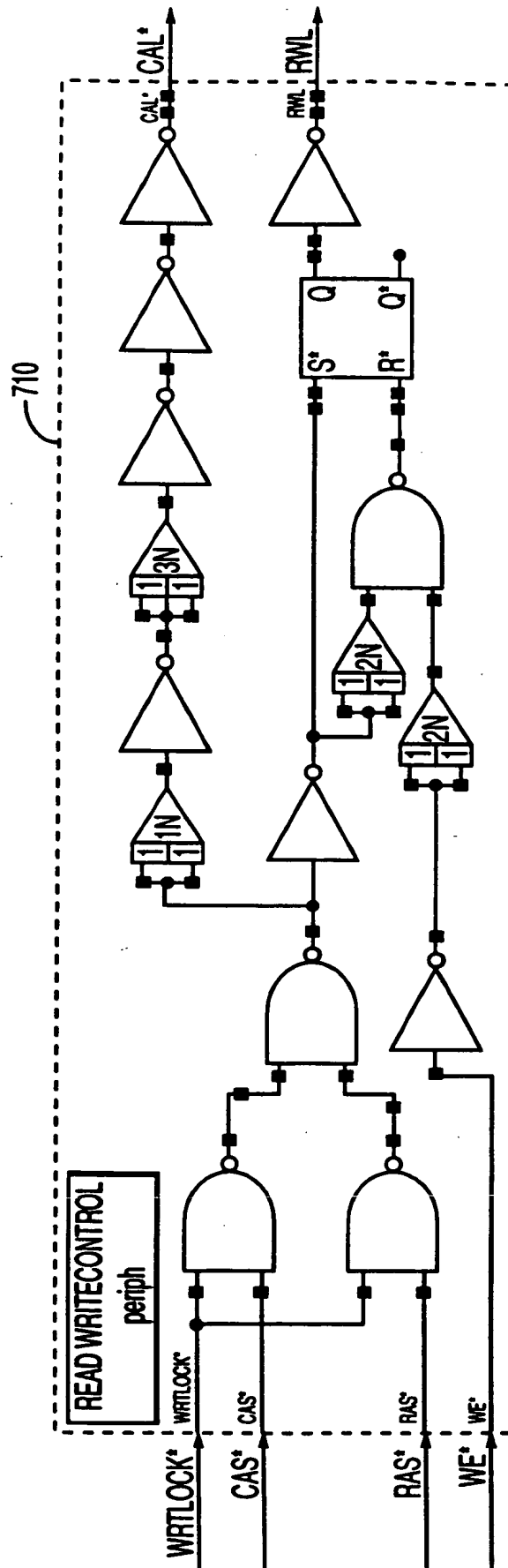


FIG. 45J

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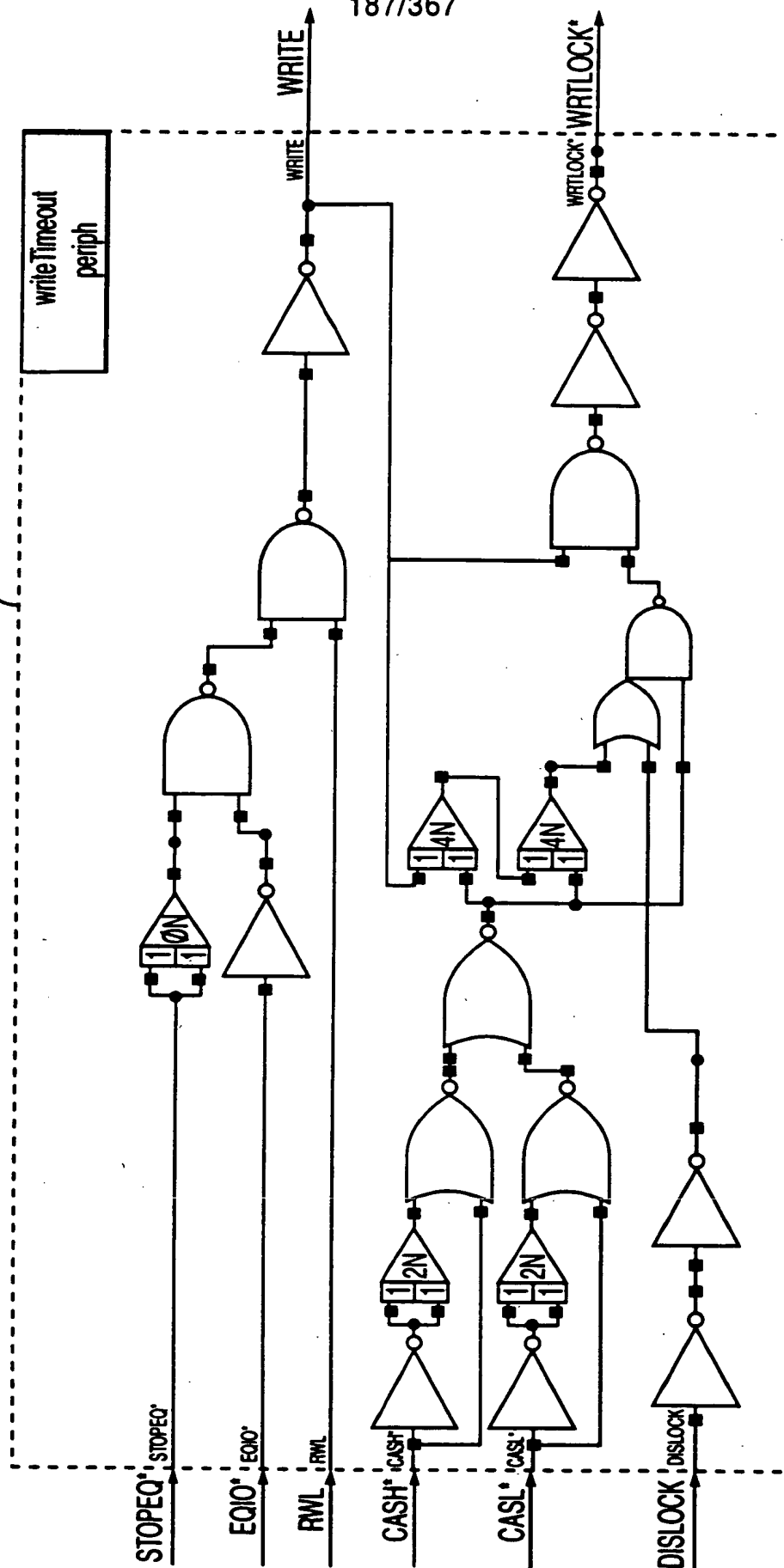


FIG. 45K

0000000000000000

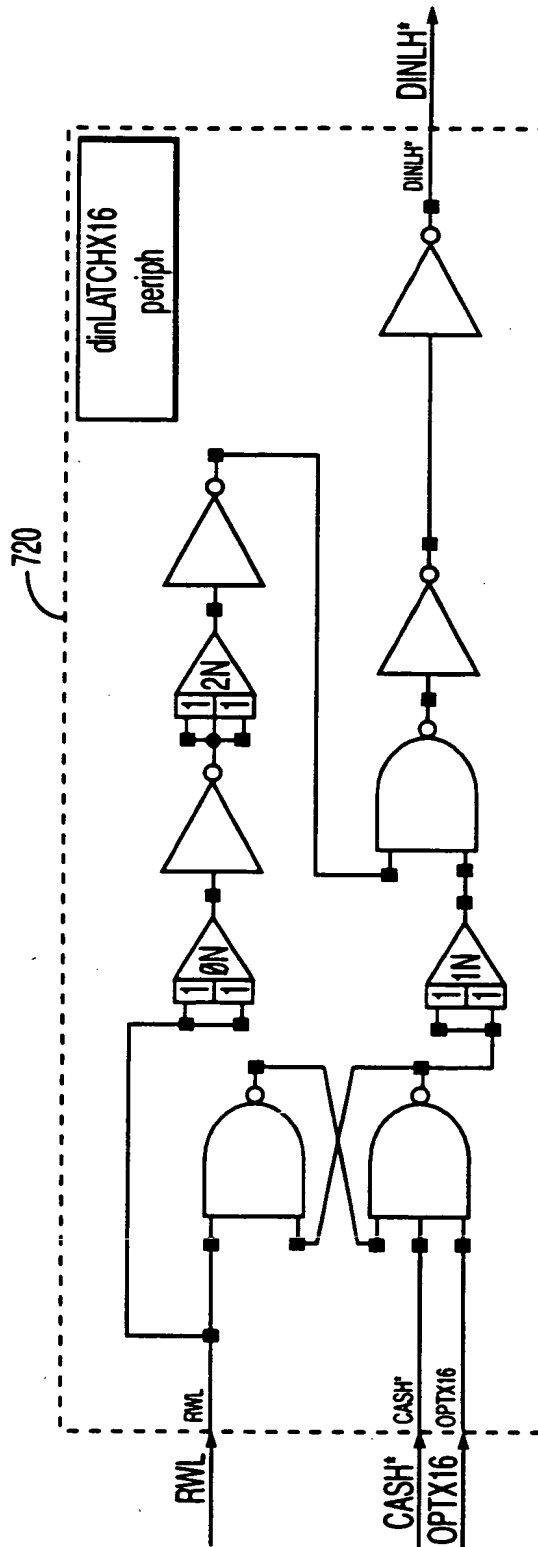


FIG. 45L

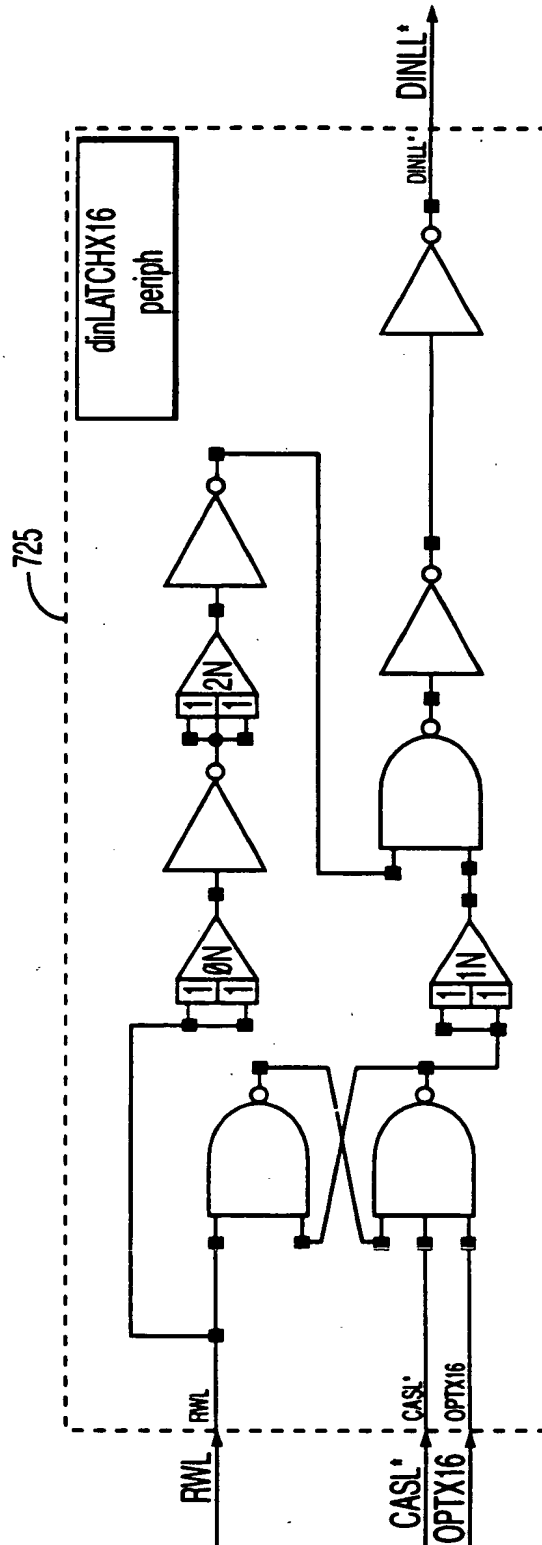


FIG. 45M

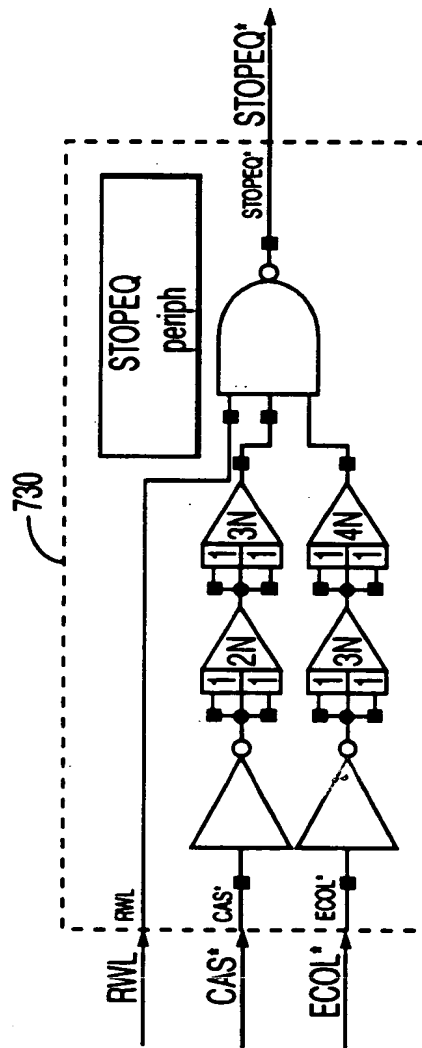


FIG. 45N

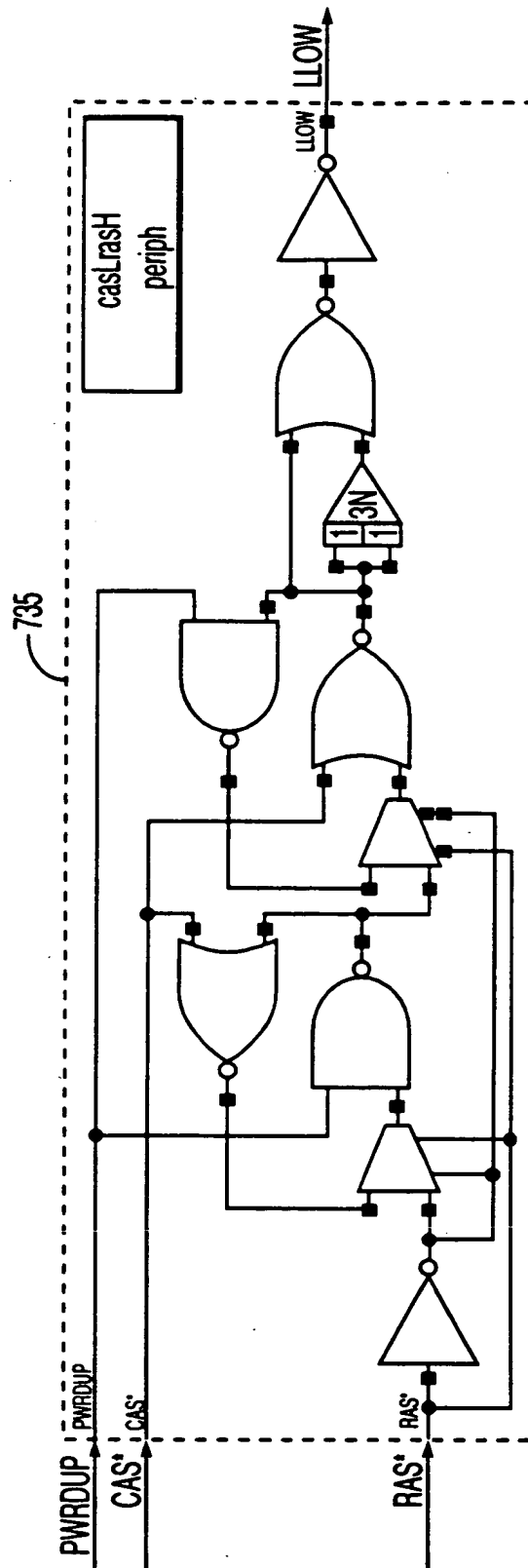


FIG. 450

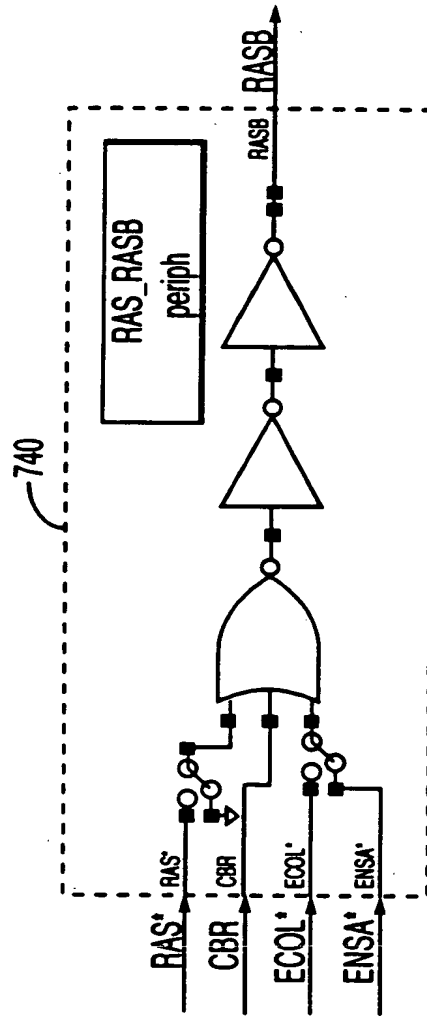


FIG. 45P

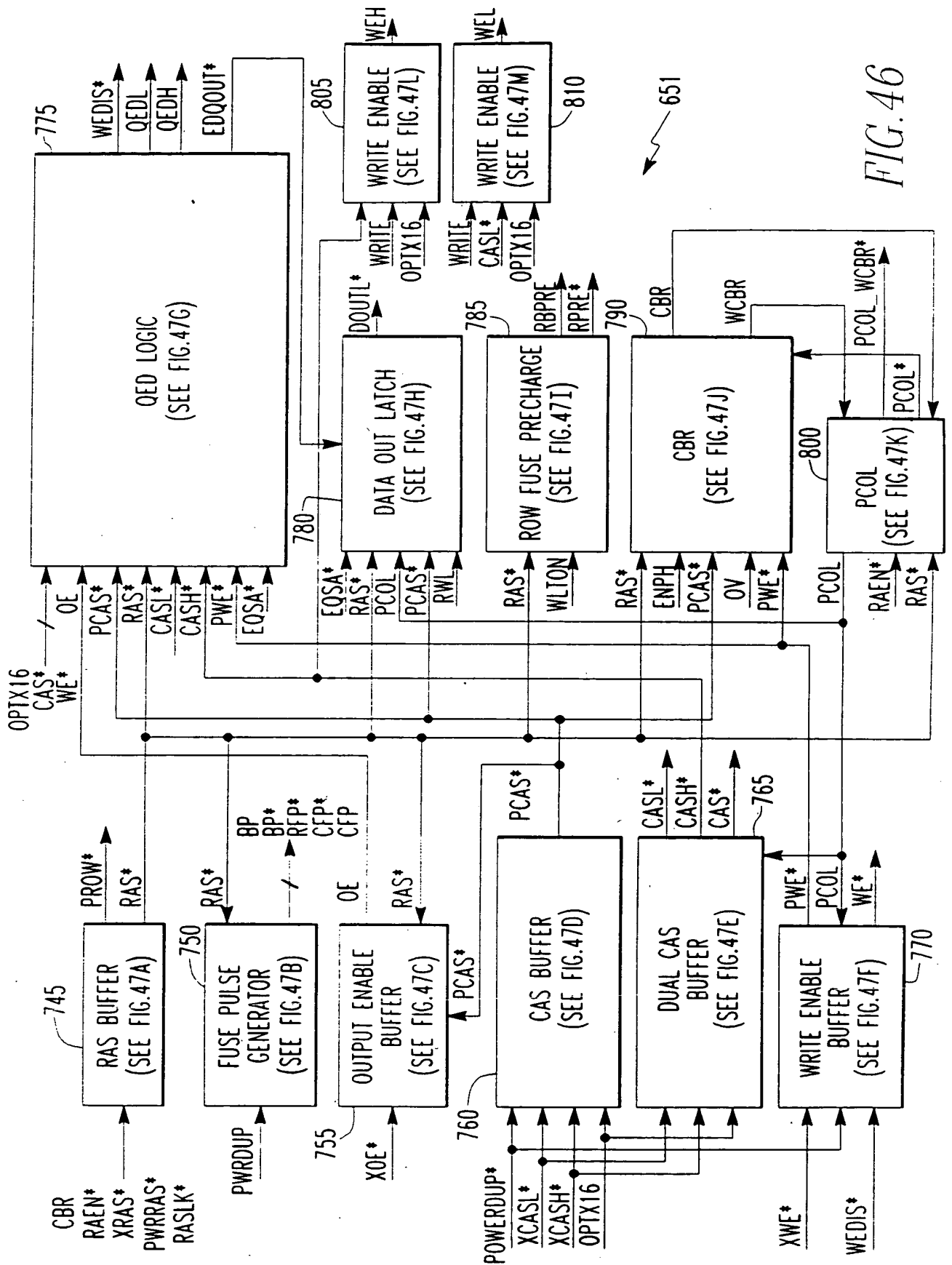


FIG. 46



FIG. 47A

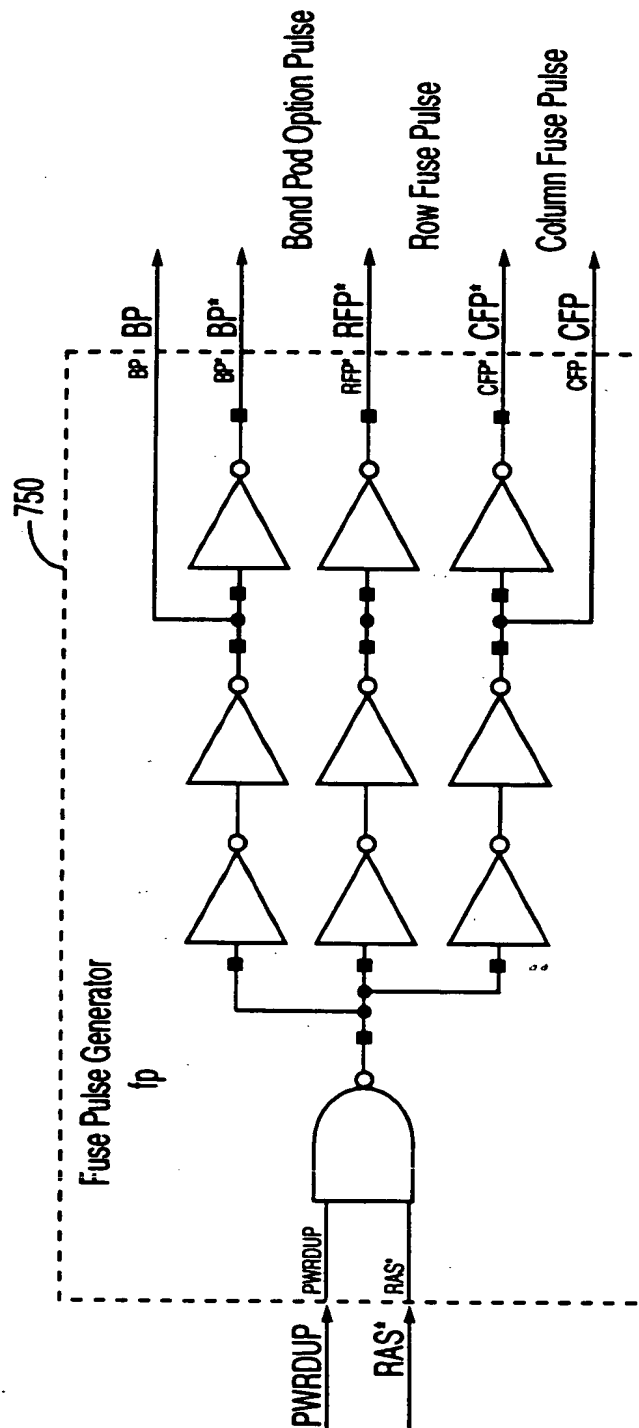
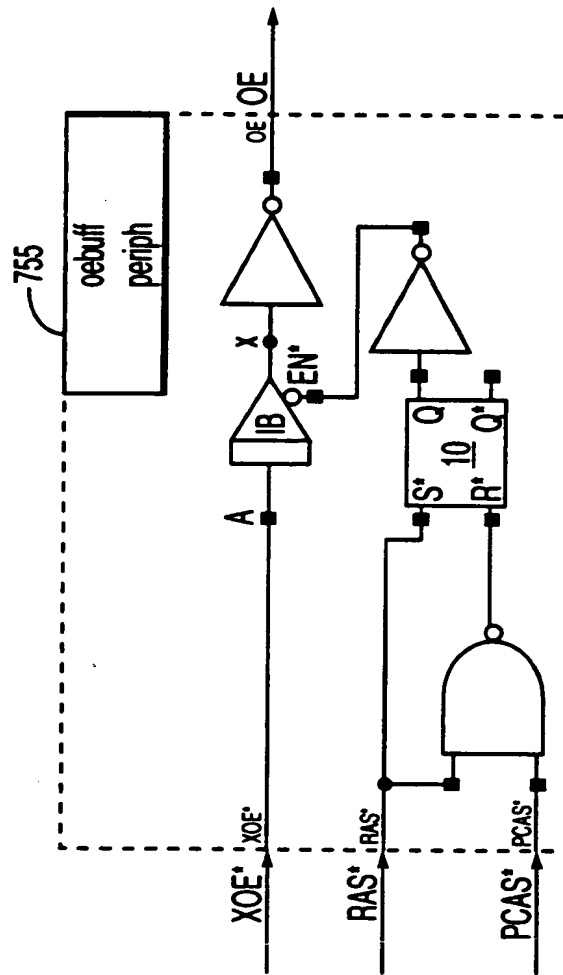


FIG. 47B



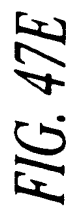


FIG. 47E

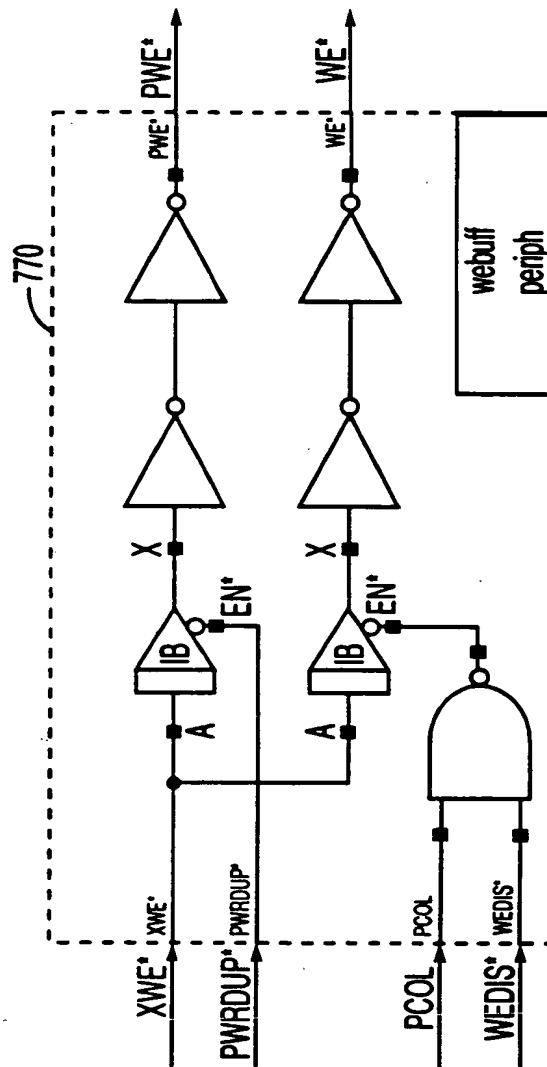


FIG. 47F

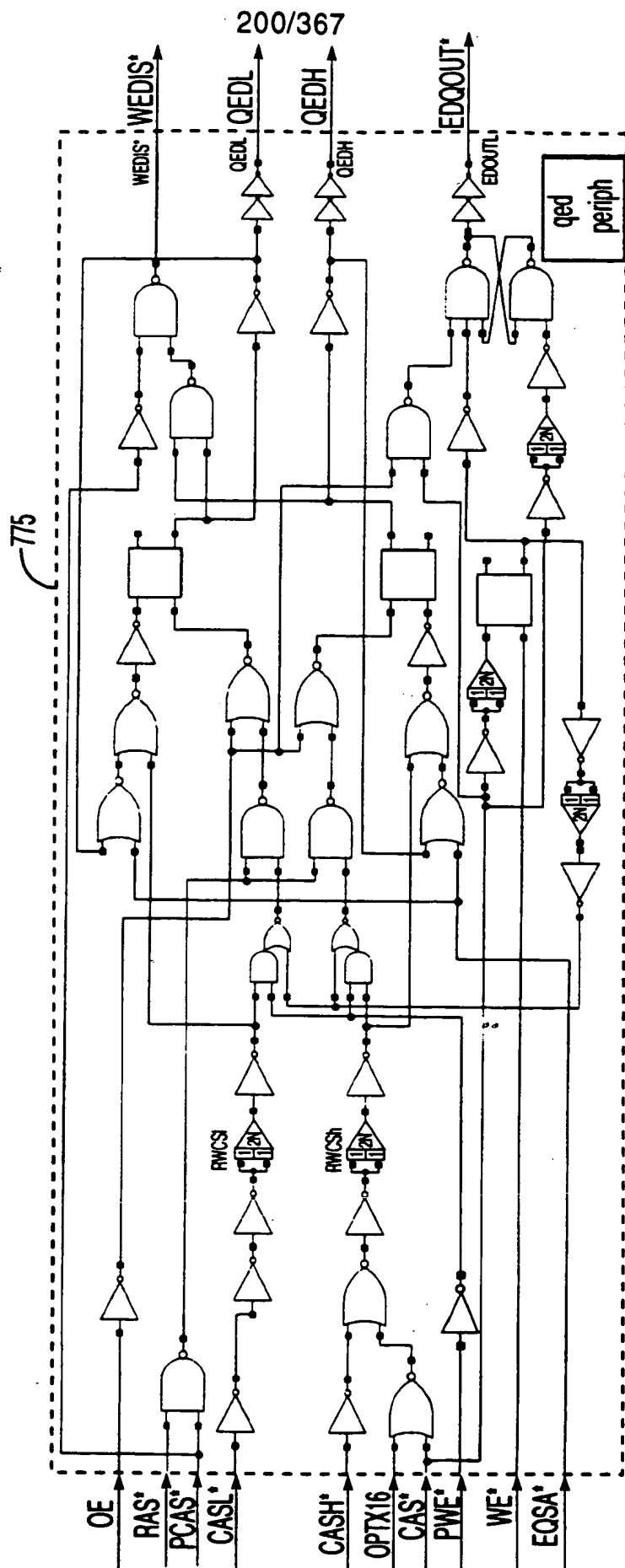


FIG. 47G

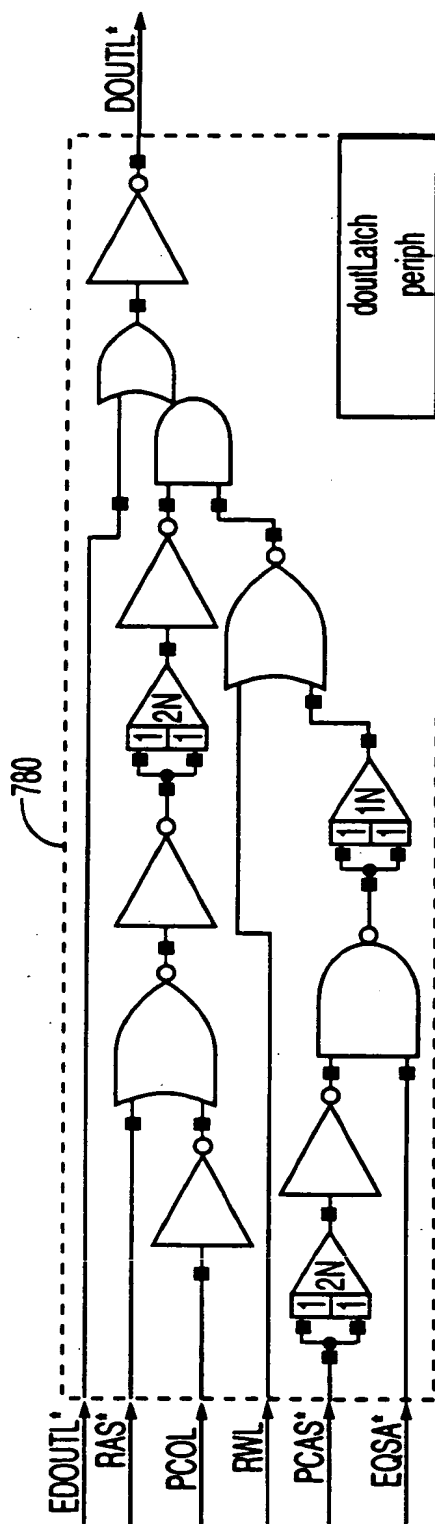


FIG. 47H

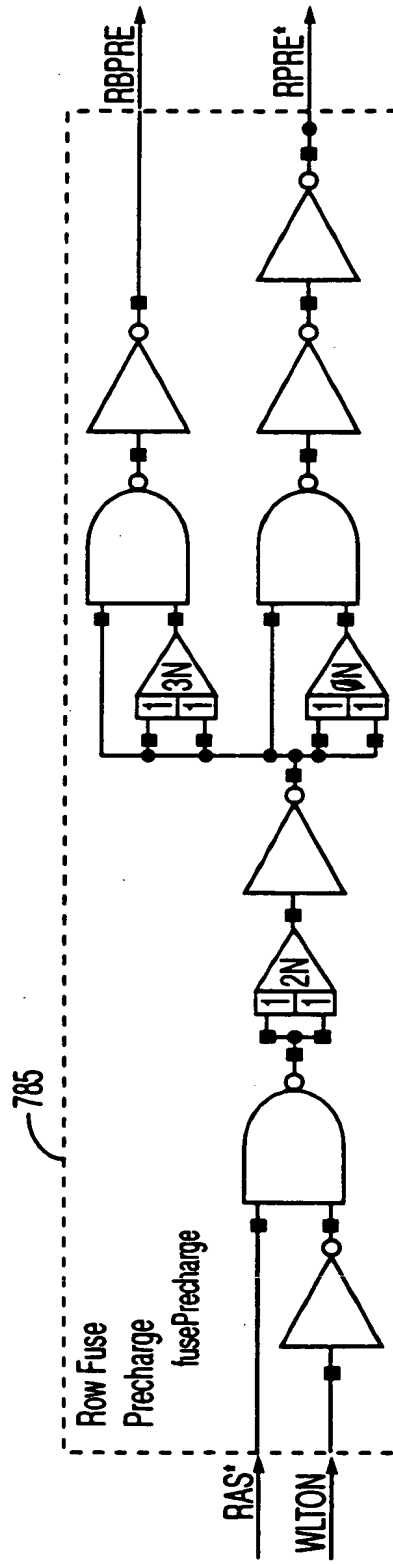


FIG. 471

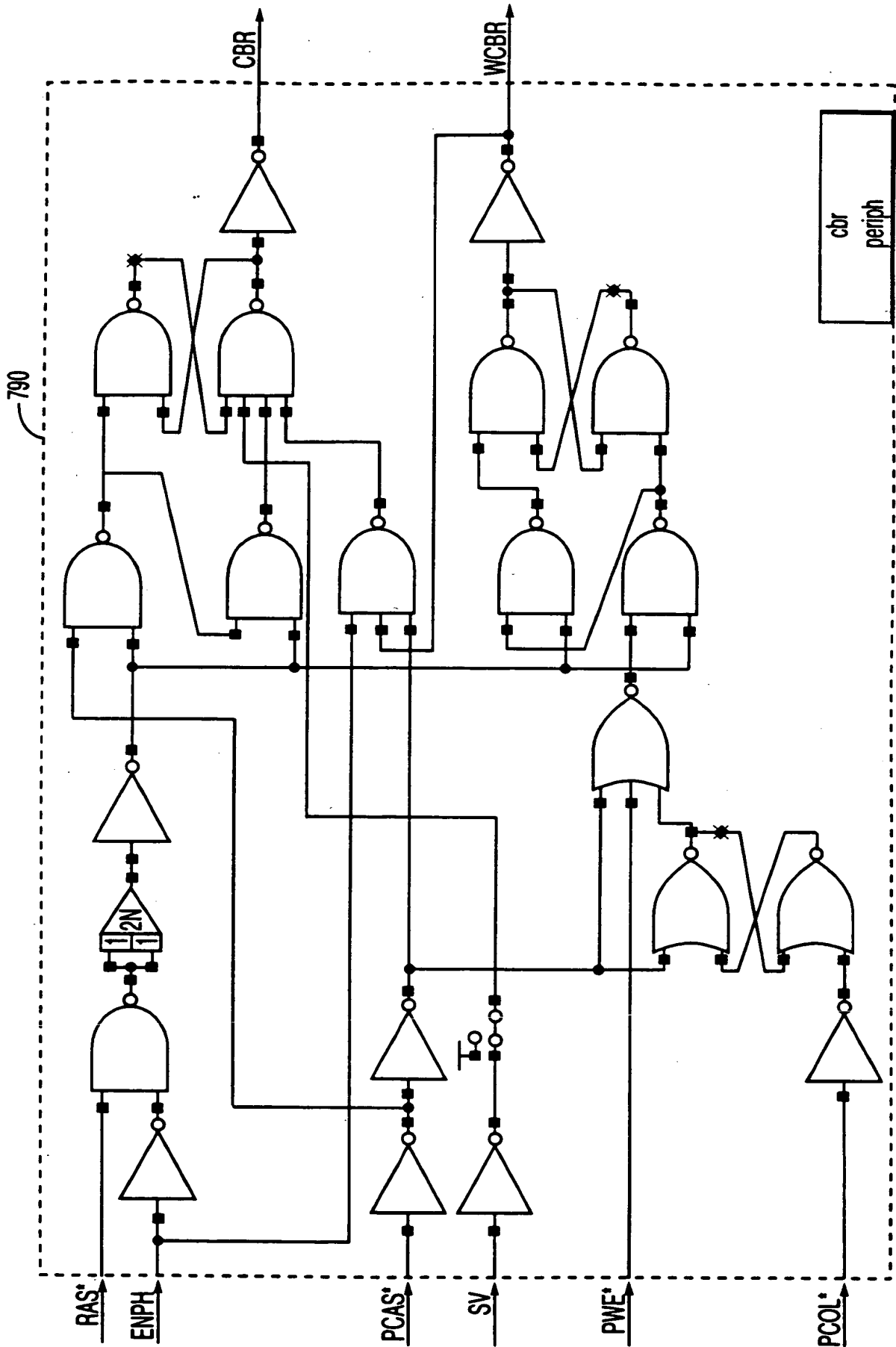


FIG. 47J

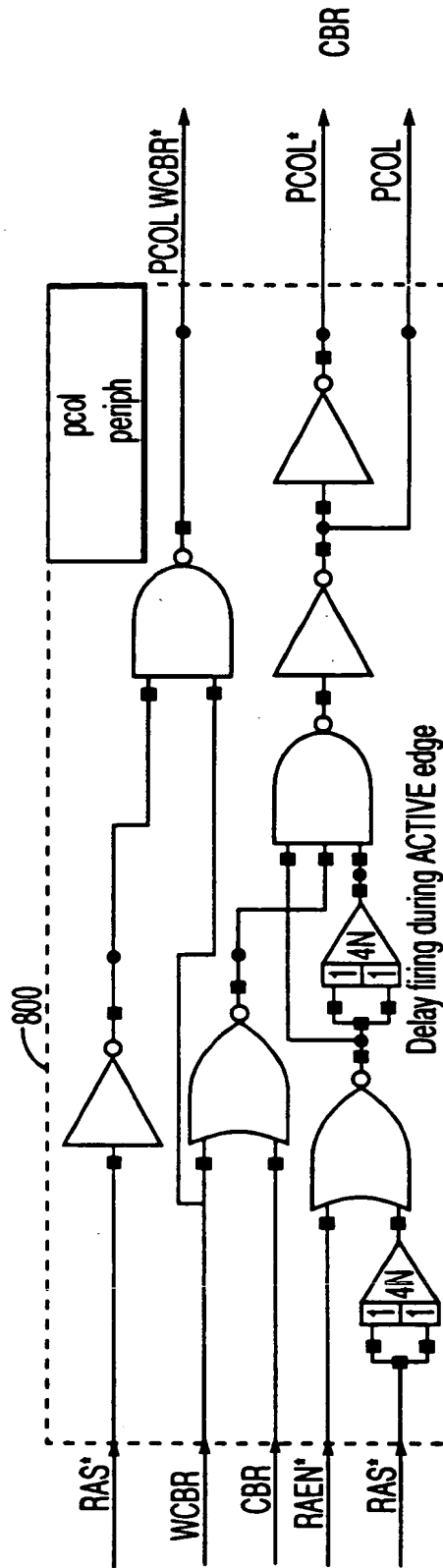


FIG. 47K

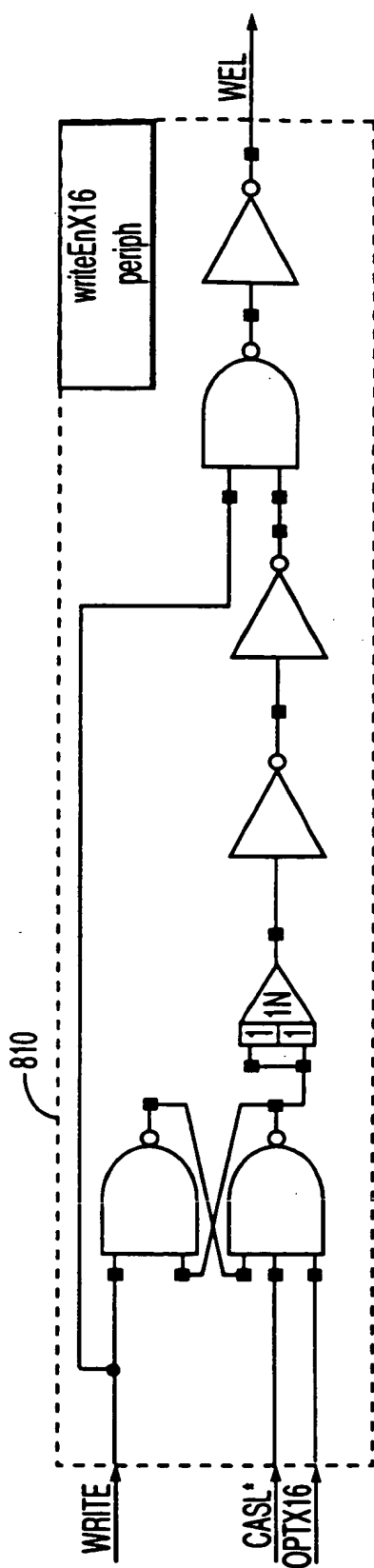


FIG. 47M

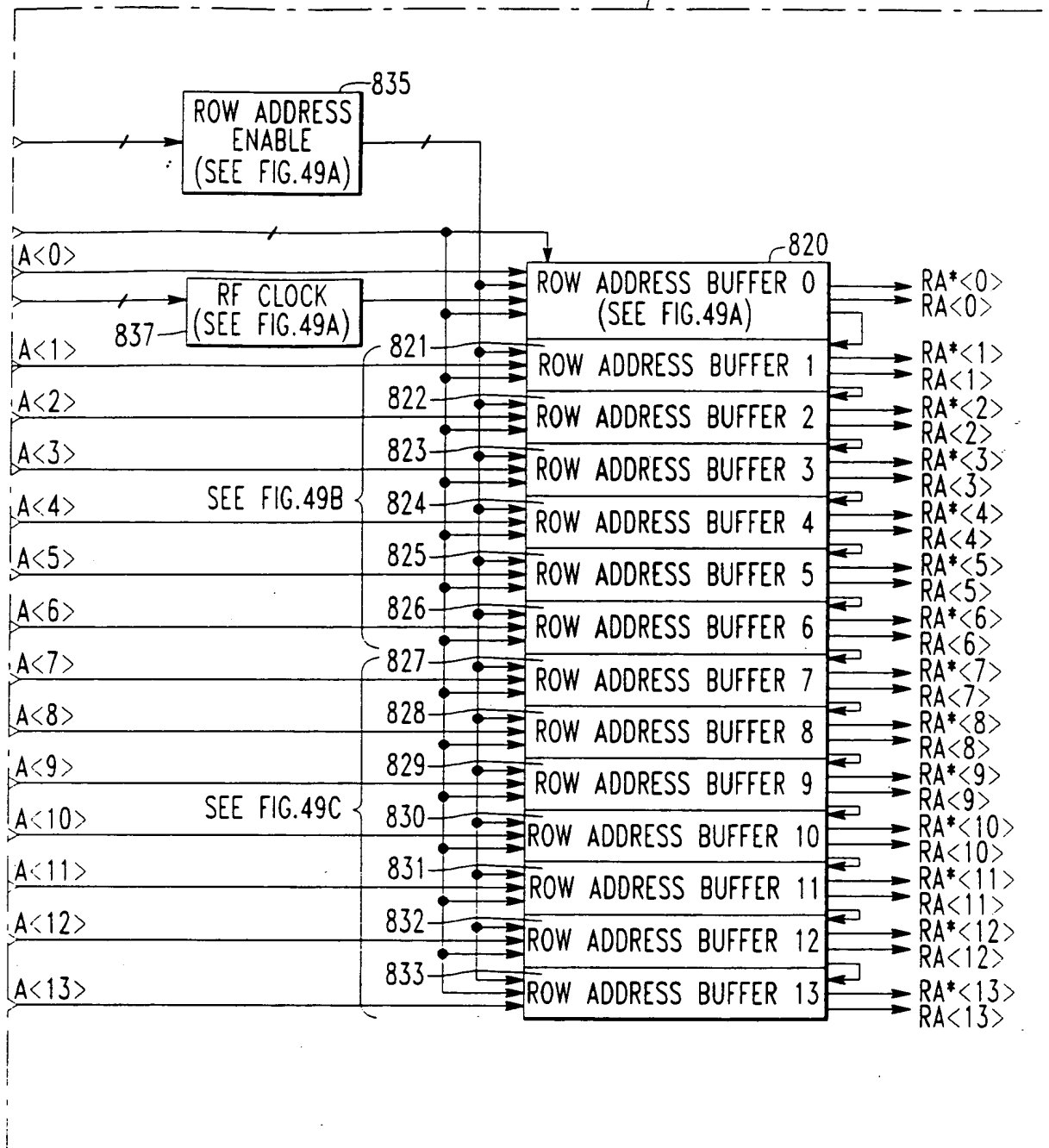


FIG. 48A

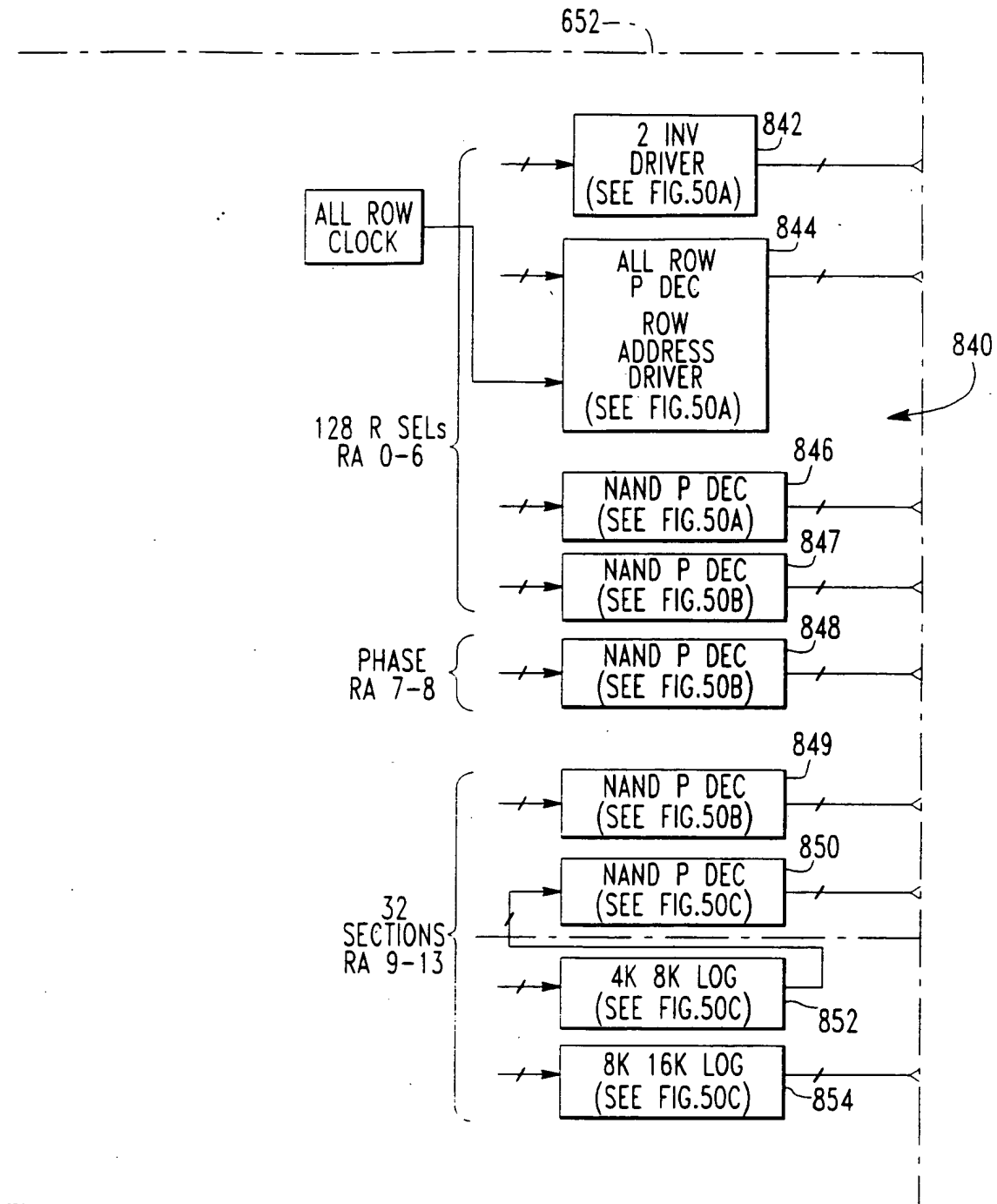


FIG. 48B

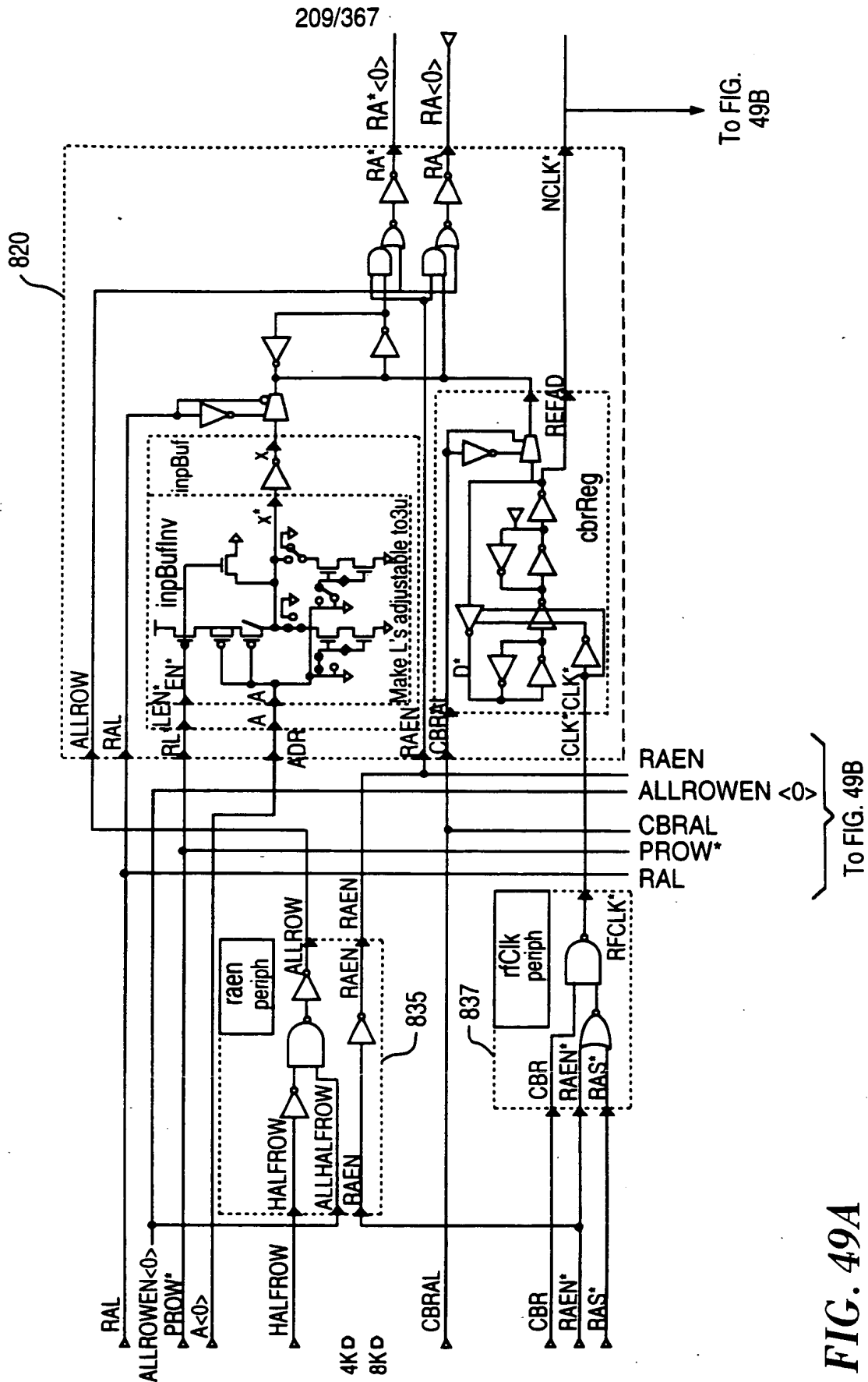


FIG. 49A

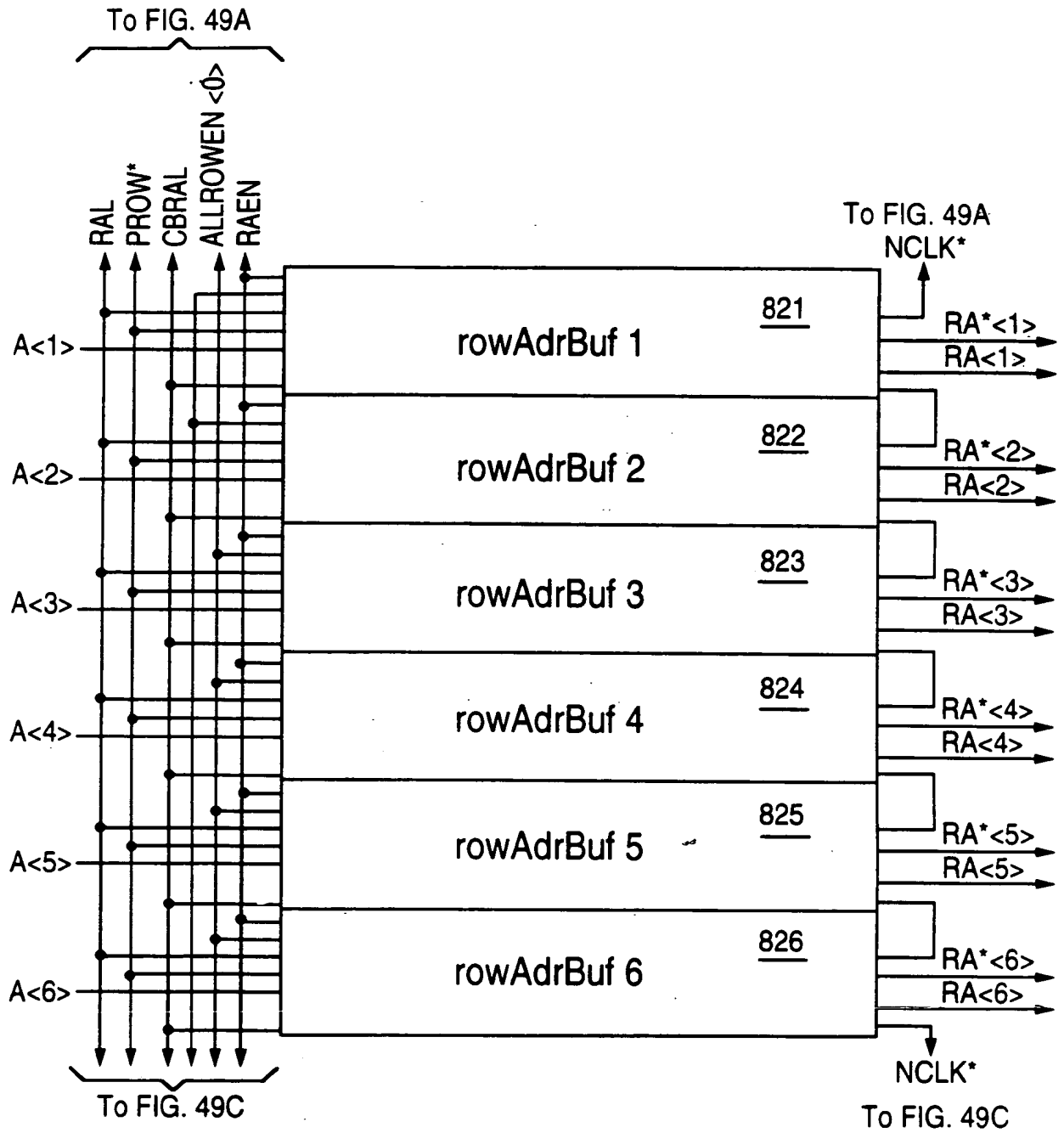


FIG. 49B

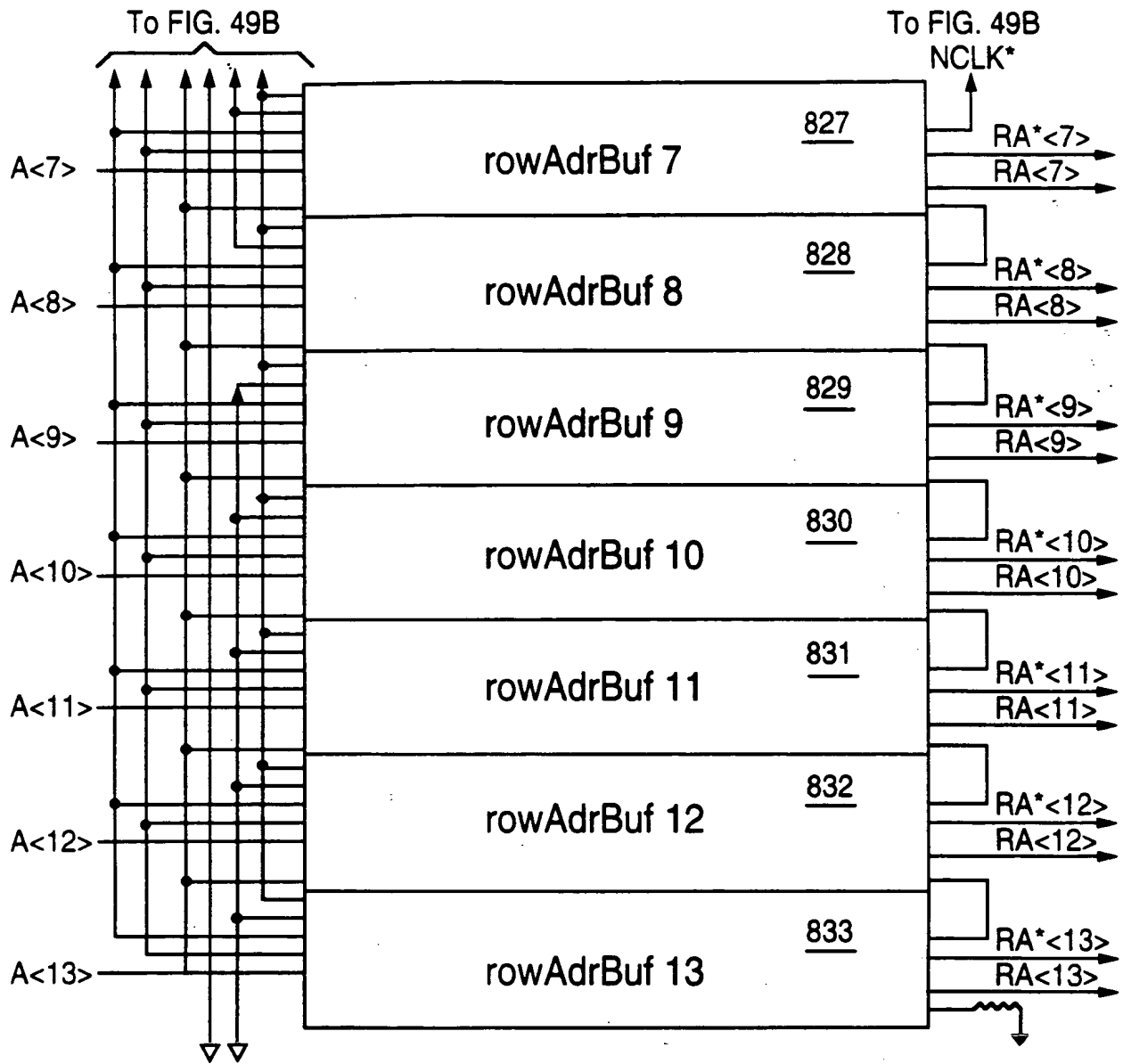


FIG. 49C

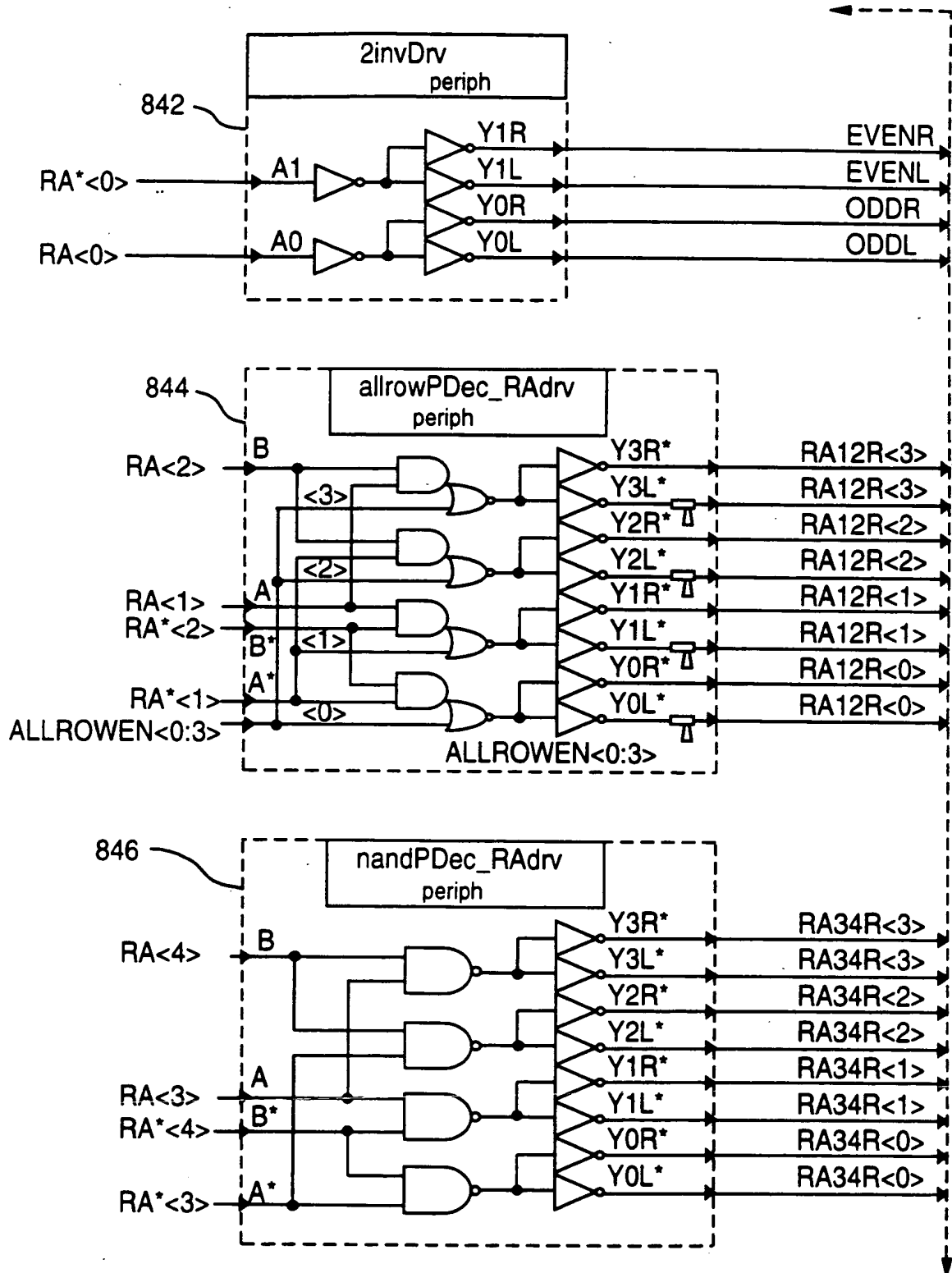
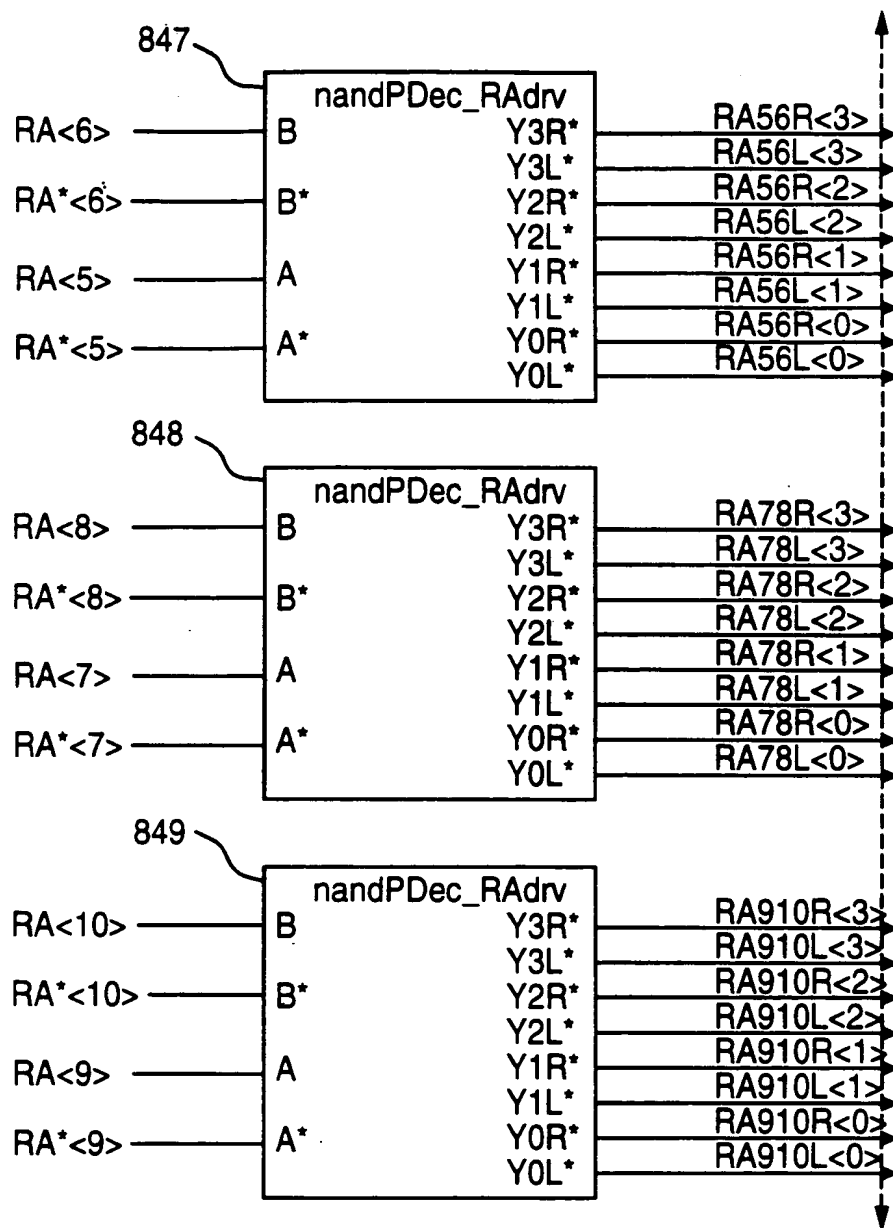


FIG. 50A

**FIG. 50B**

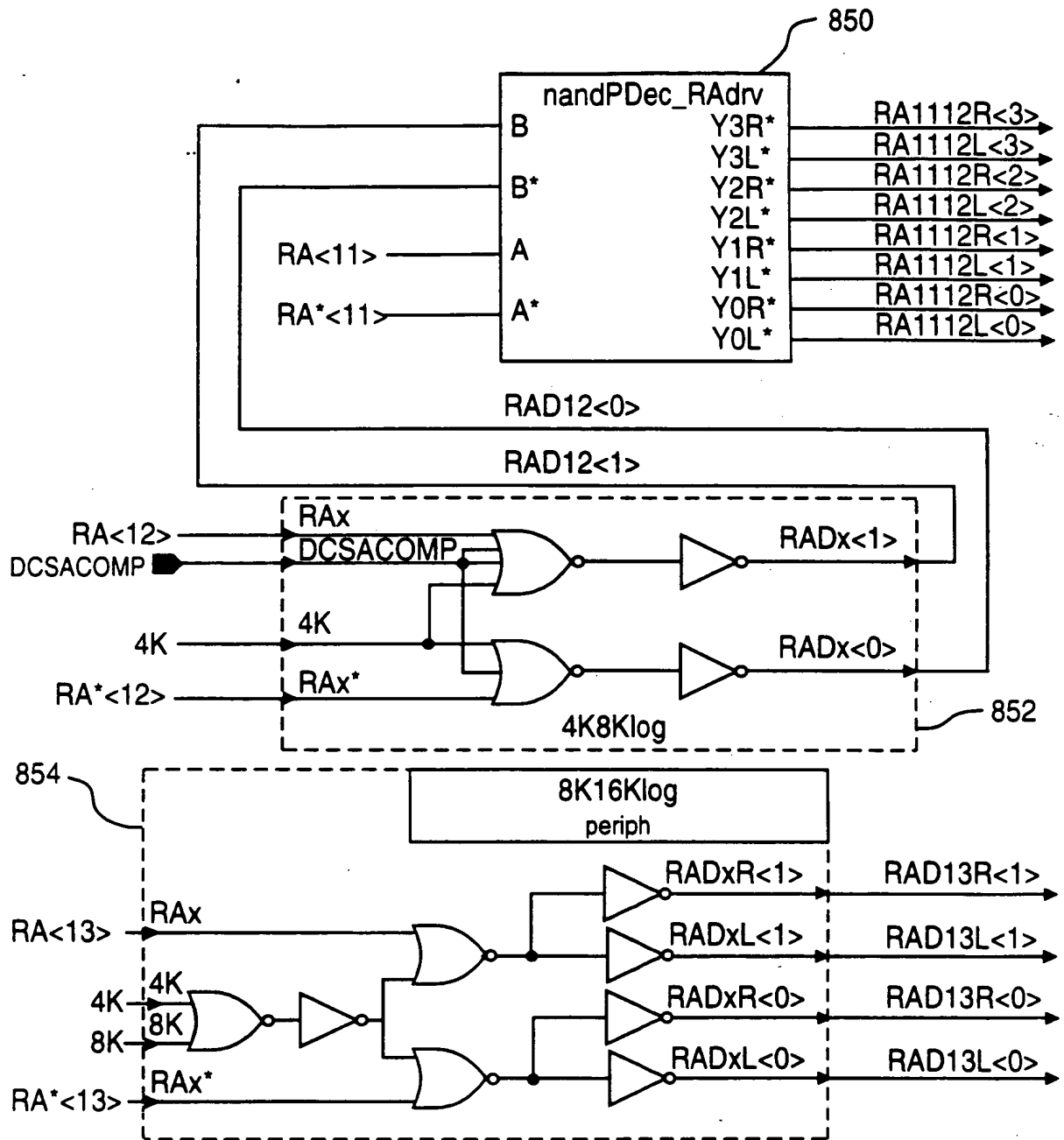


FIG. 50C

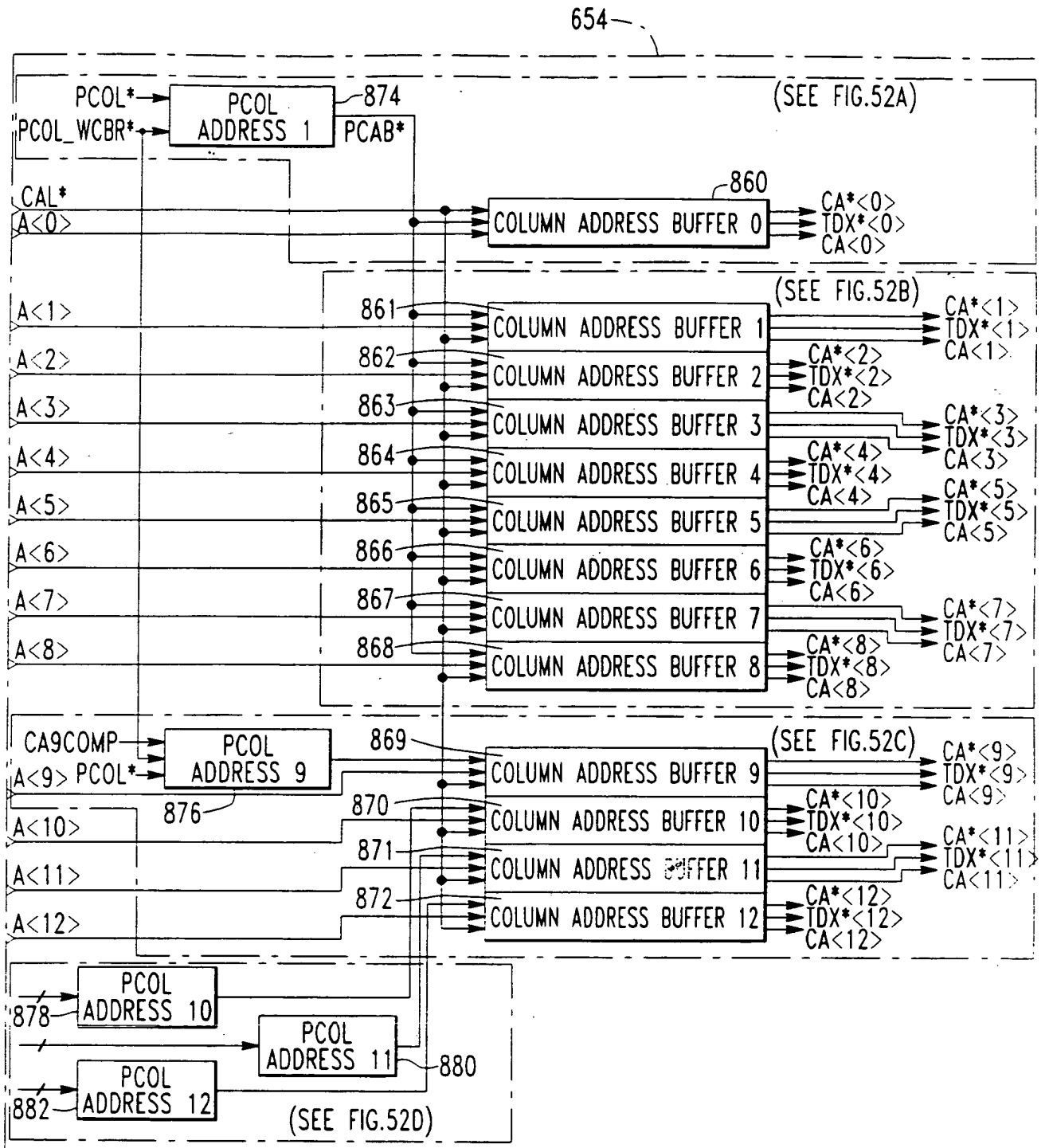


FIG. 51A

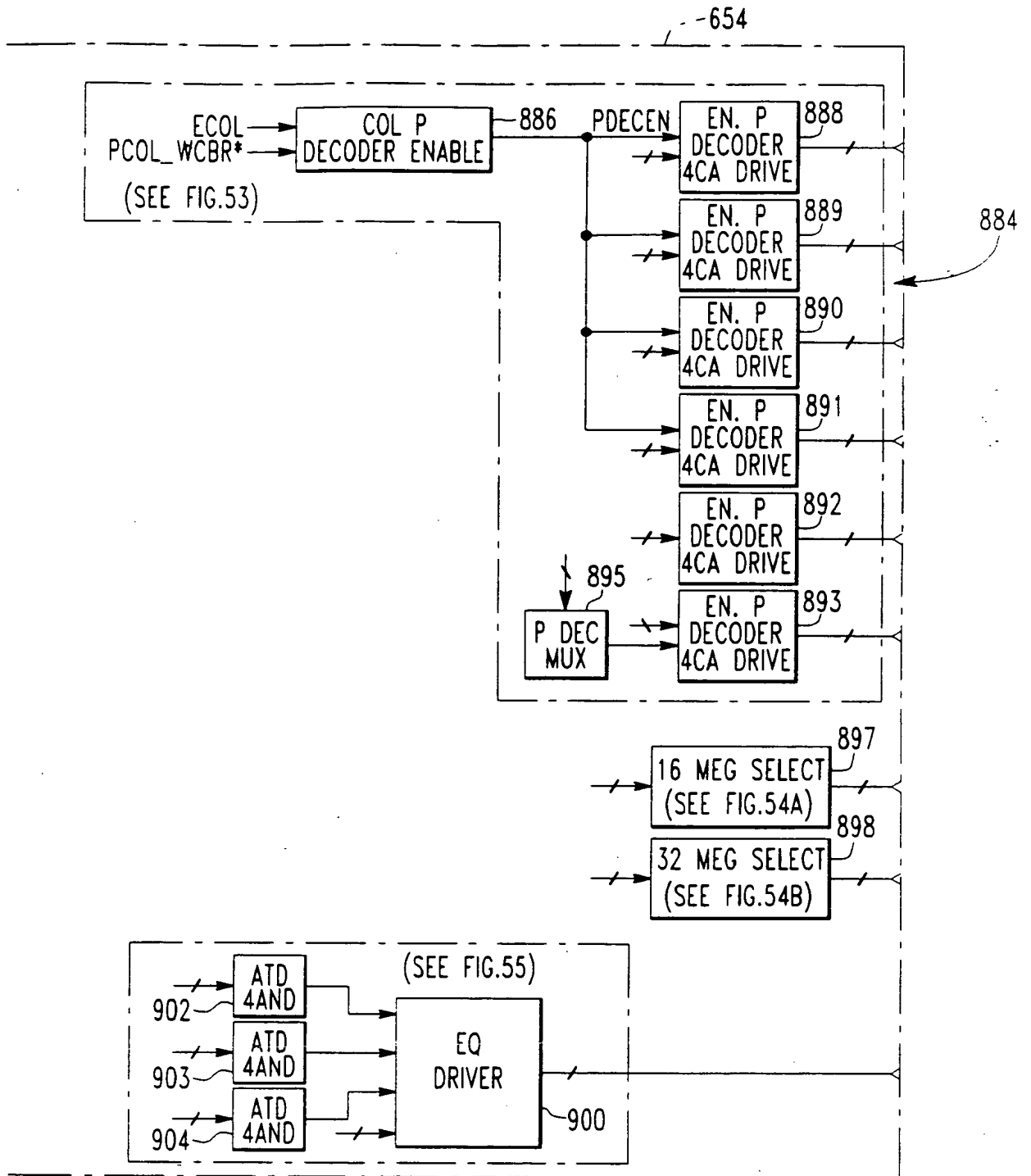


FIG. 51B

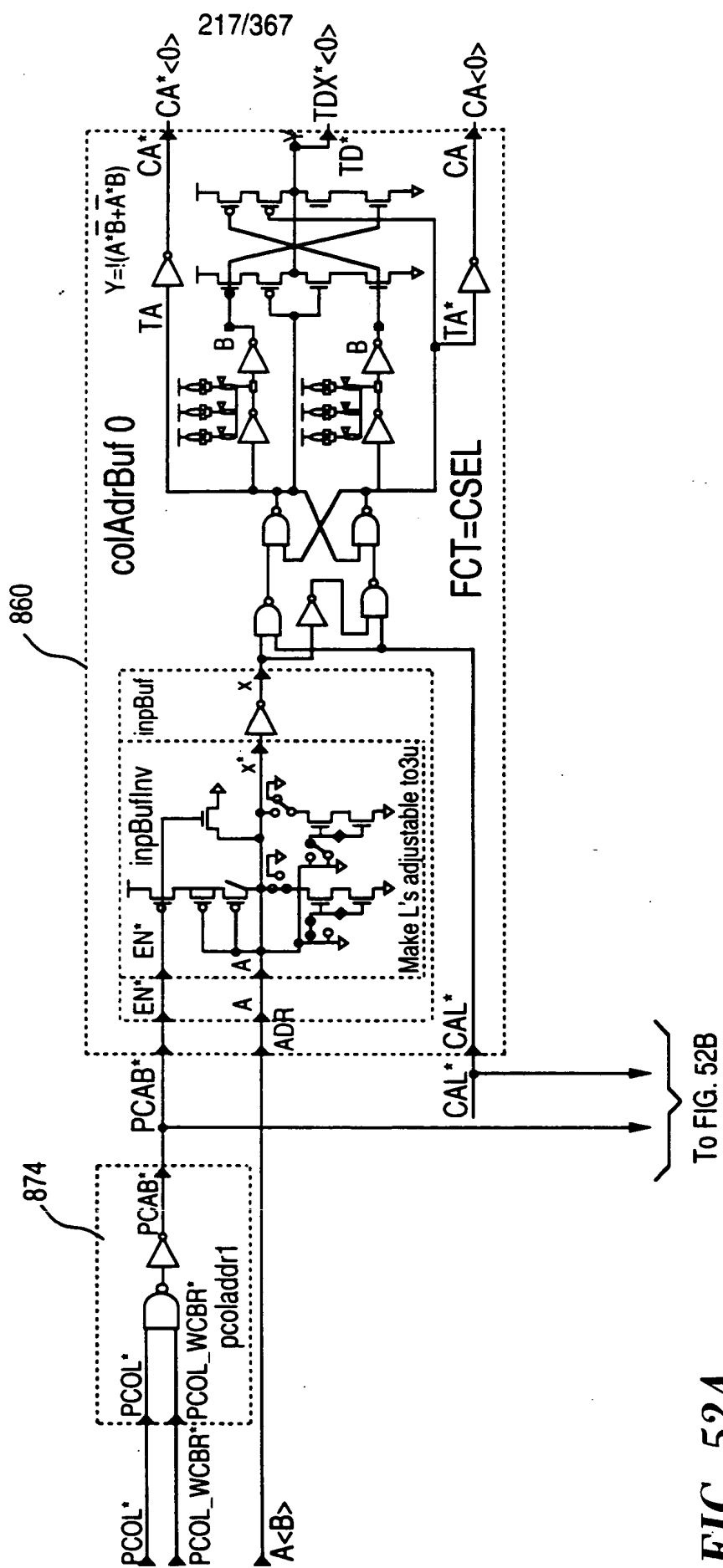


FIG. 52A

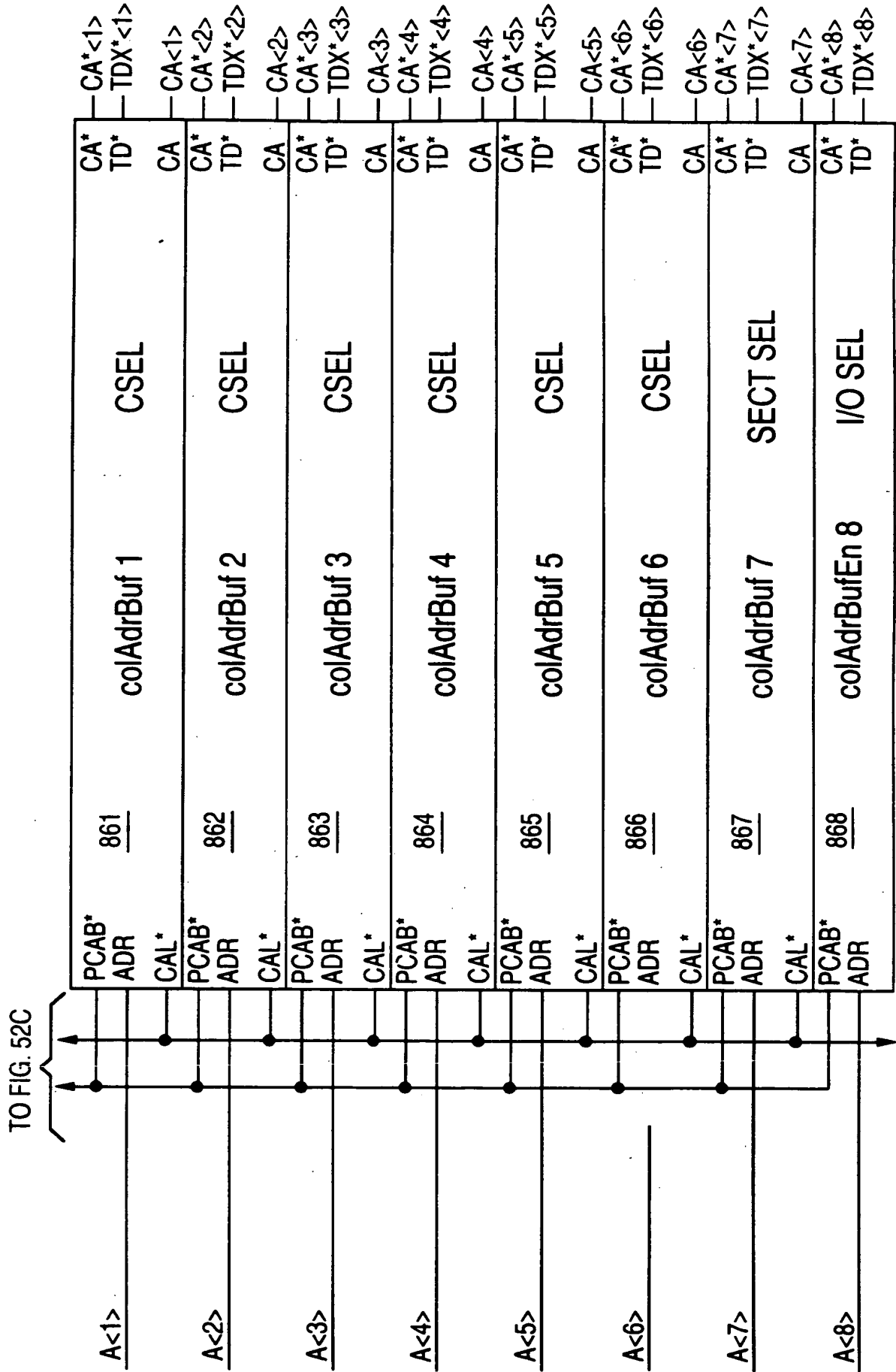


FIG. 52B

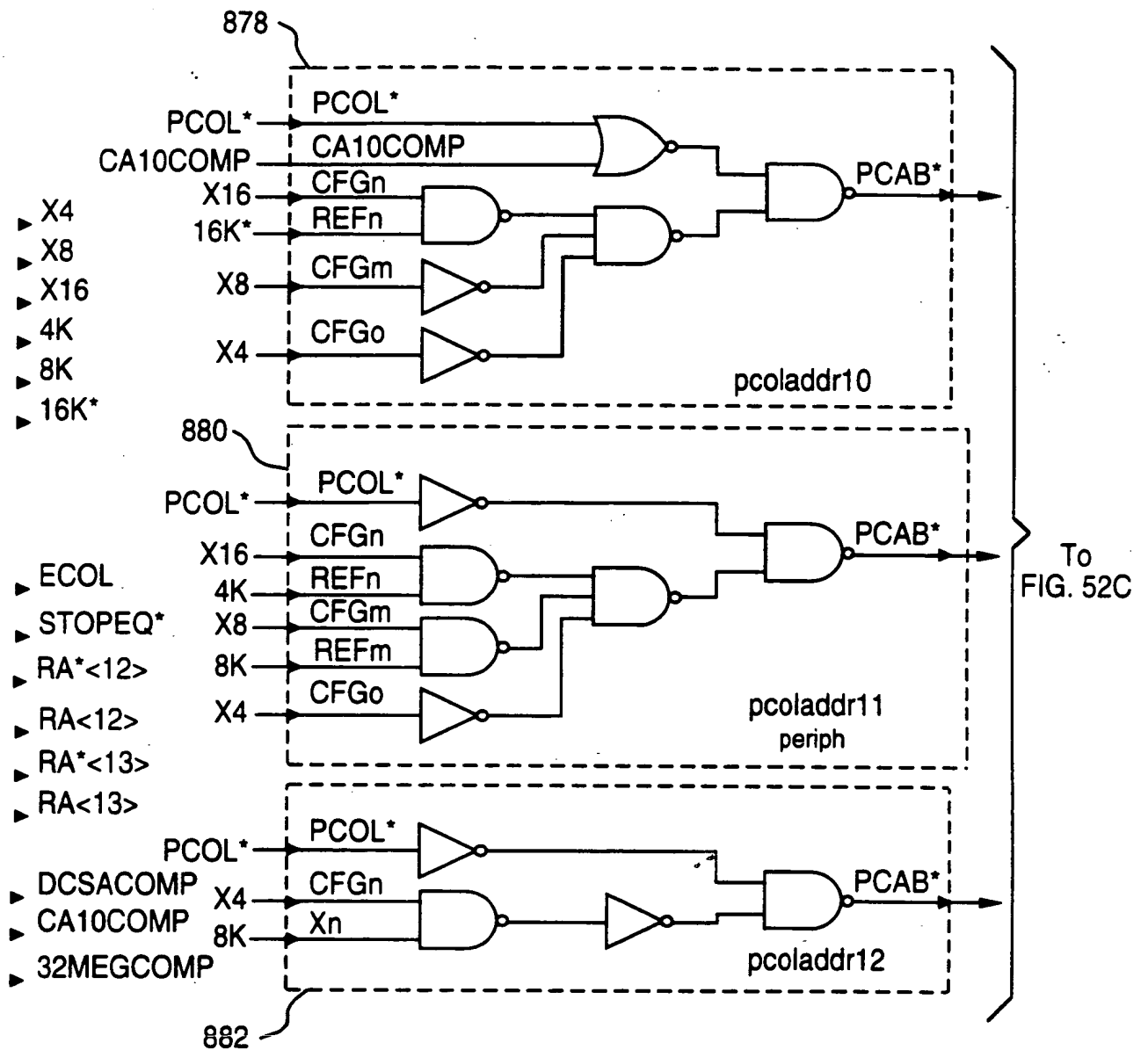


FIG. 52D

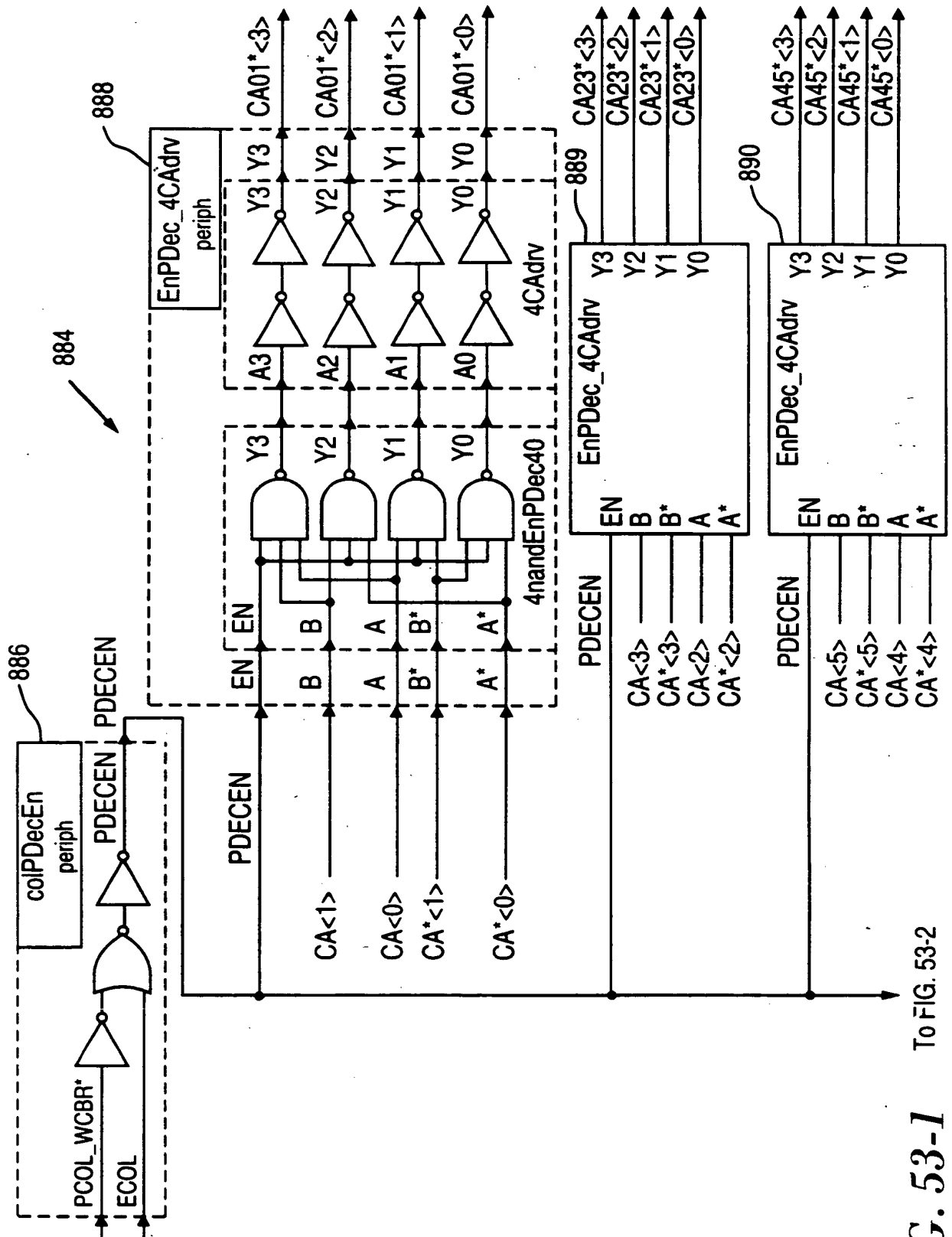


FIG. 53-1

To FIG. 53-1

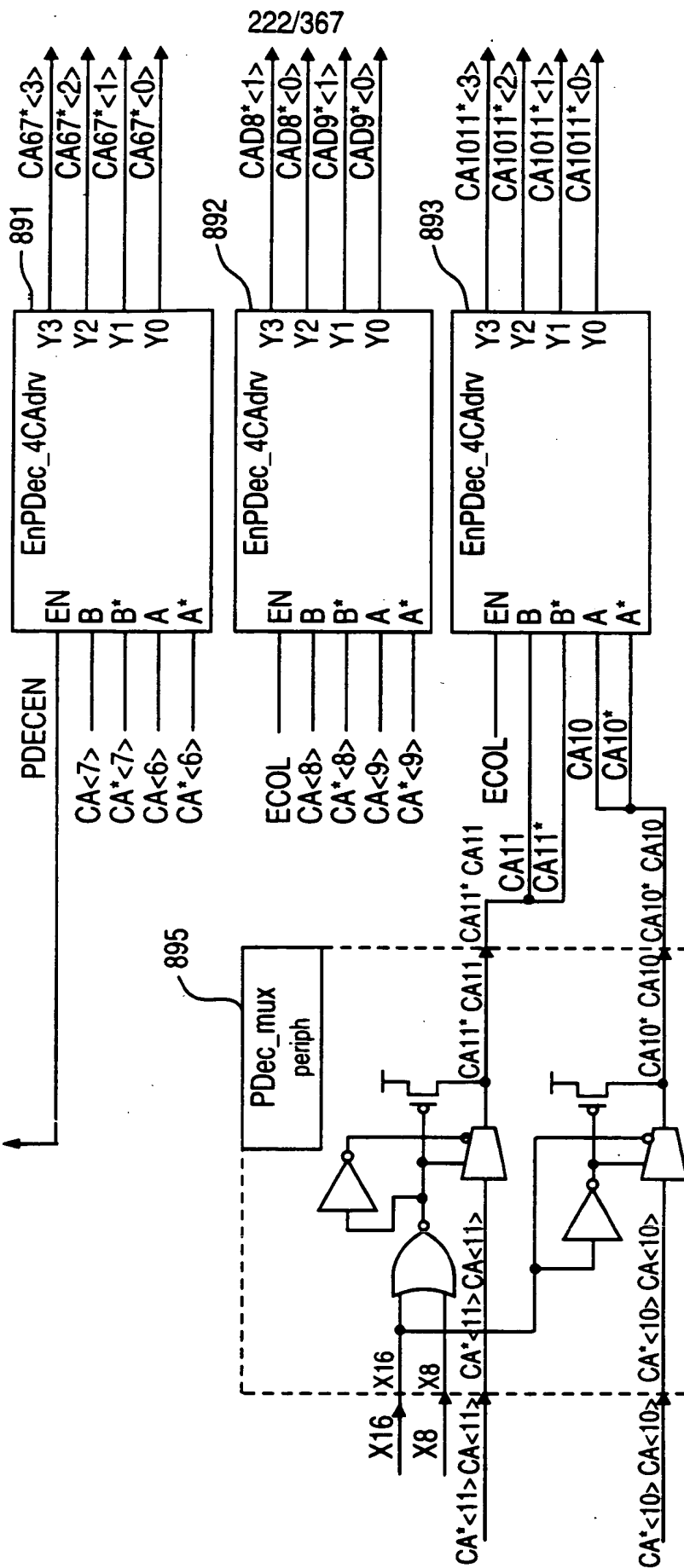
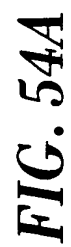


FIG. 53-2



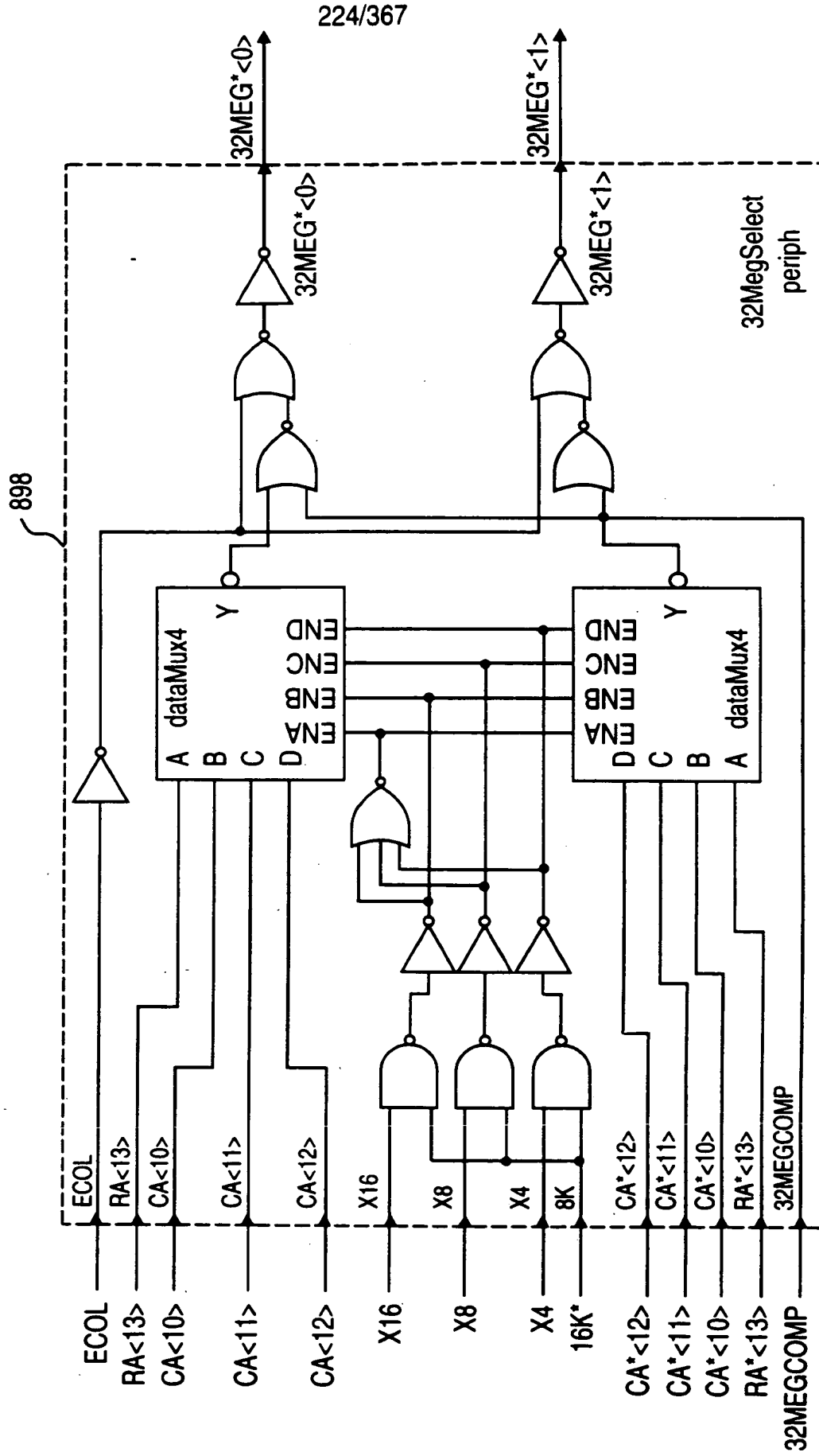


FIG. 54B

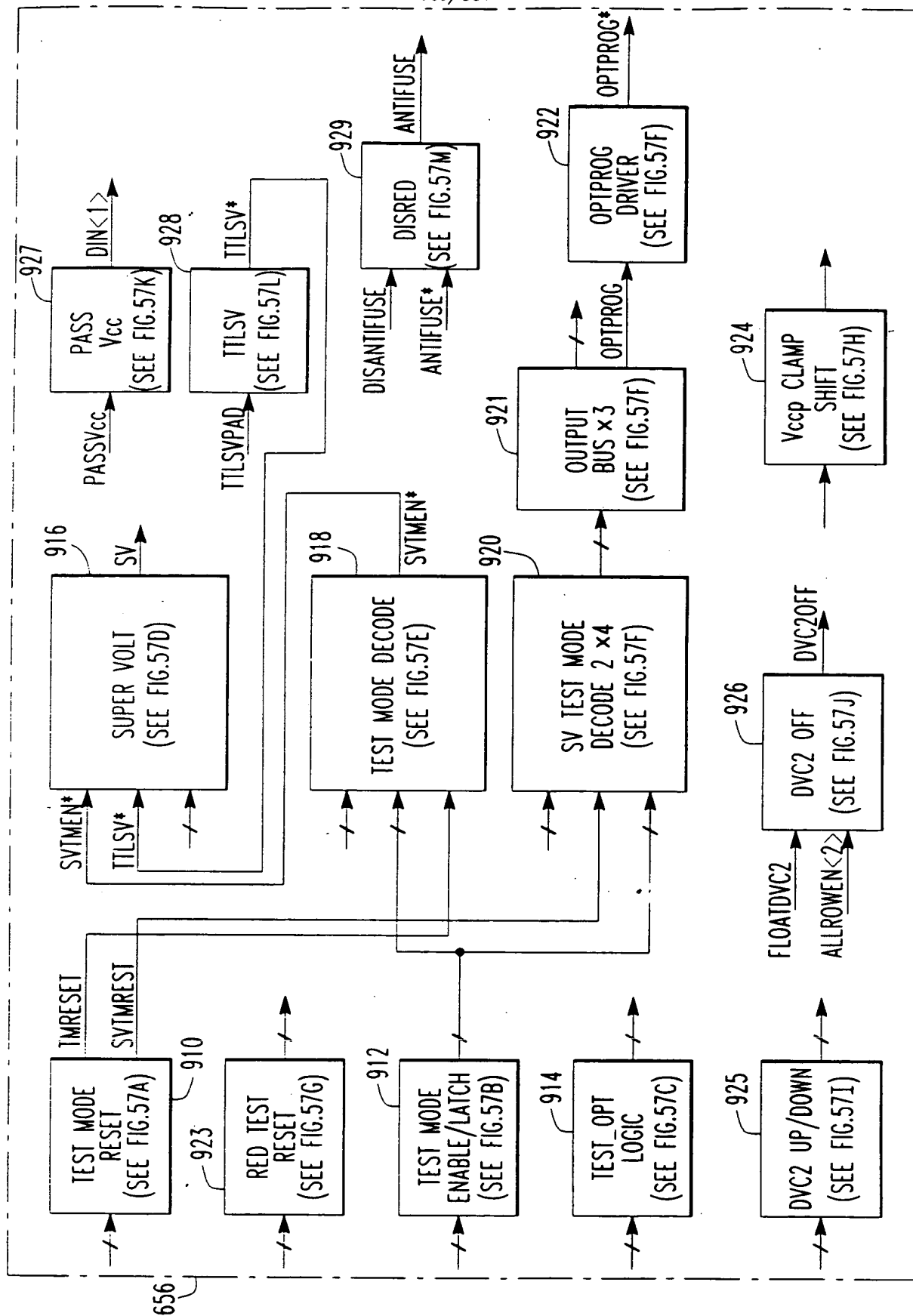


FIG. 56

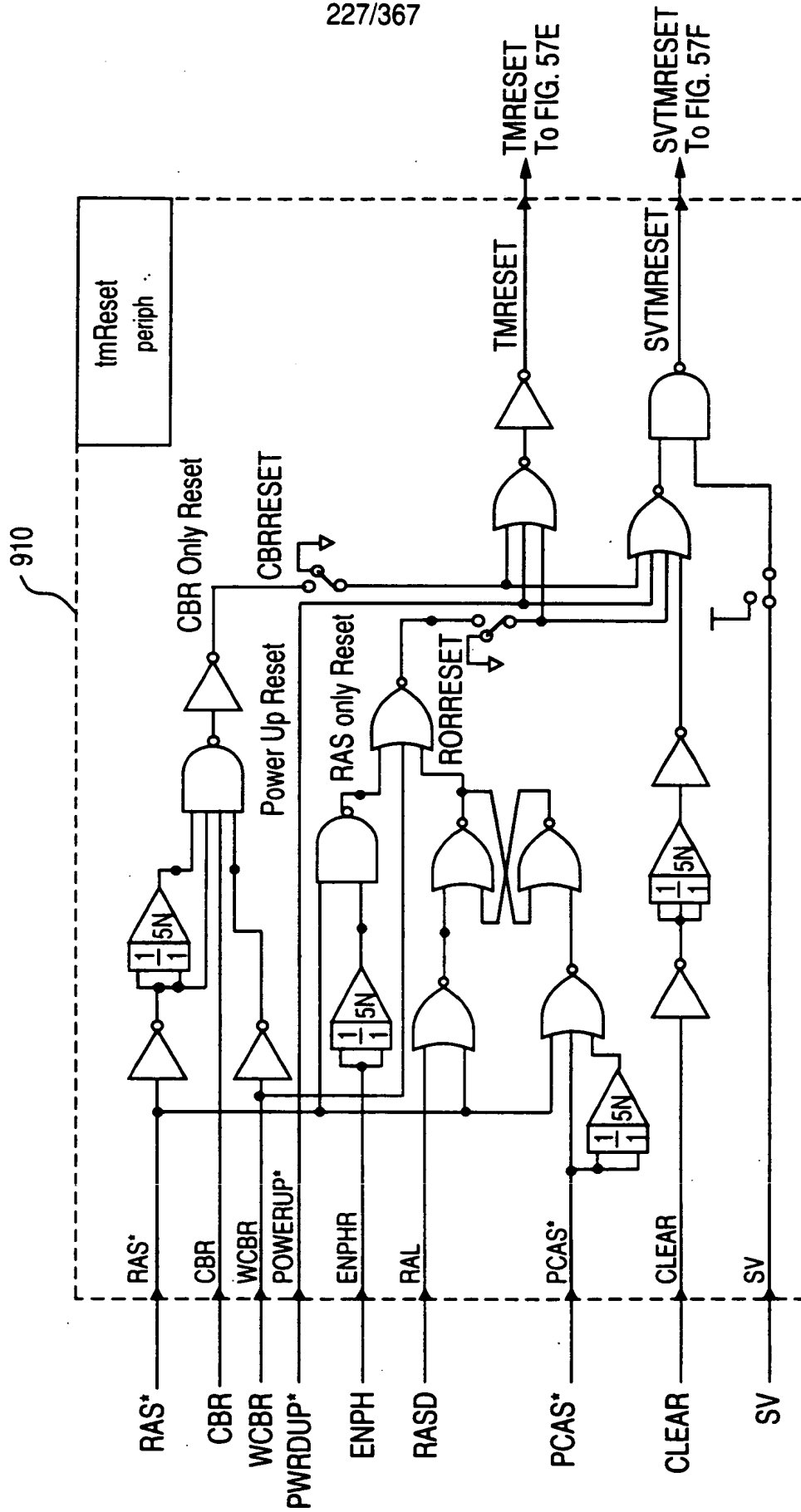


FIG. 57A

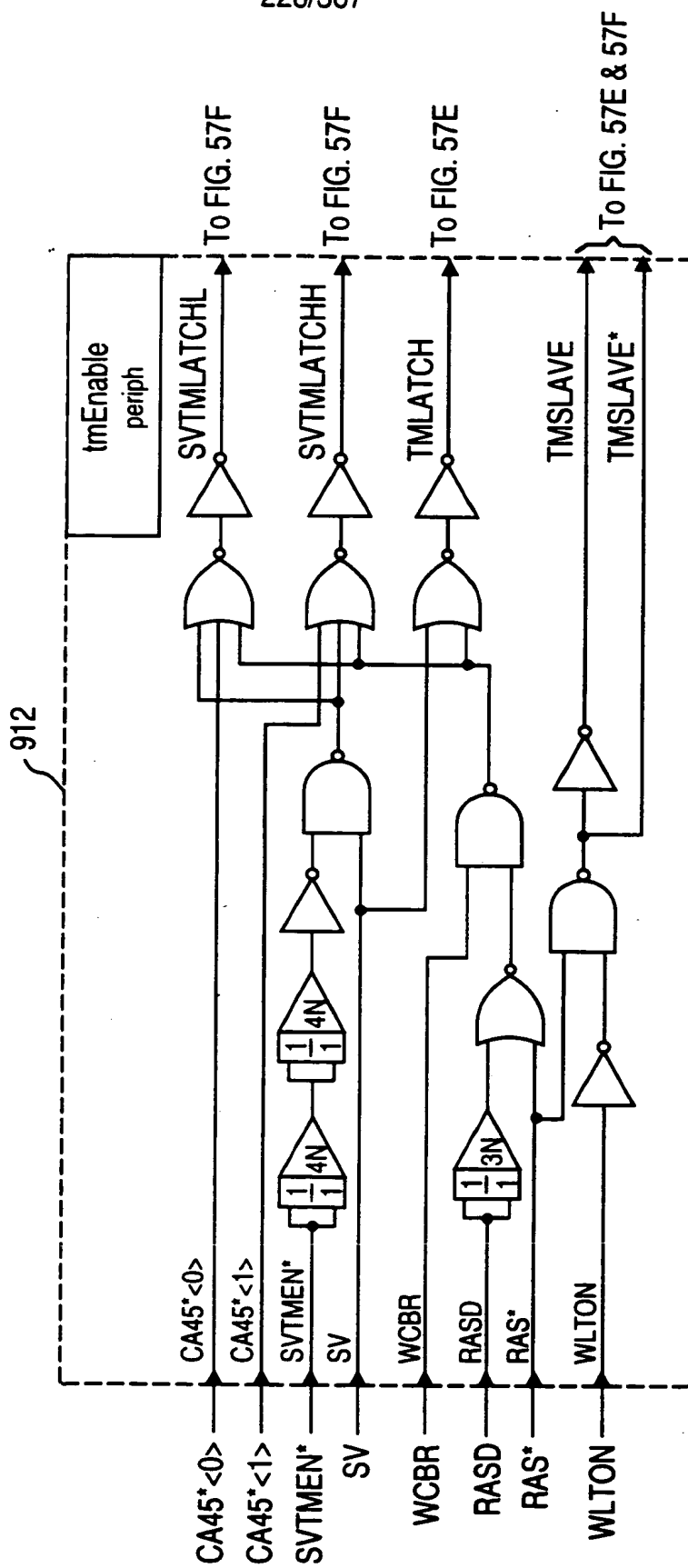


FIG. 57B

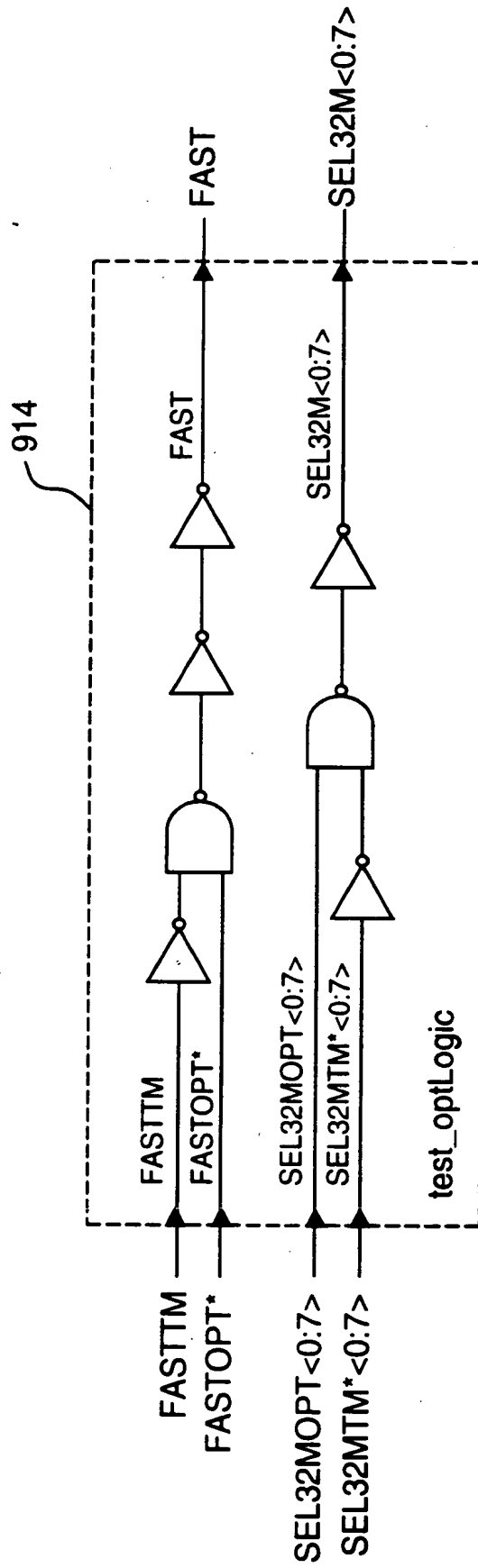


FIG. 57C

FIG. 57D

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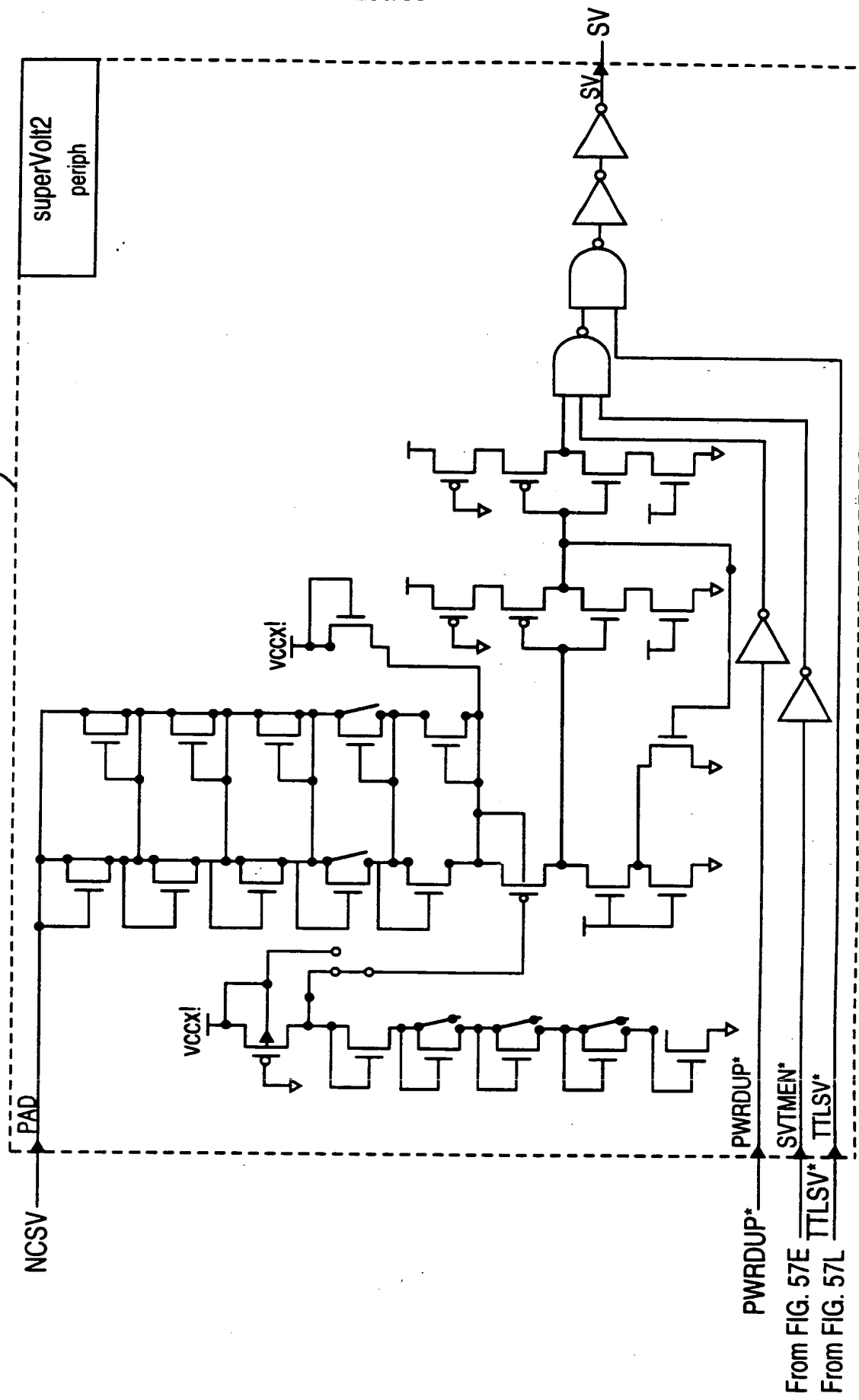


FIG. 57D

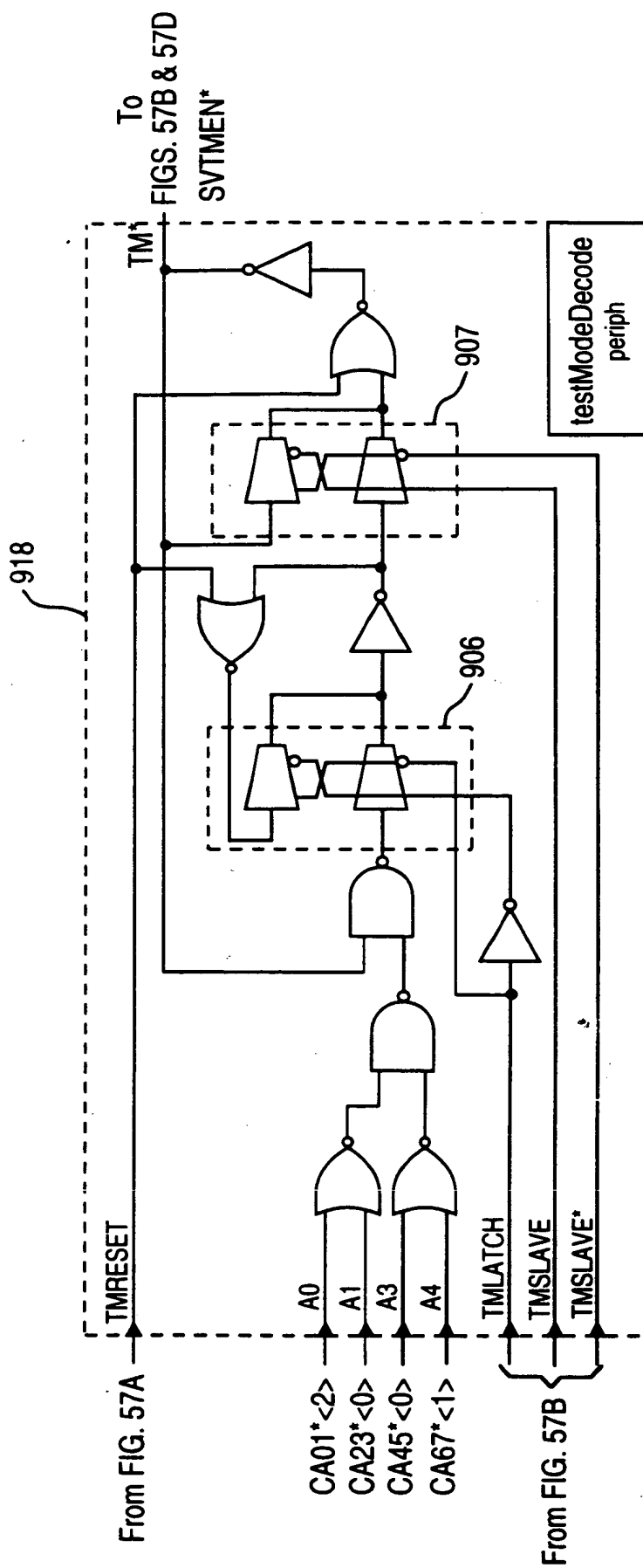


FIG. 57E

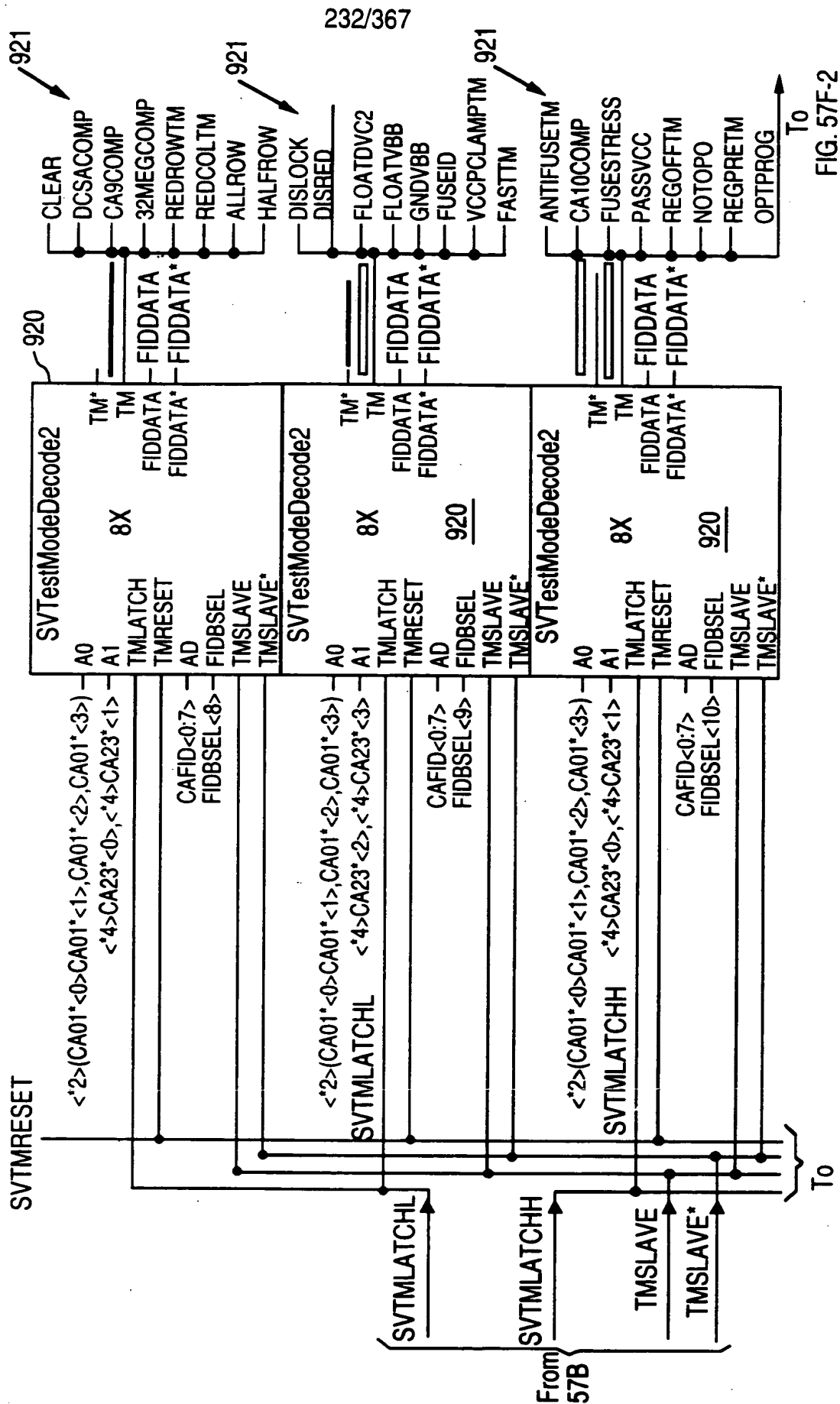


FIG. 57F-3

FIG. 57F-1

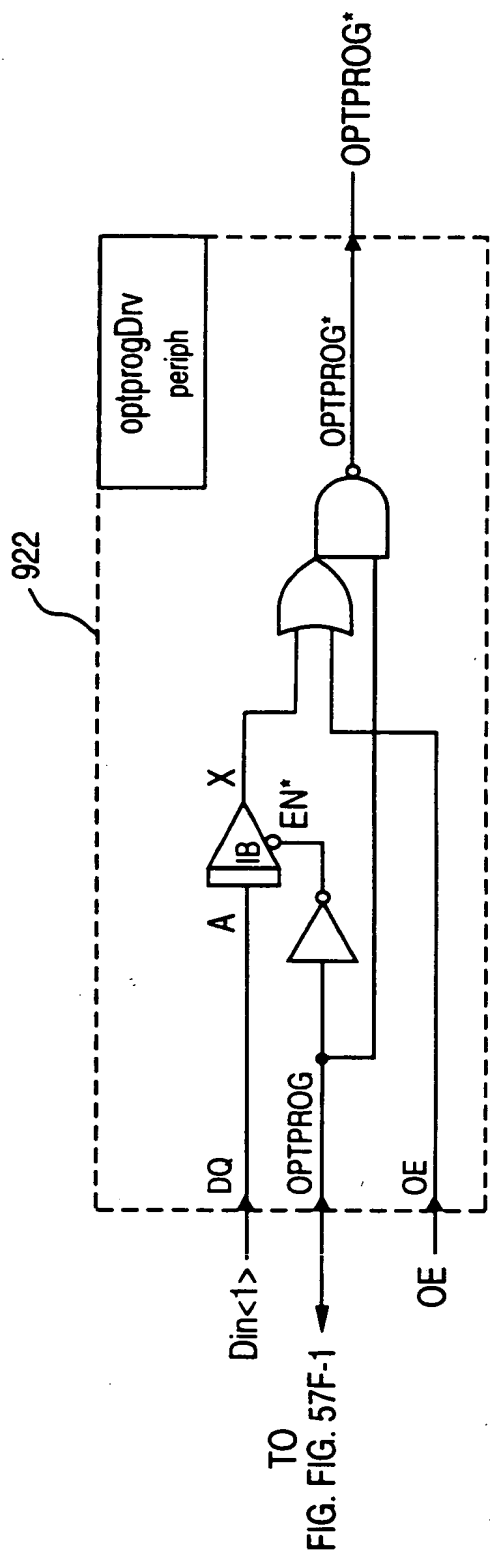
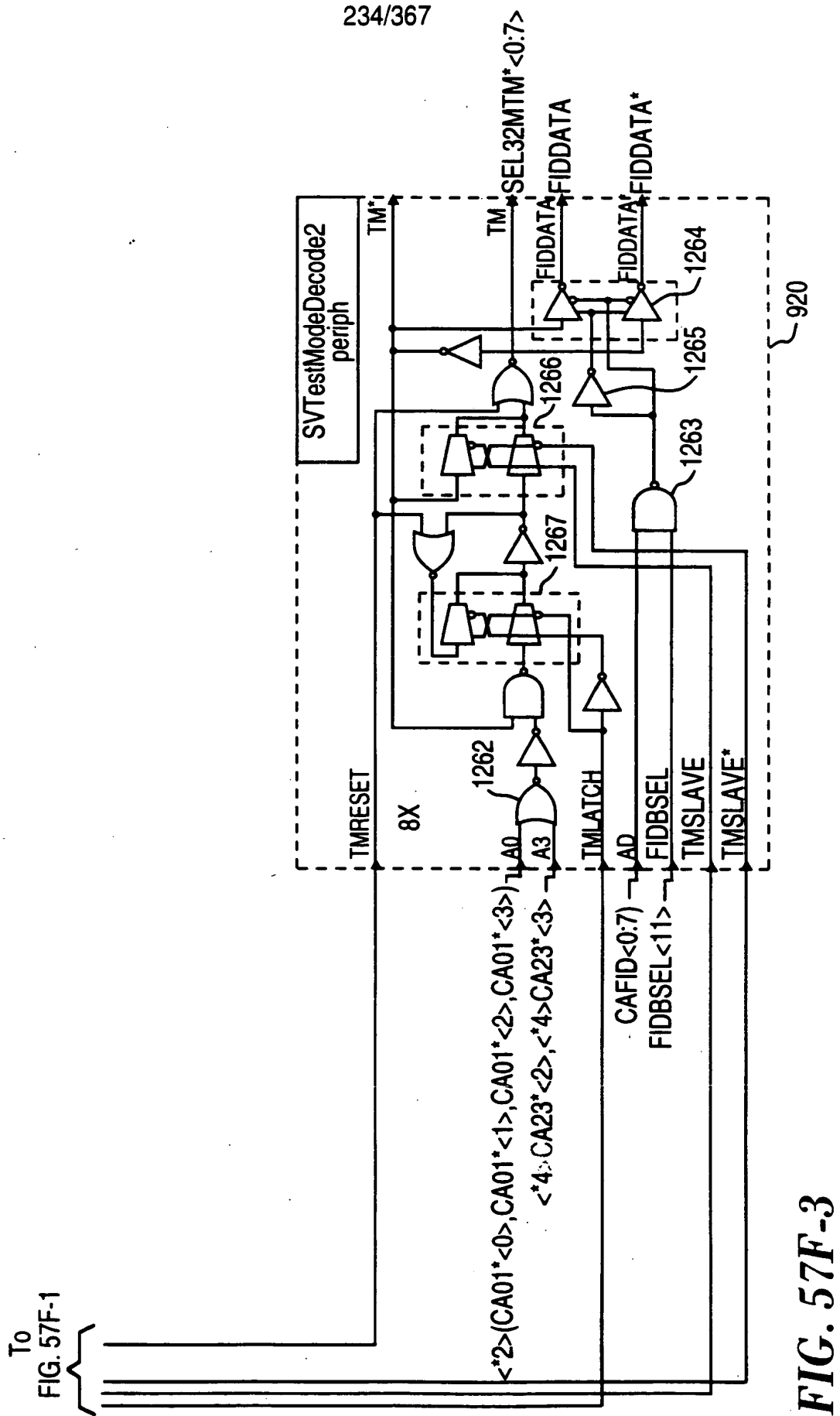


FIG. 57F-2



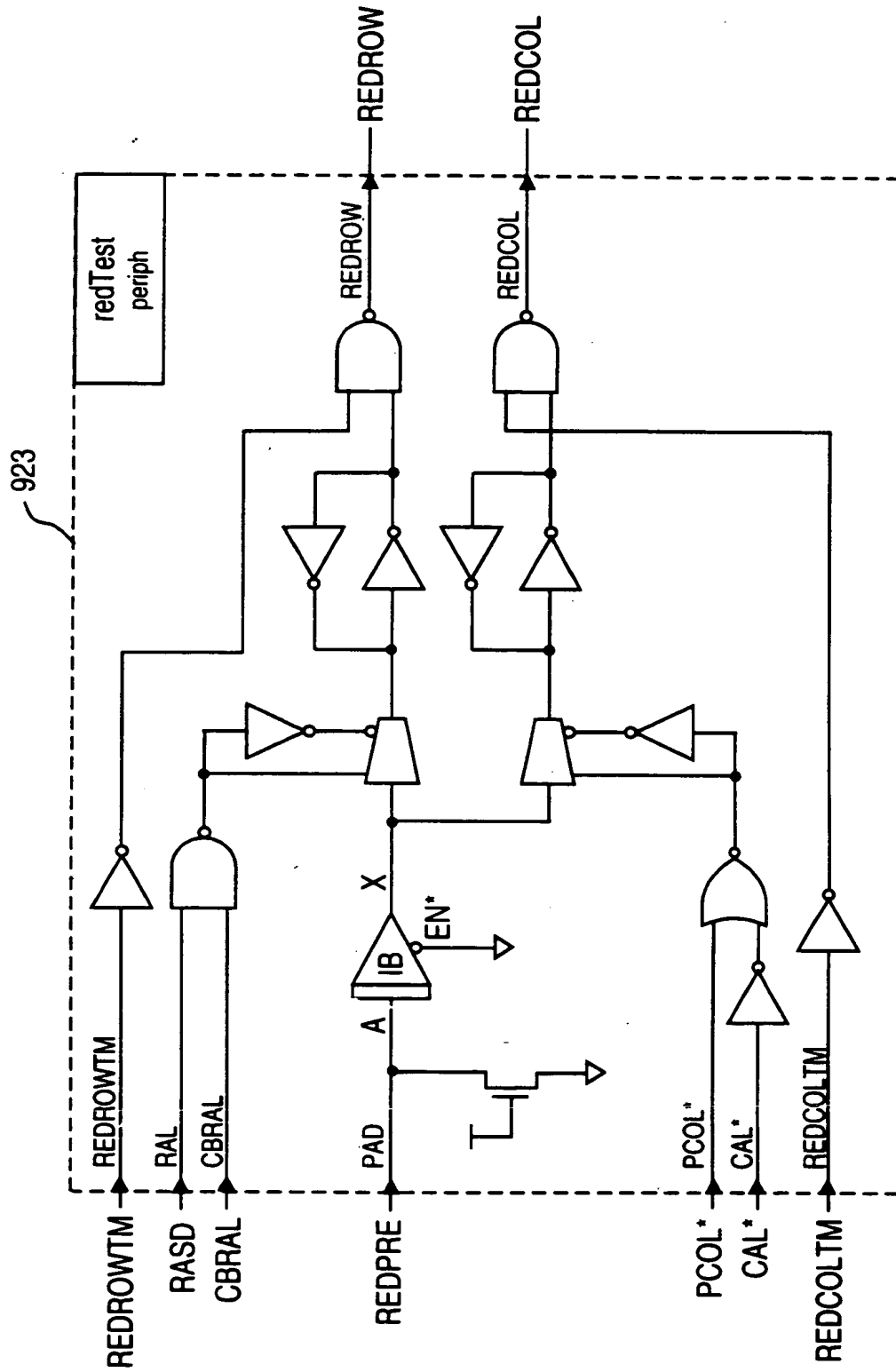


FIG. 57C

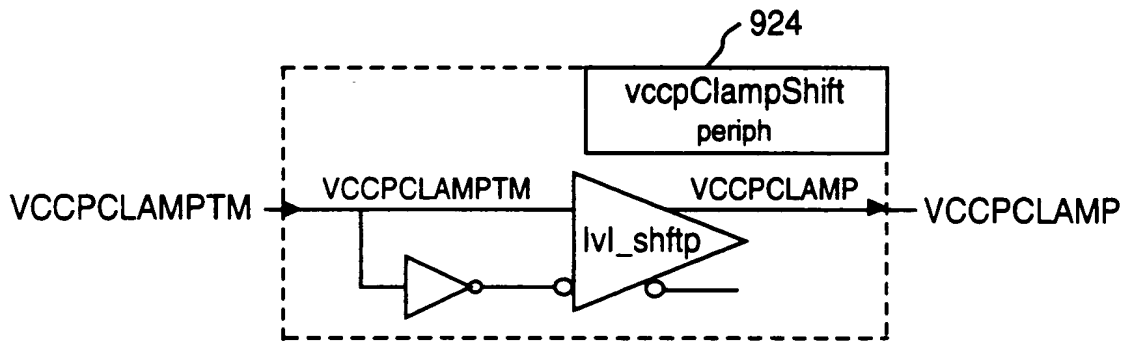
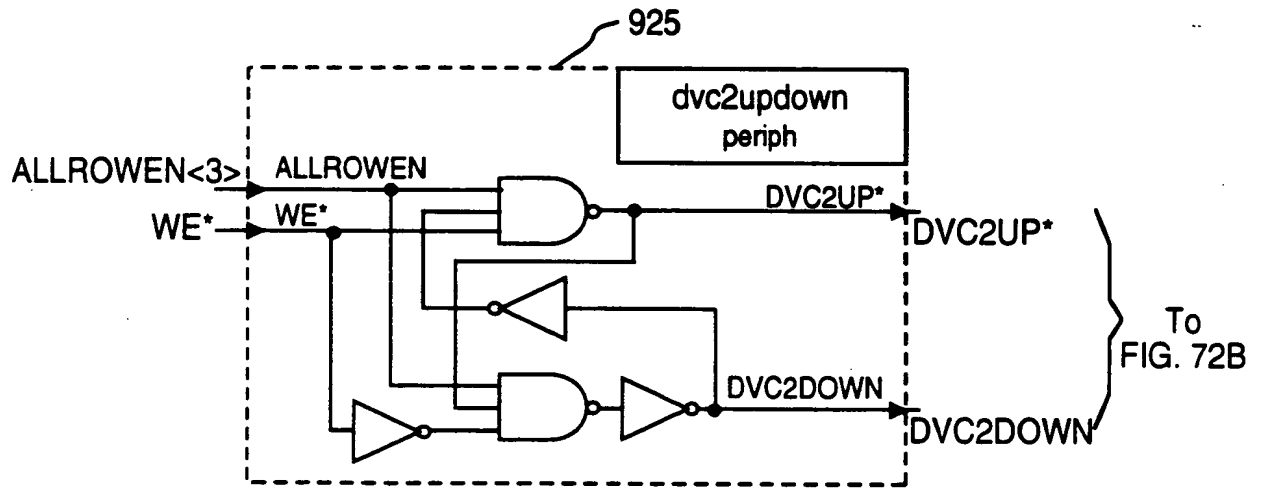
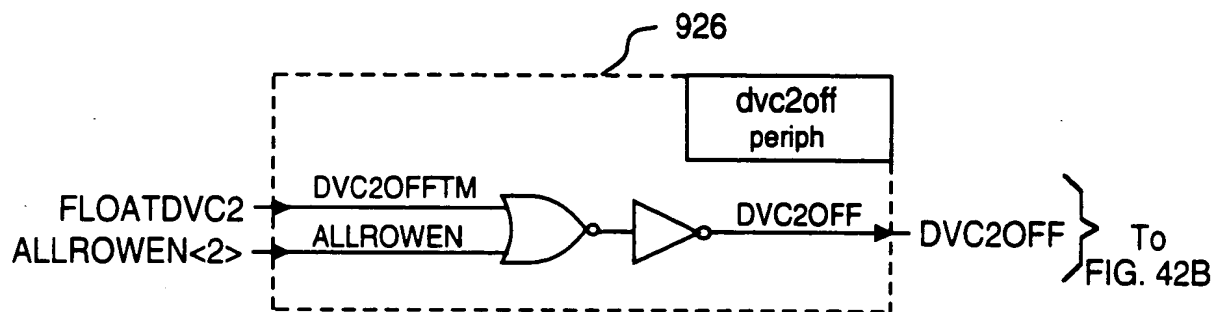


FIG. 57H

**FIG. 57I**

**FIG. 57J**

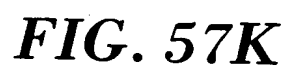
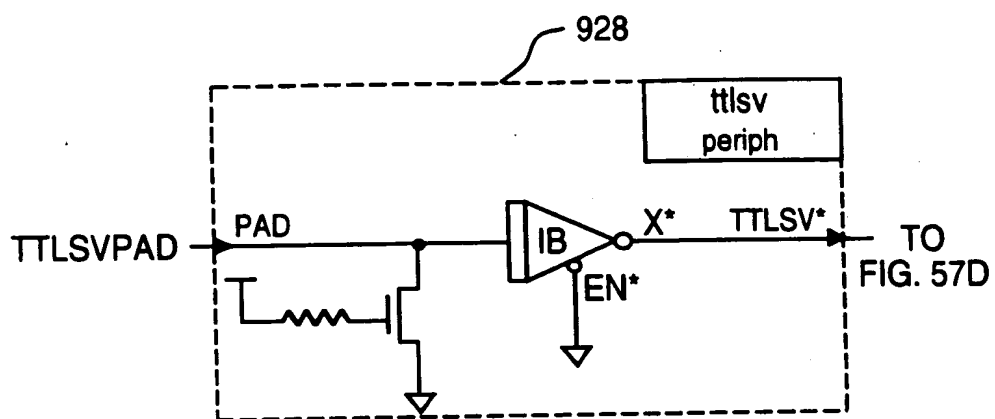


FIG. 57K

**FIG. 57L**

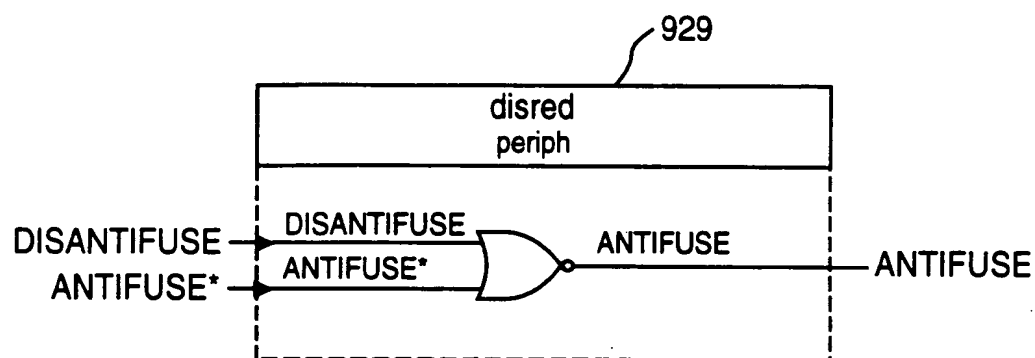
**FIG. 57M**



FIG. 58A



FIG. 58B

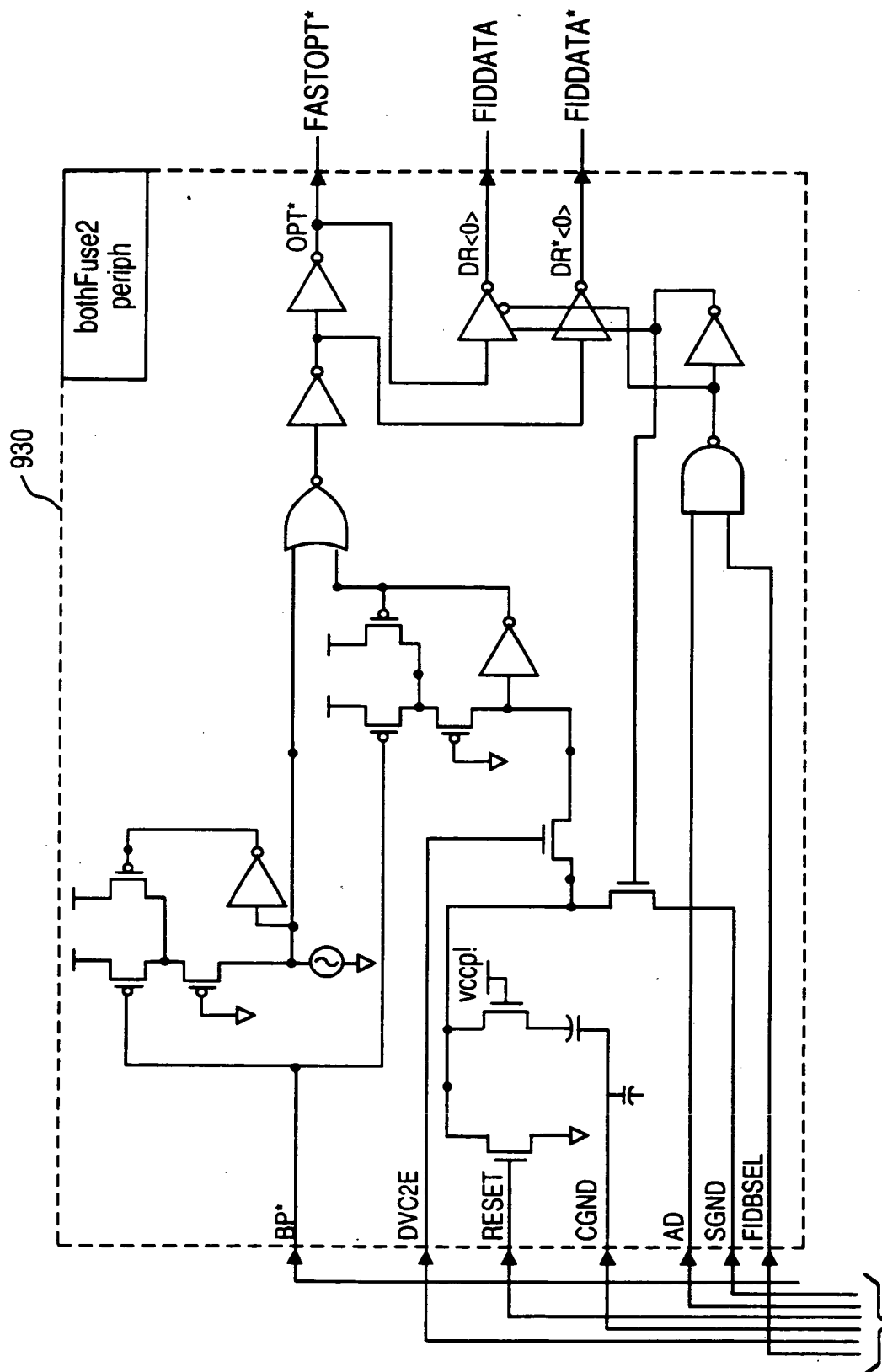


FIG. 59B

FIG. 59A

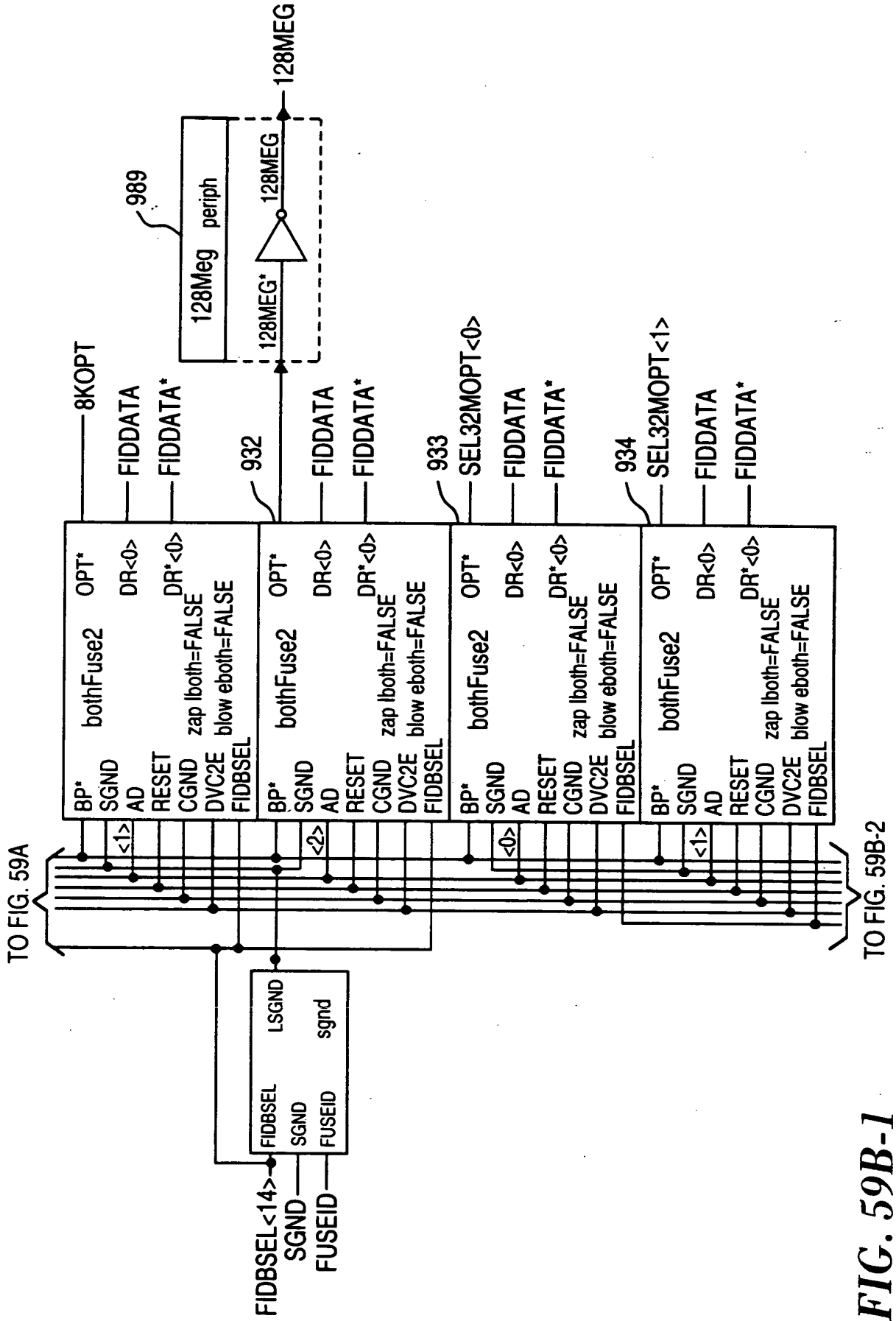


FIG. 59B-1

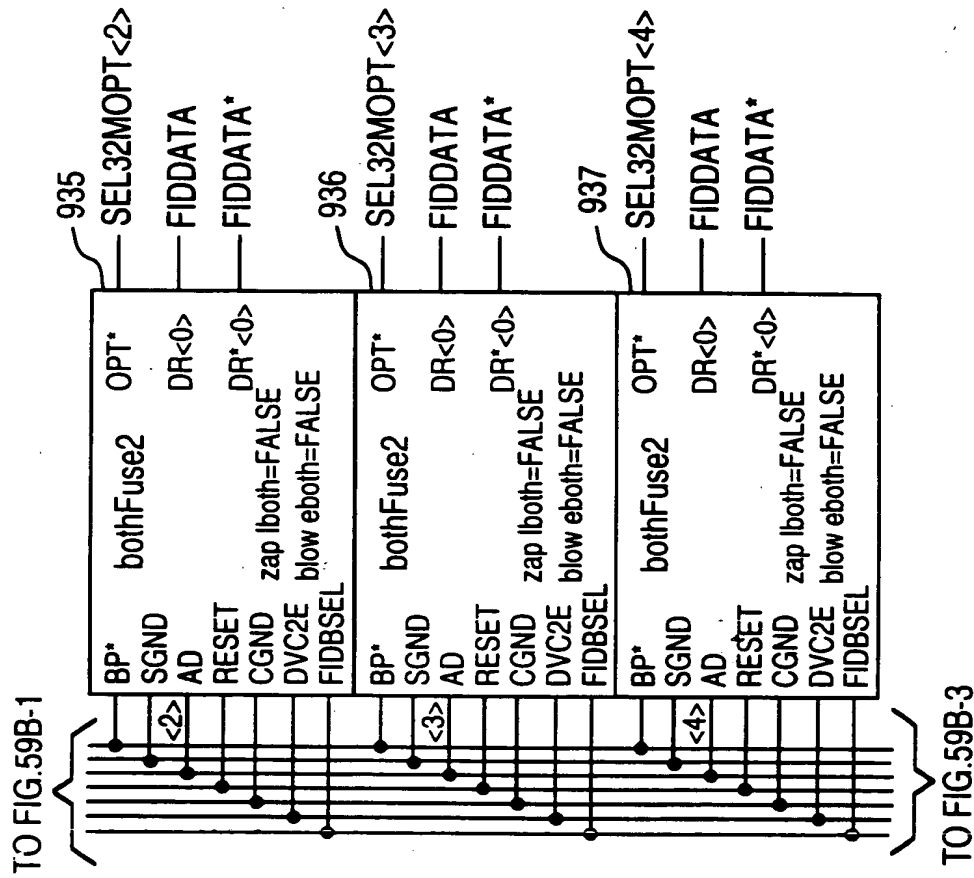


FIG. 59B-2

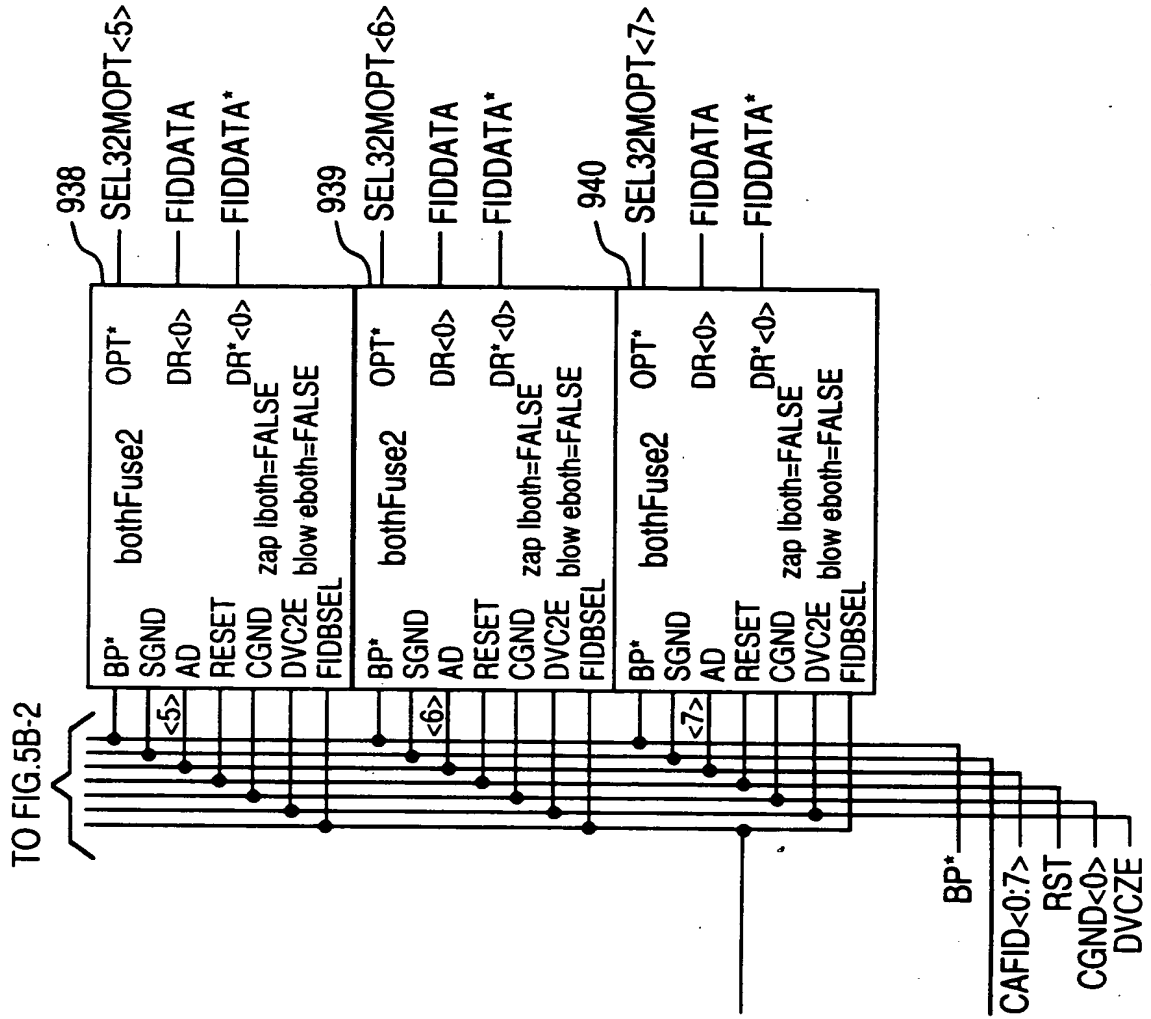
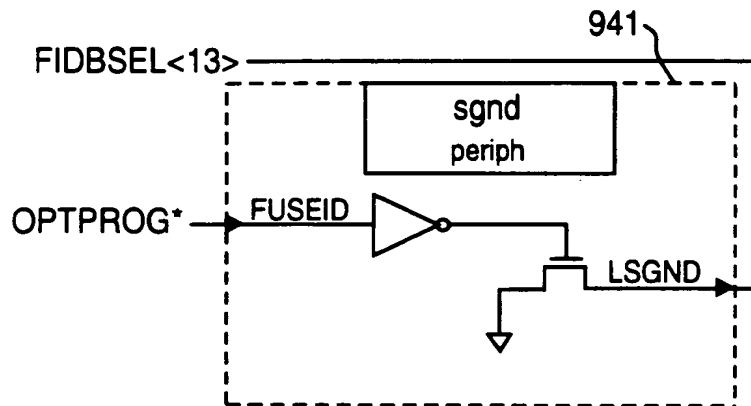


FIG. 59B-3

**FIG. 59C**

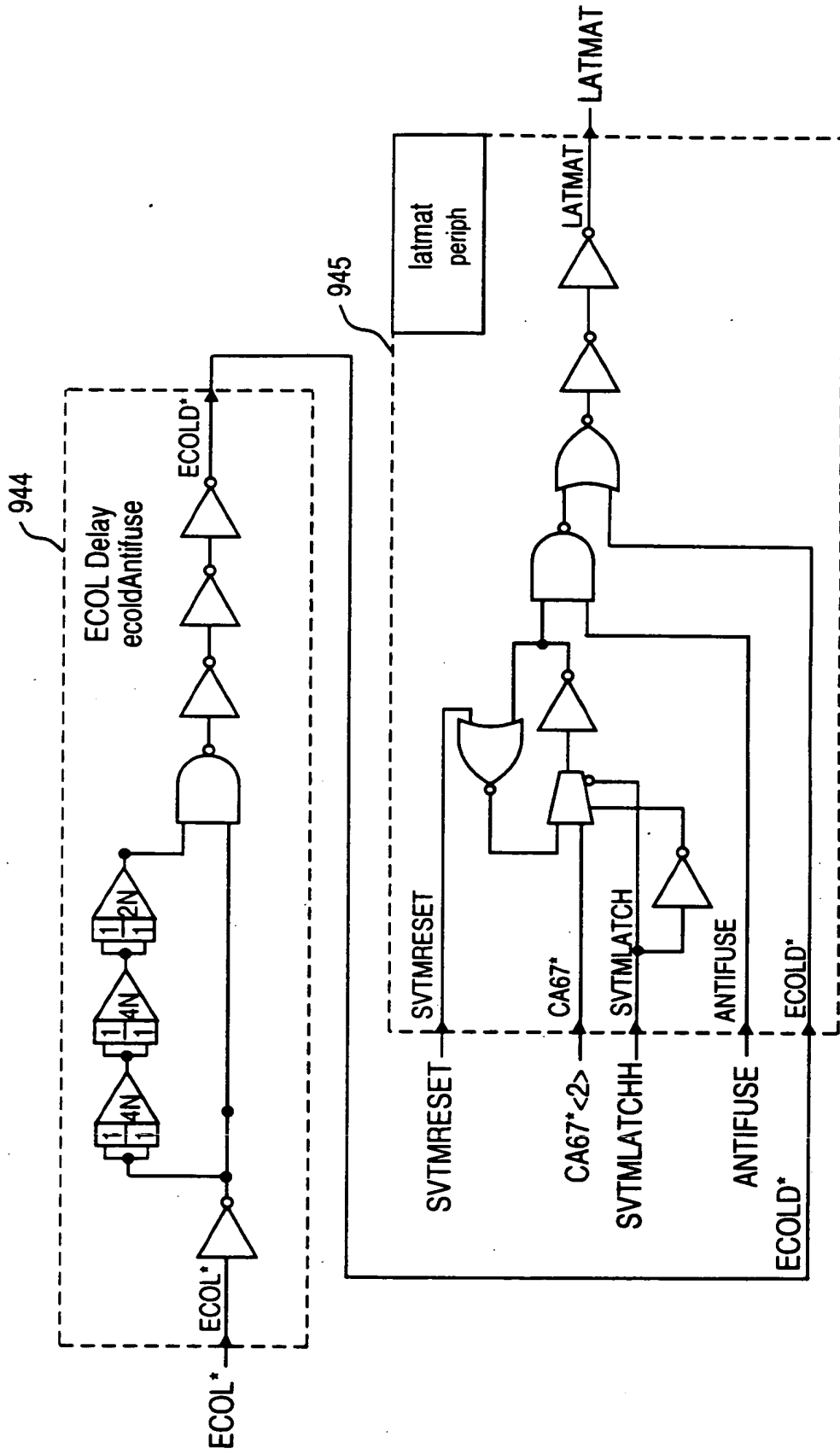


FIG. 59D

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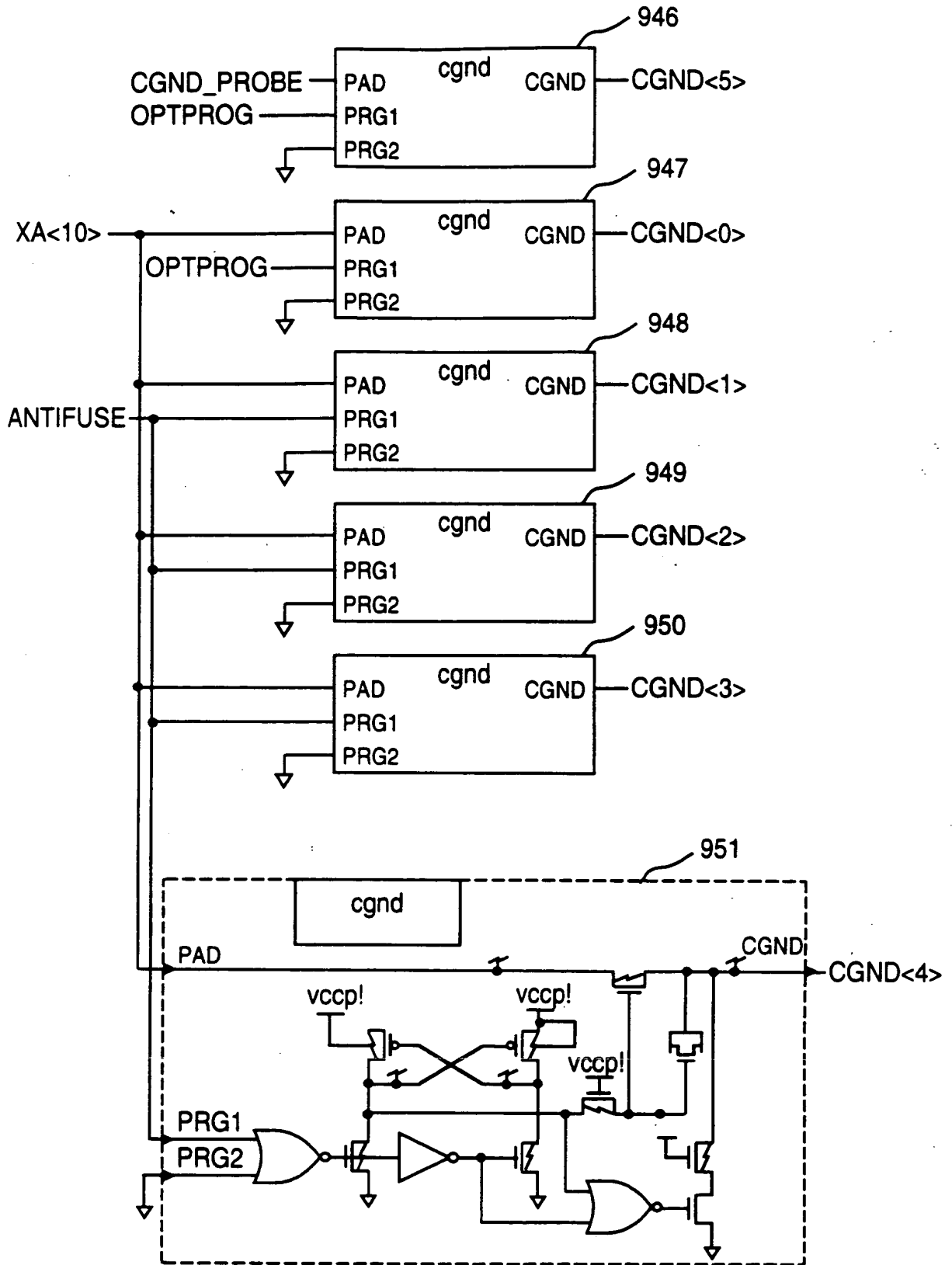


FIG. 59E

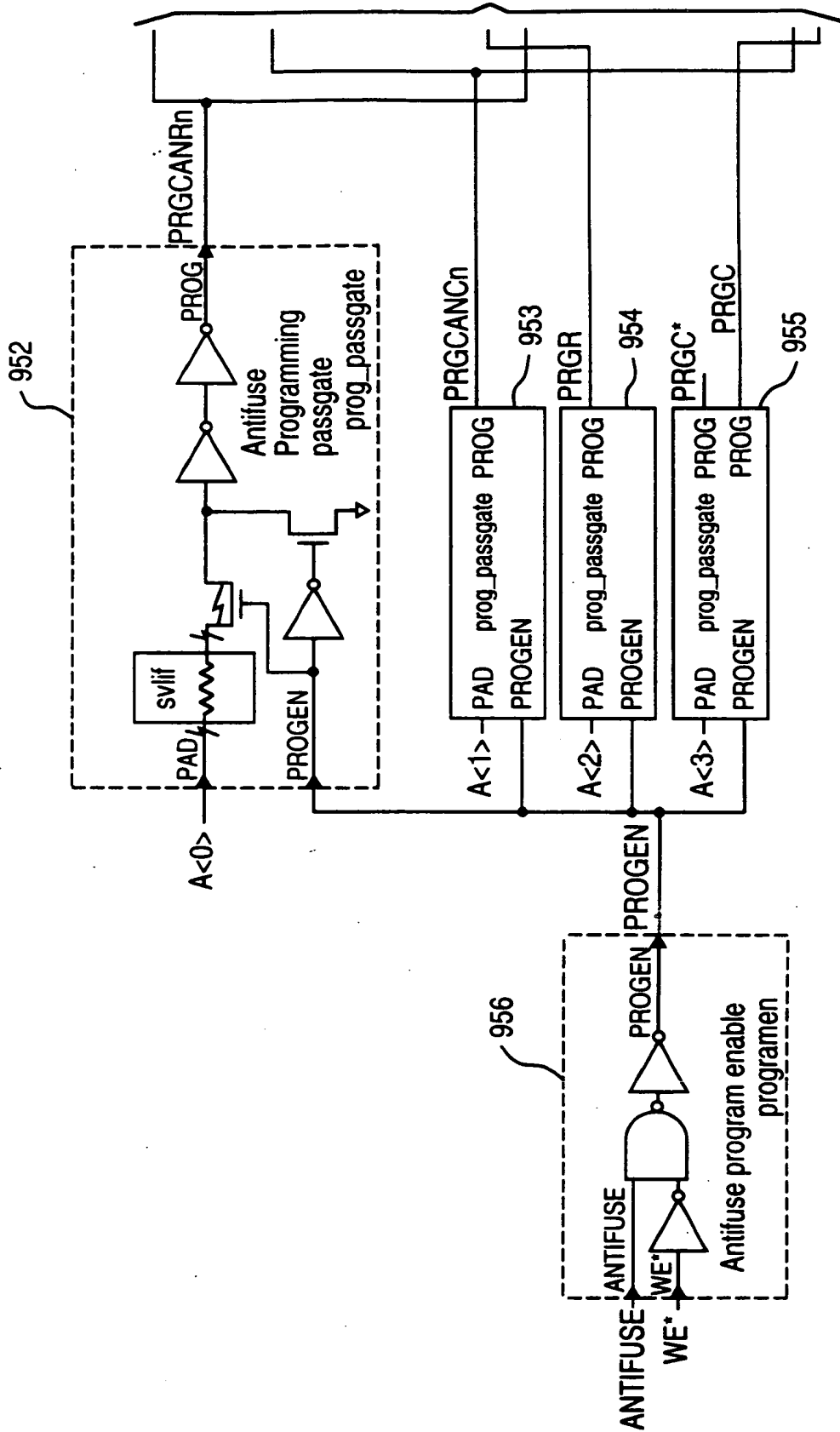


FIG. 59F-1

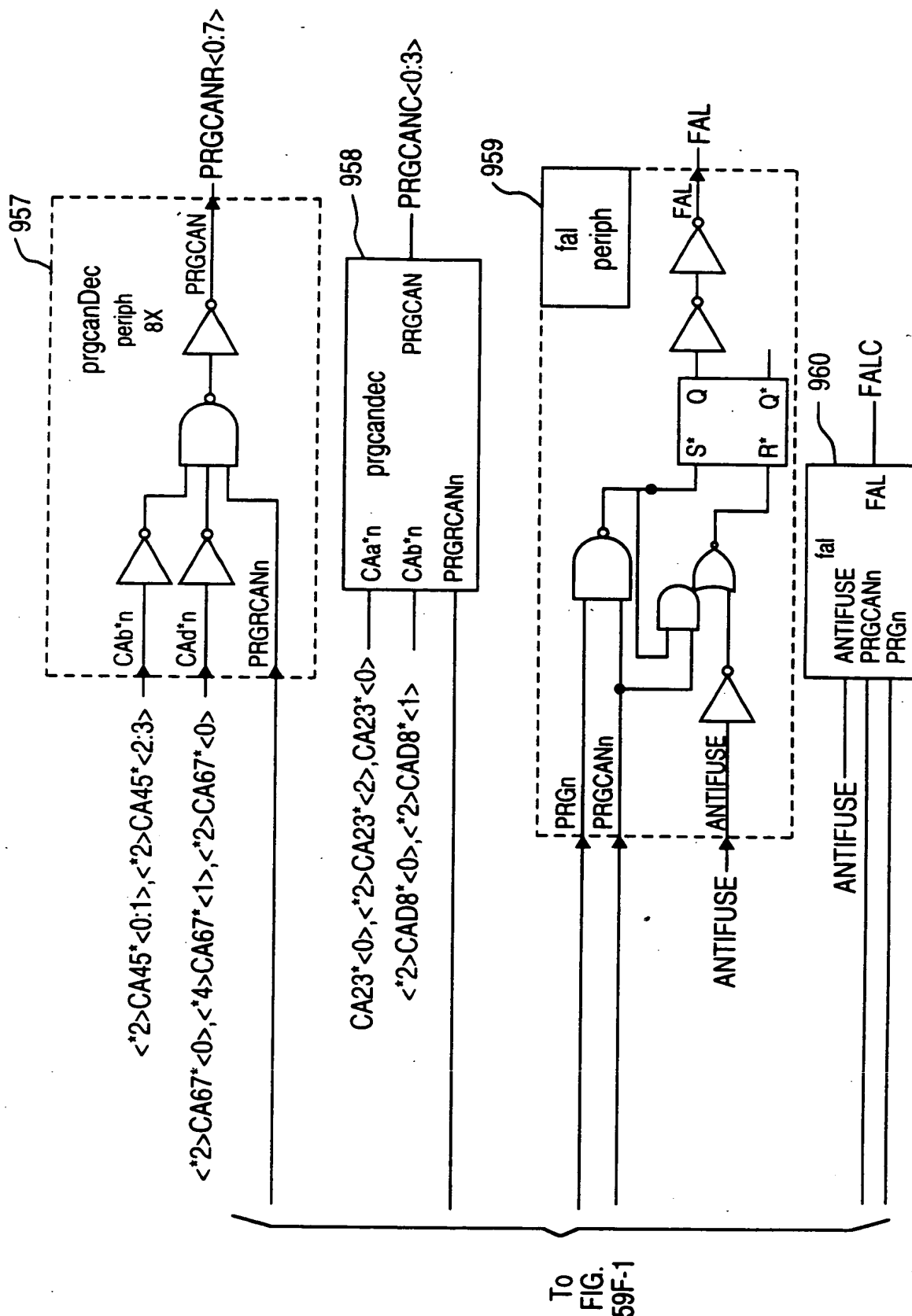


FIG. 59F-2

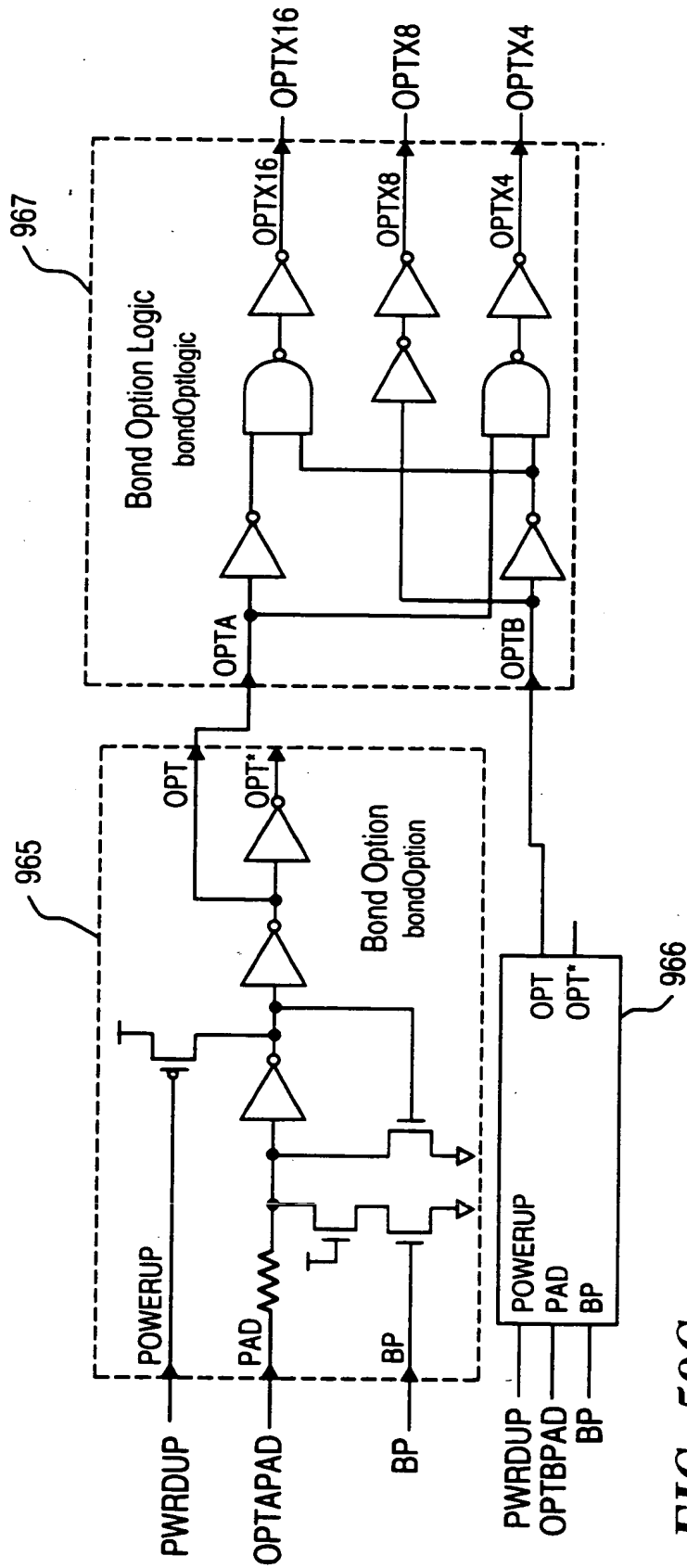


FIG. 59C

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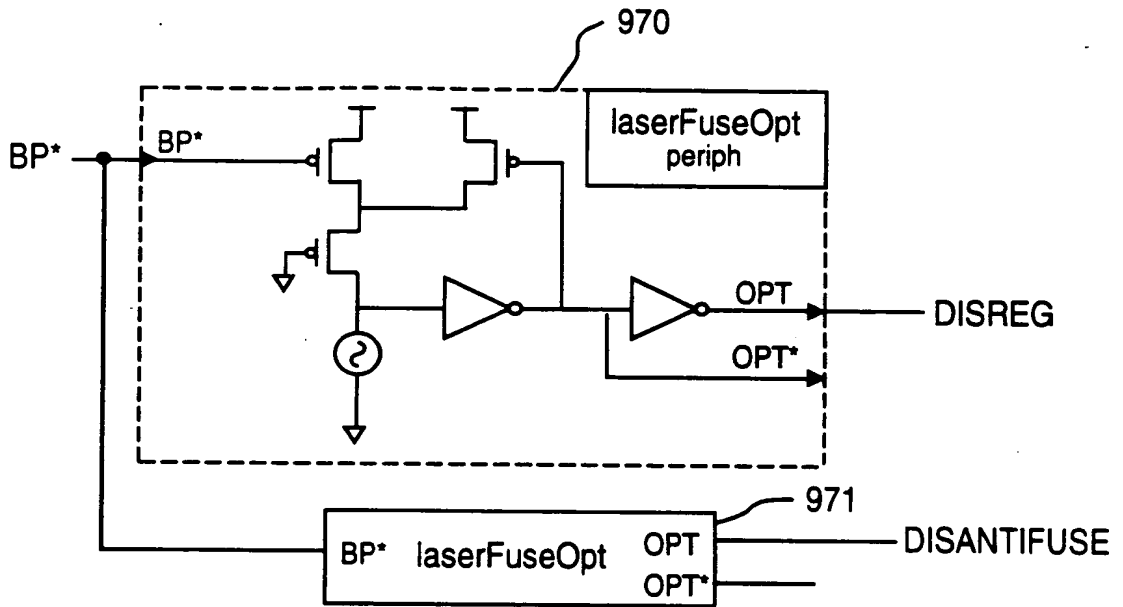


FIG. 59H

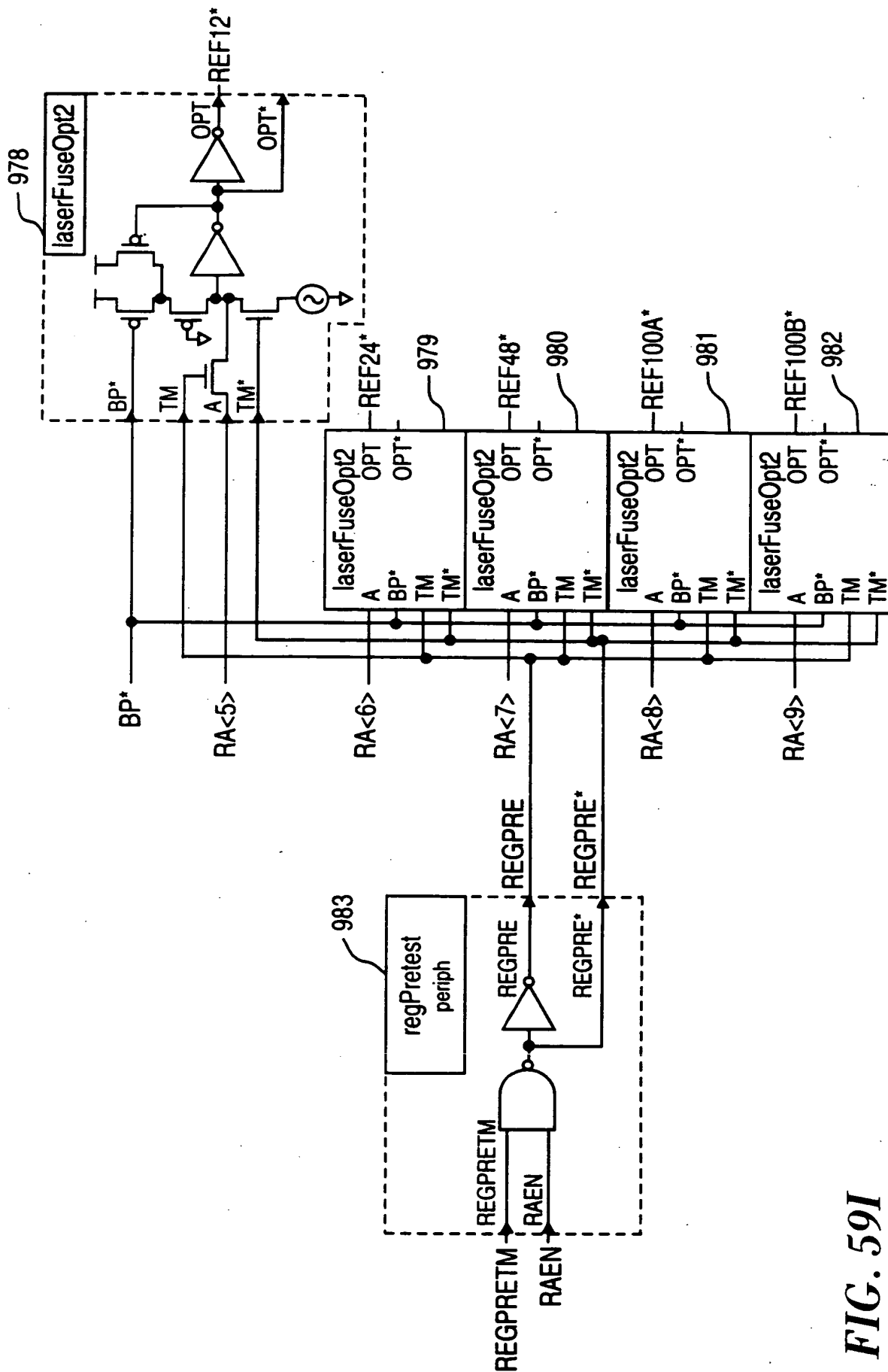
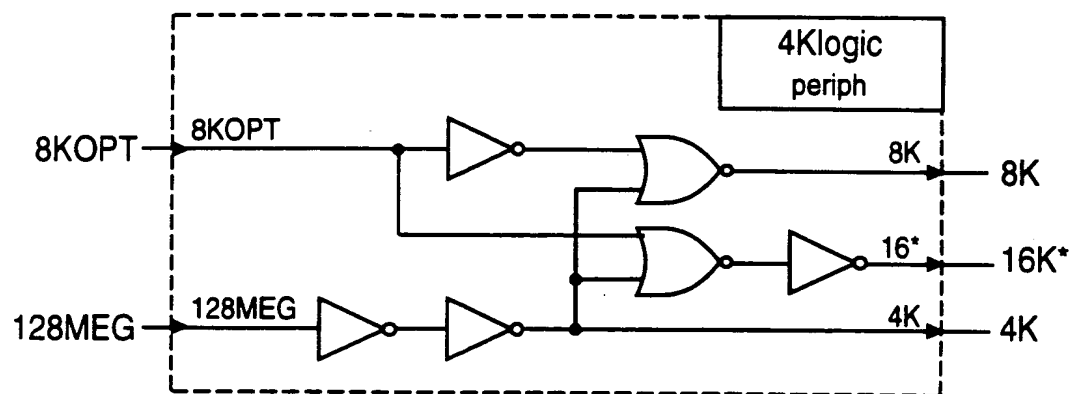
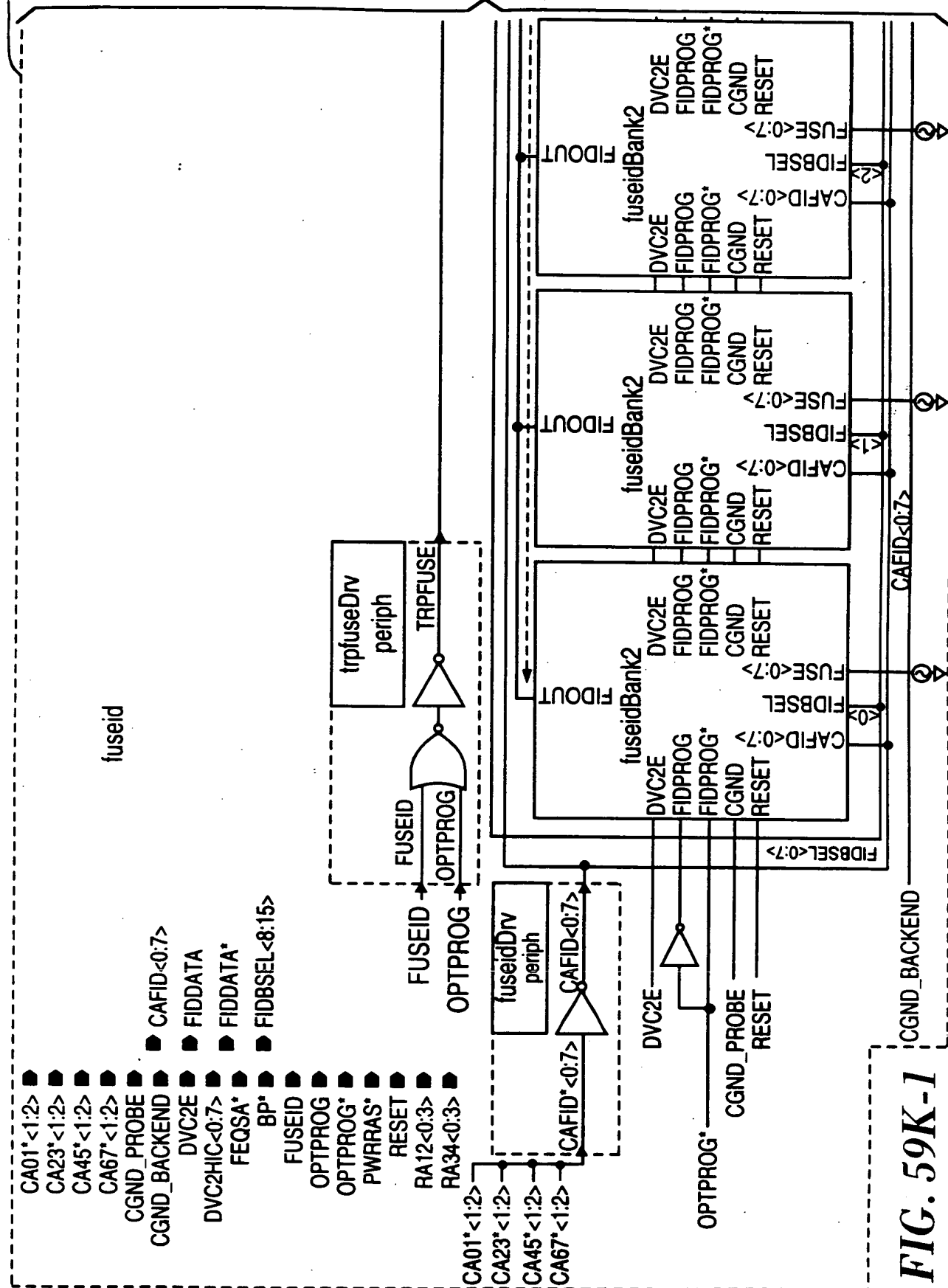
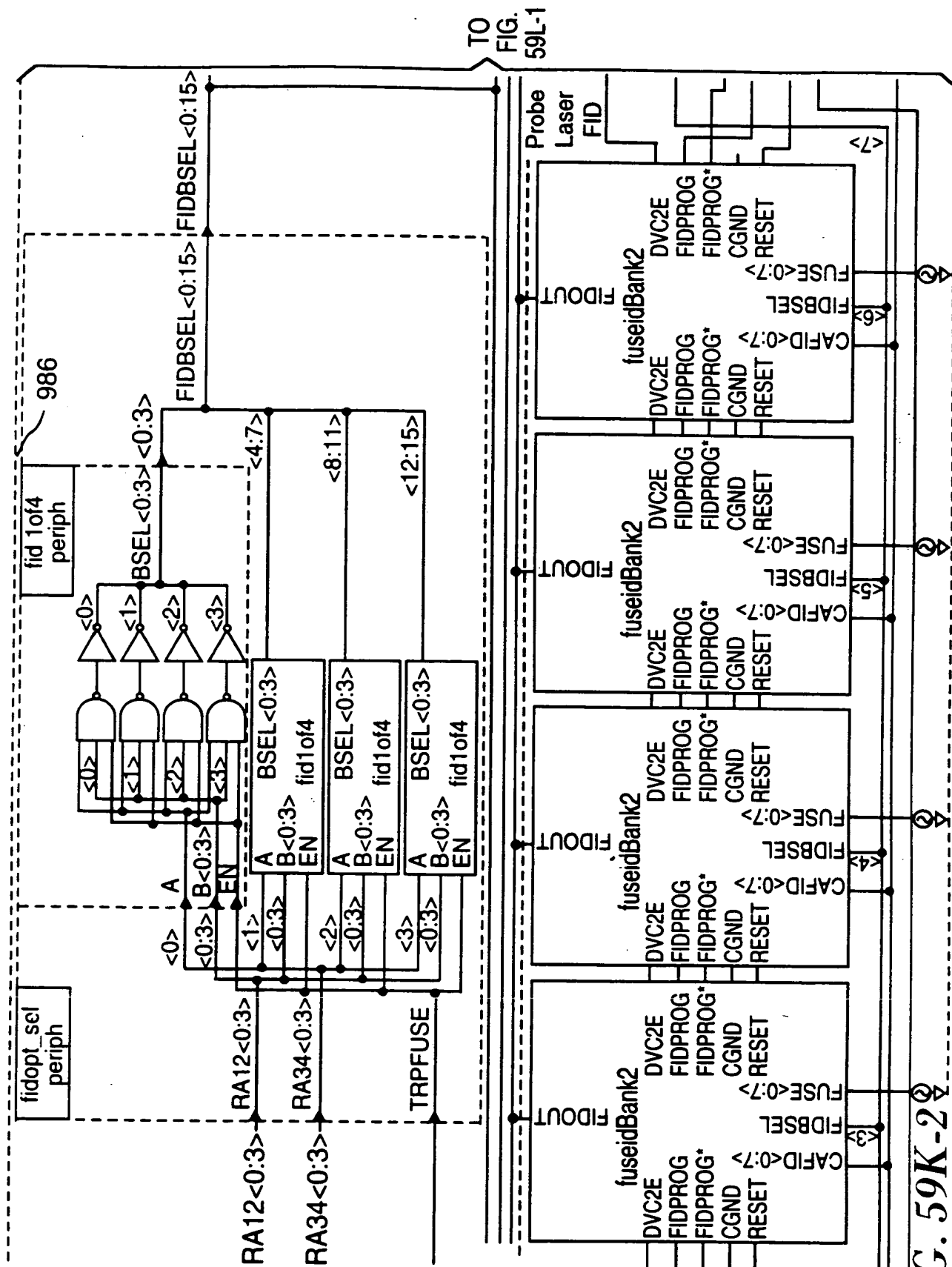


FIG. 591

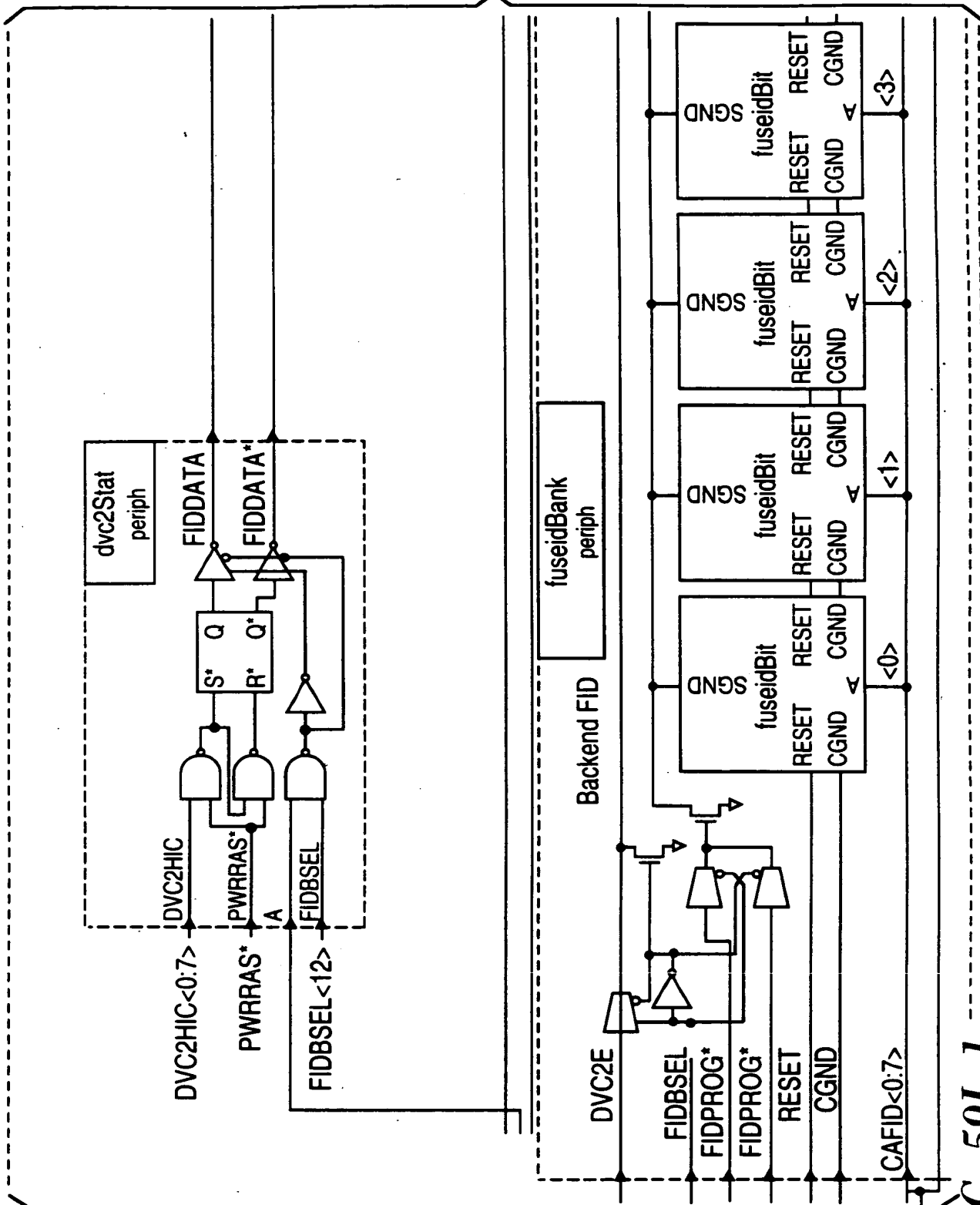
**FIG. 59J**





TO FIG. 59L-1

TO
FIG.
59L-2



TO
FIG.
59K-1

FIG. 59L-1

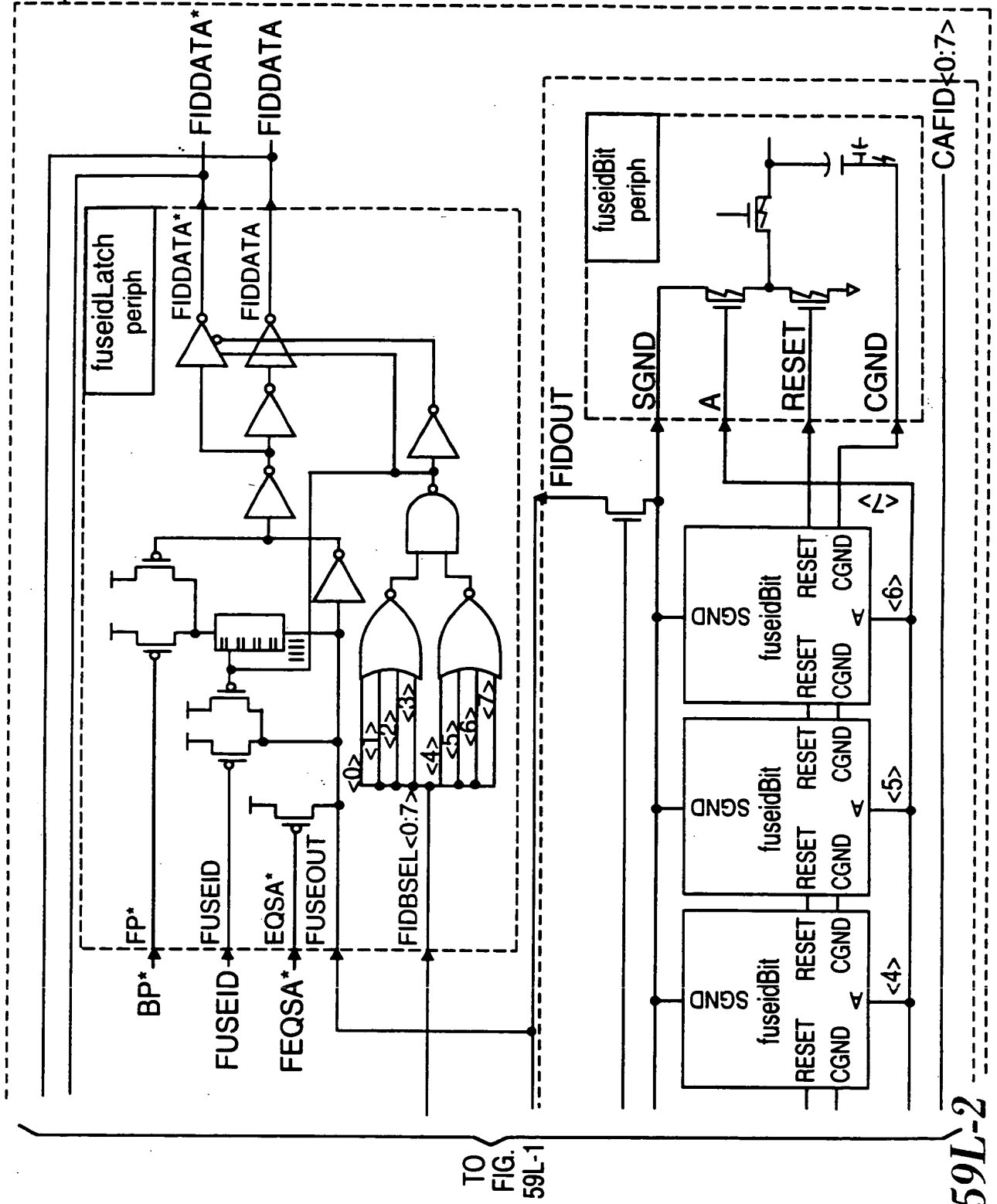


FIG. 59L-2

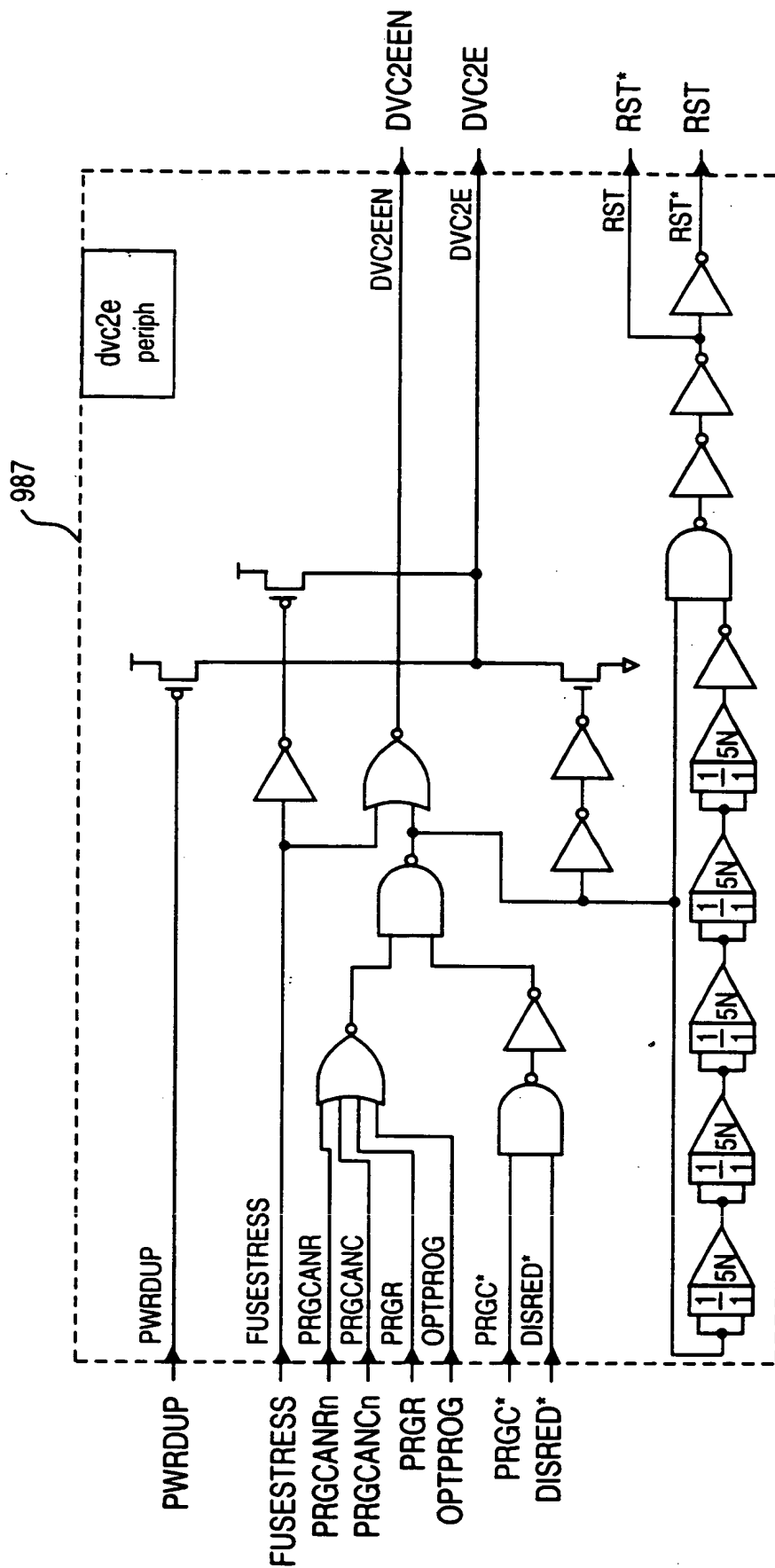
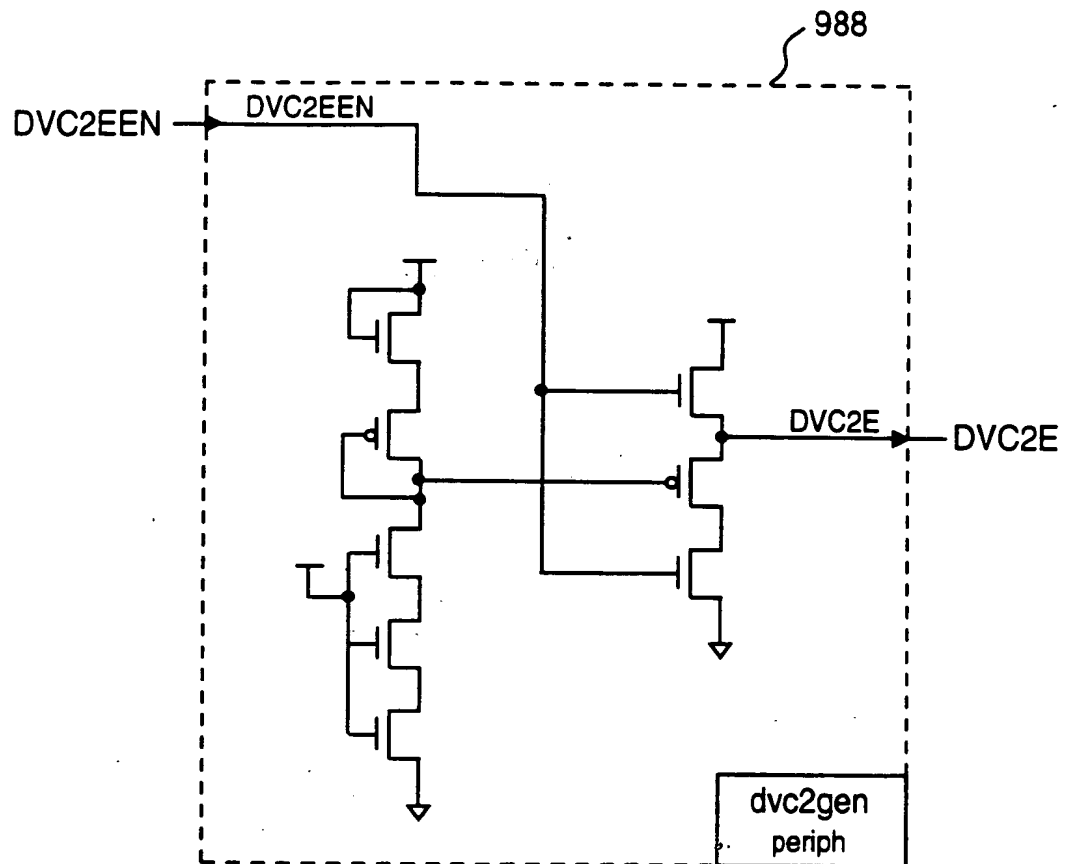


FIG. 59M



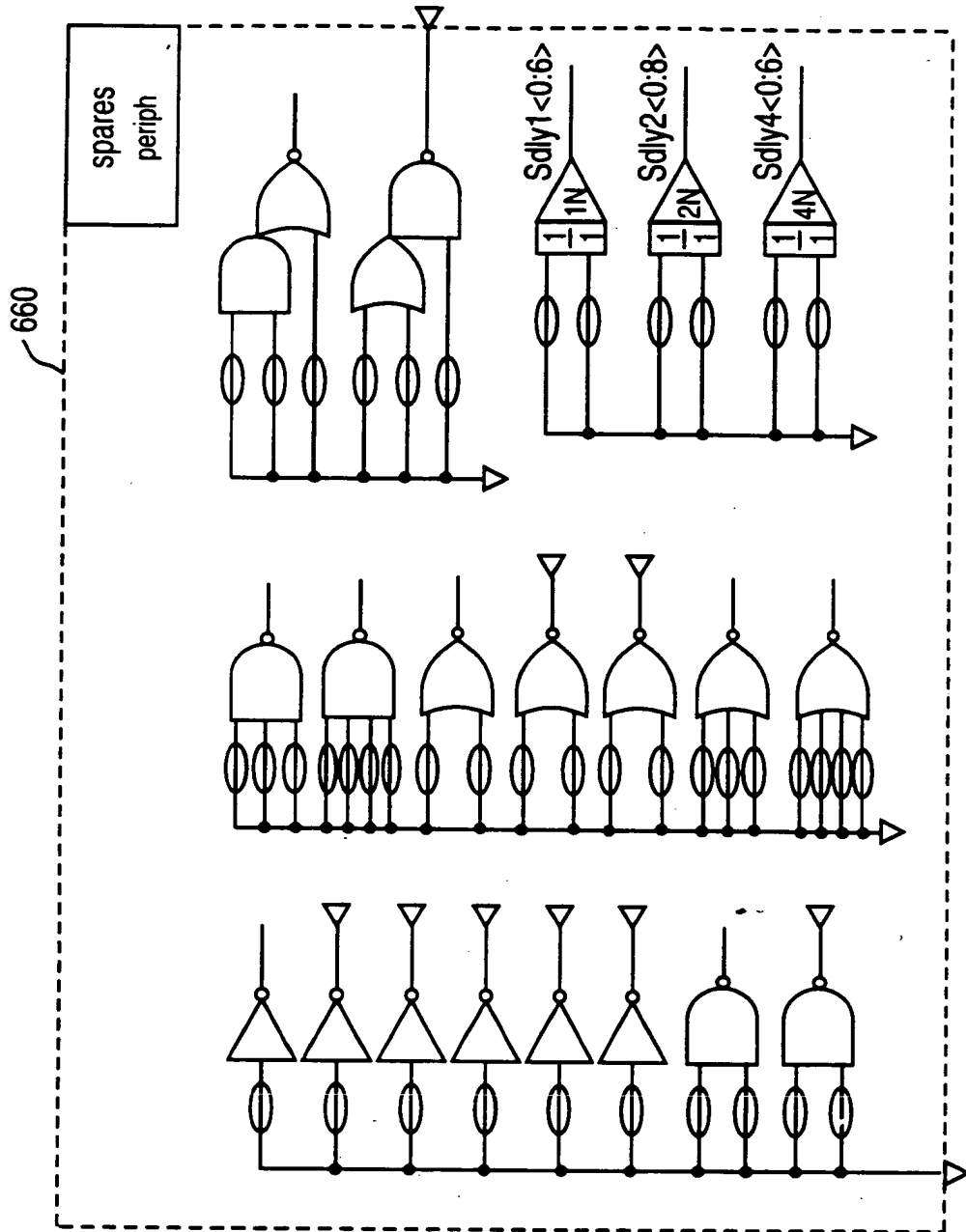
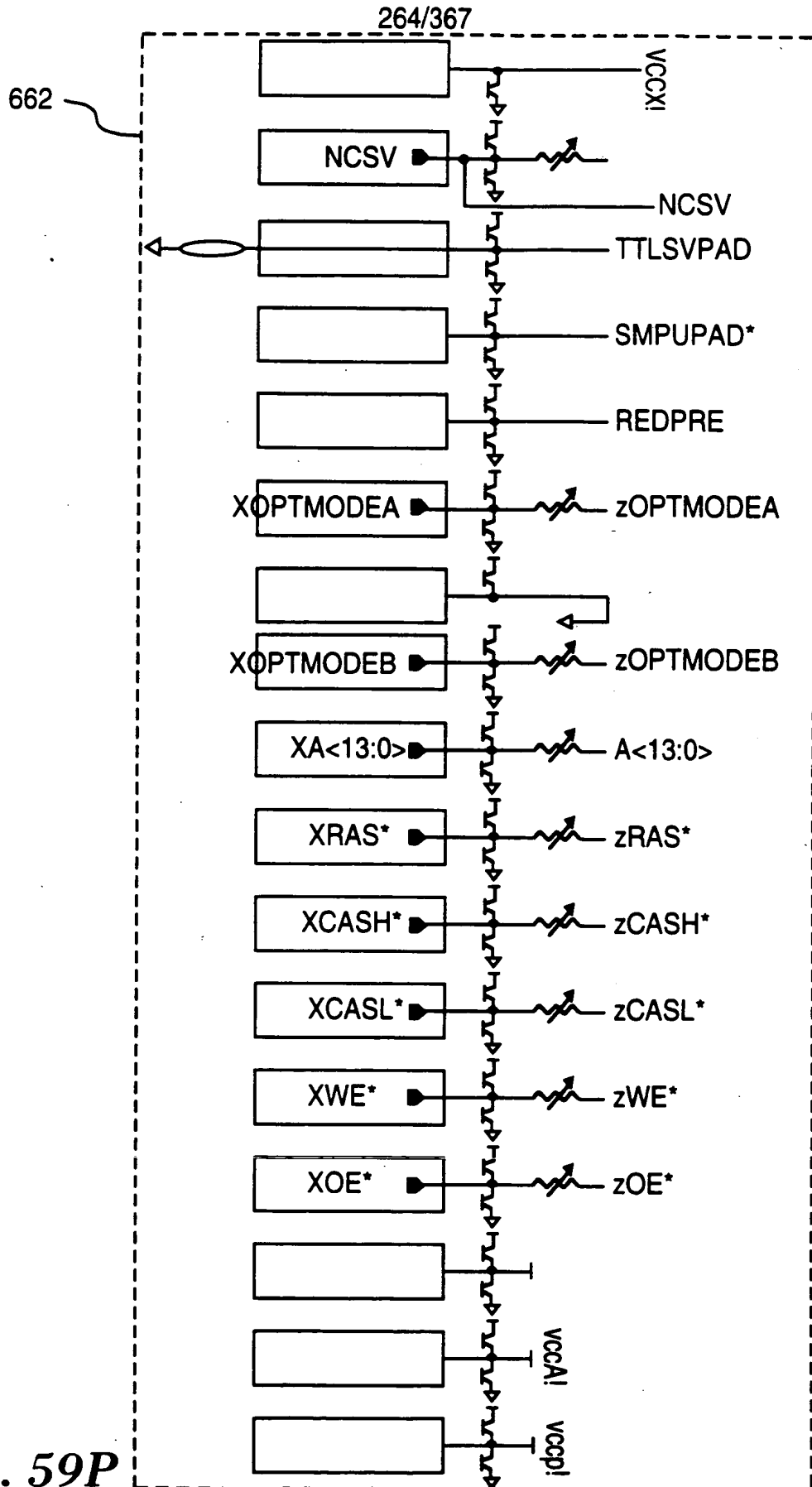


FIG. 590



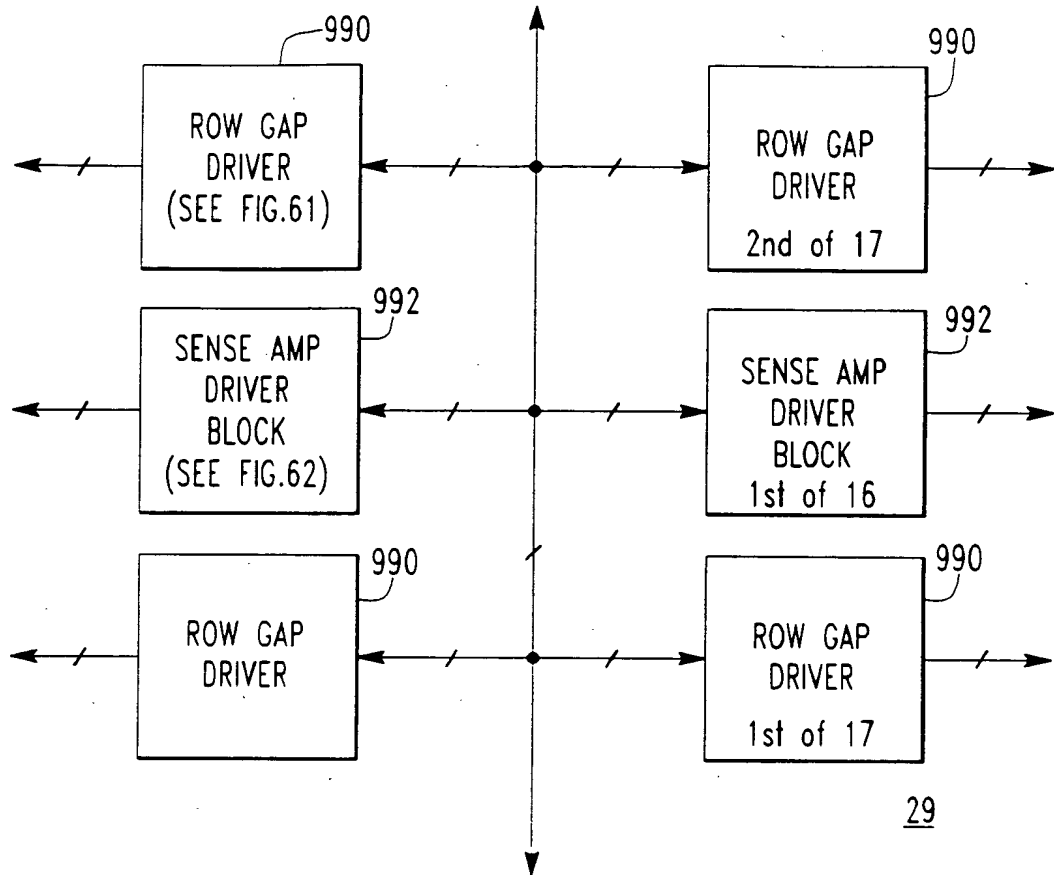


FIG. 60

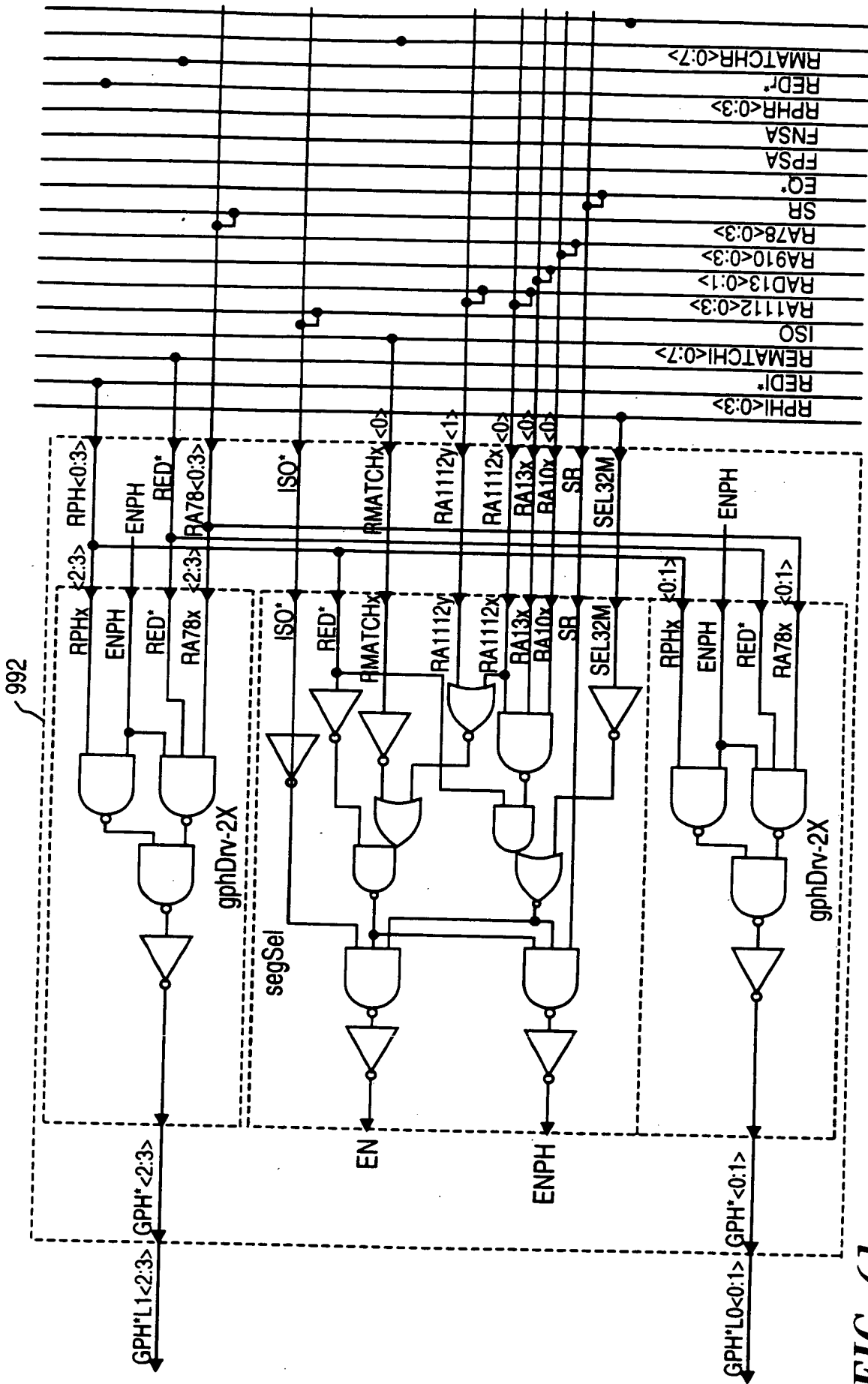


FIG. 61

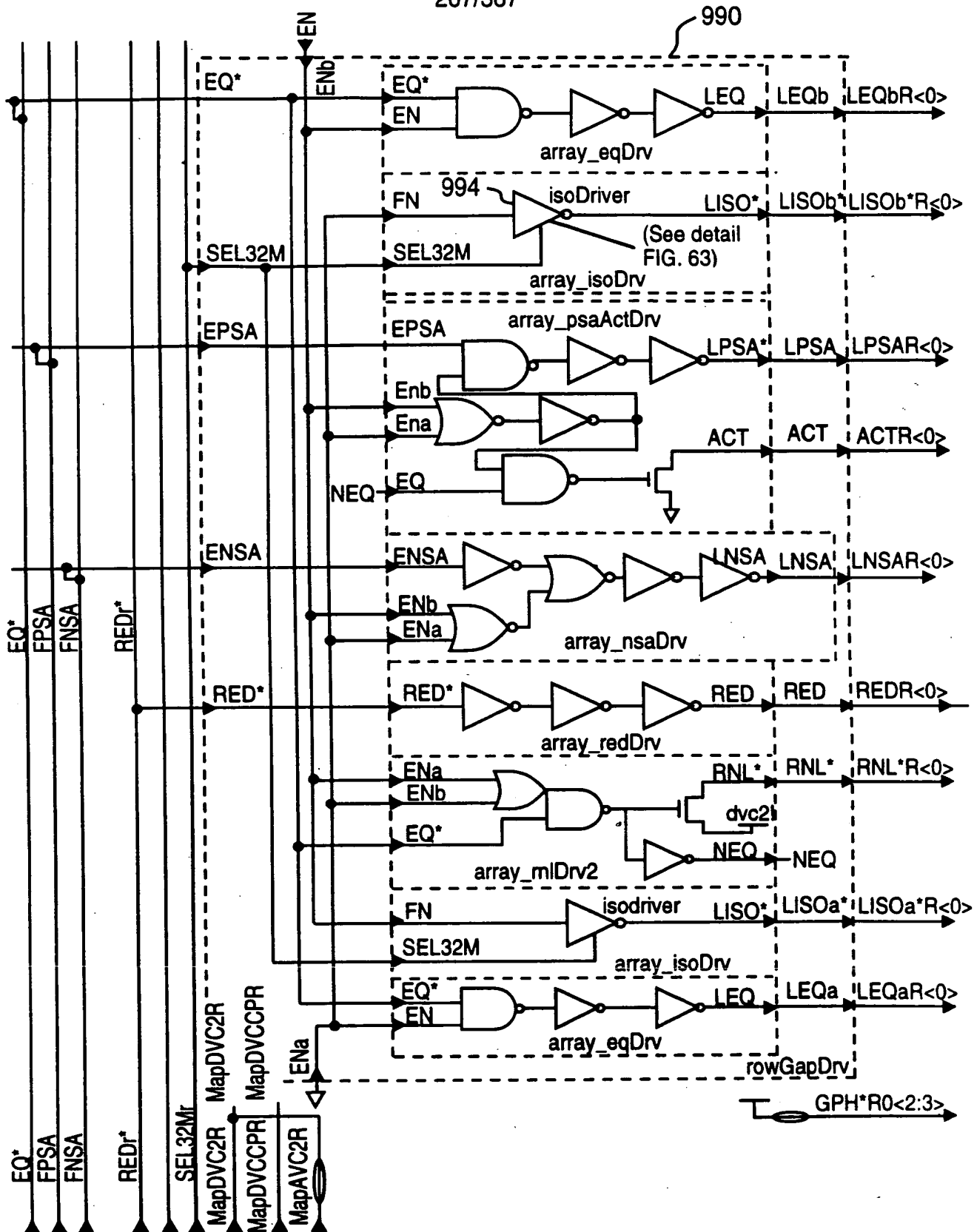


FIG. 62

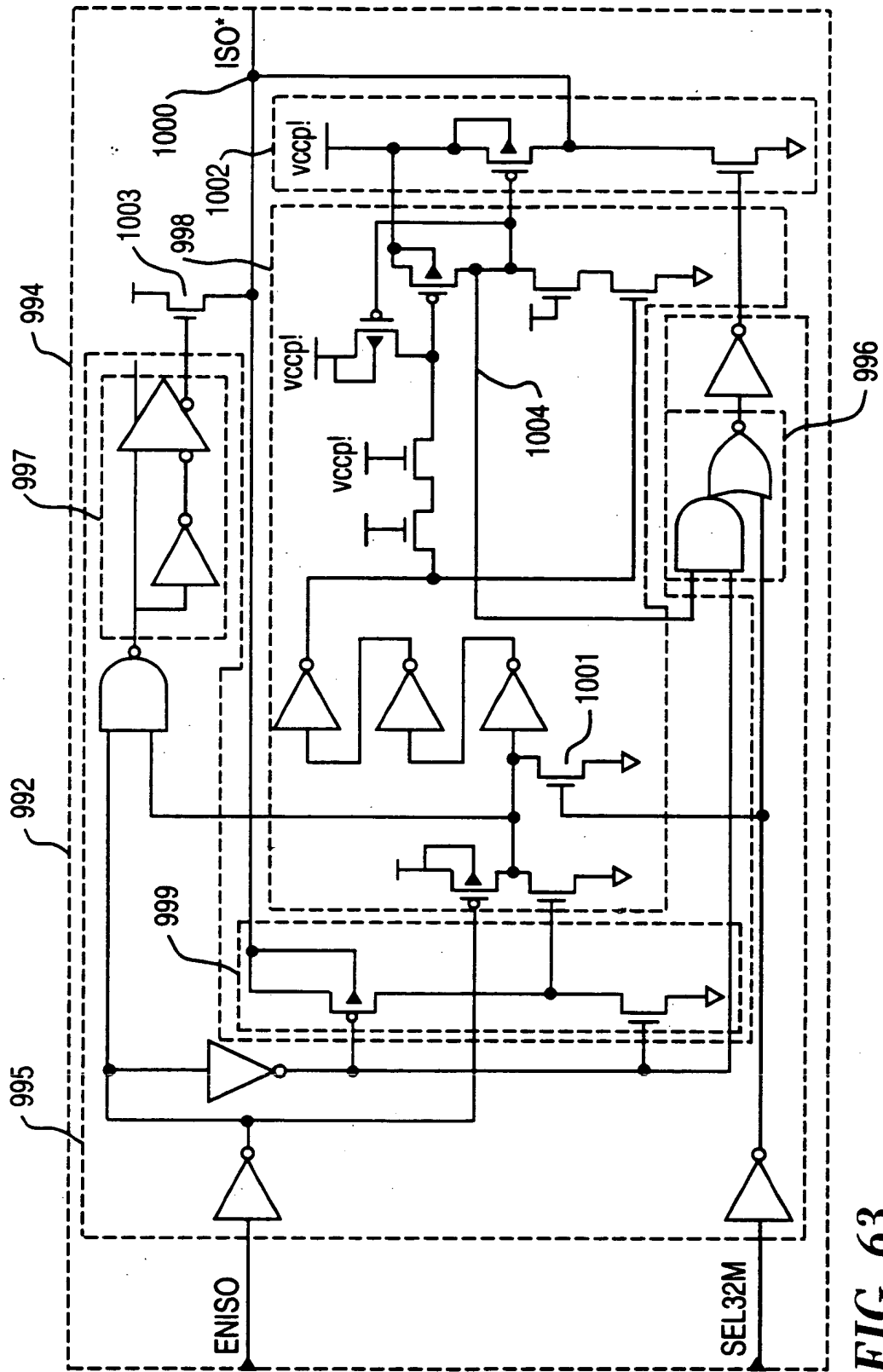


FIG. 63

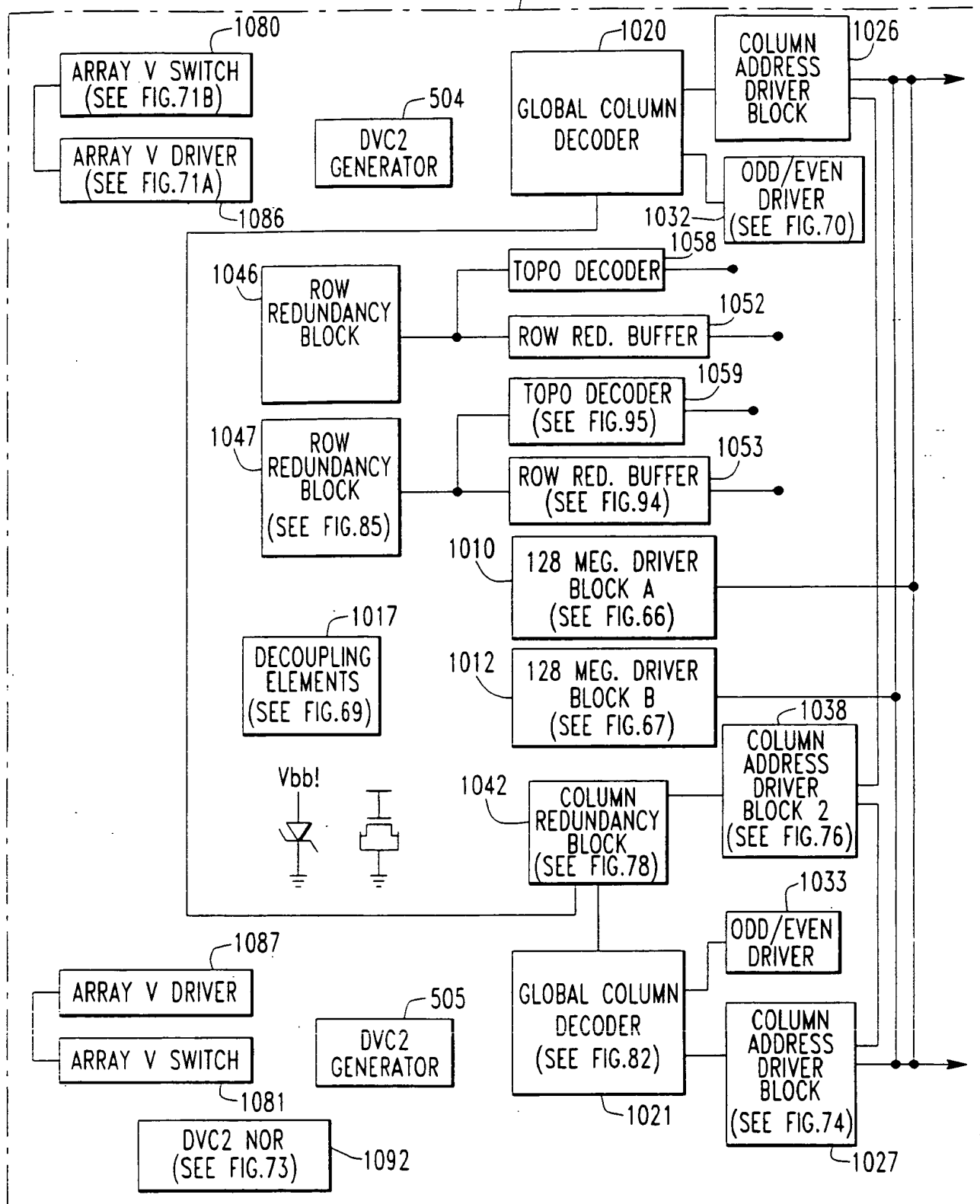


FIG. 64A

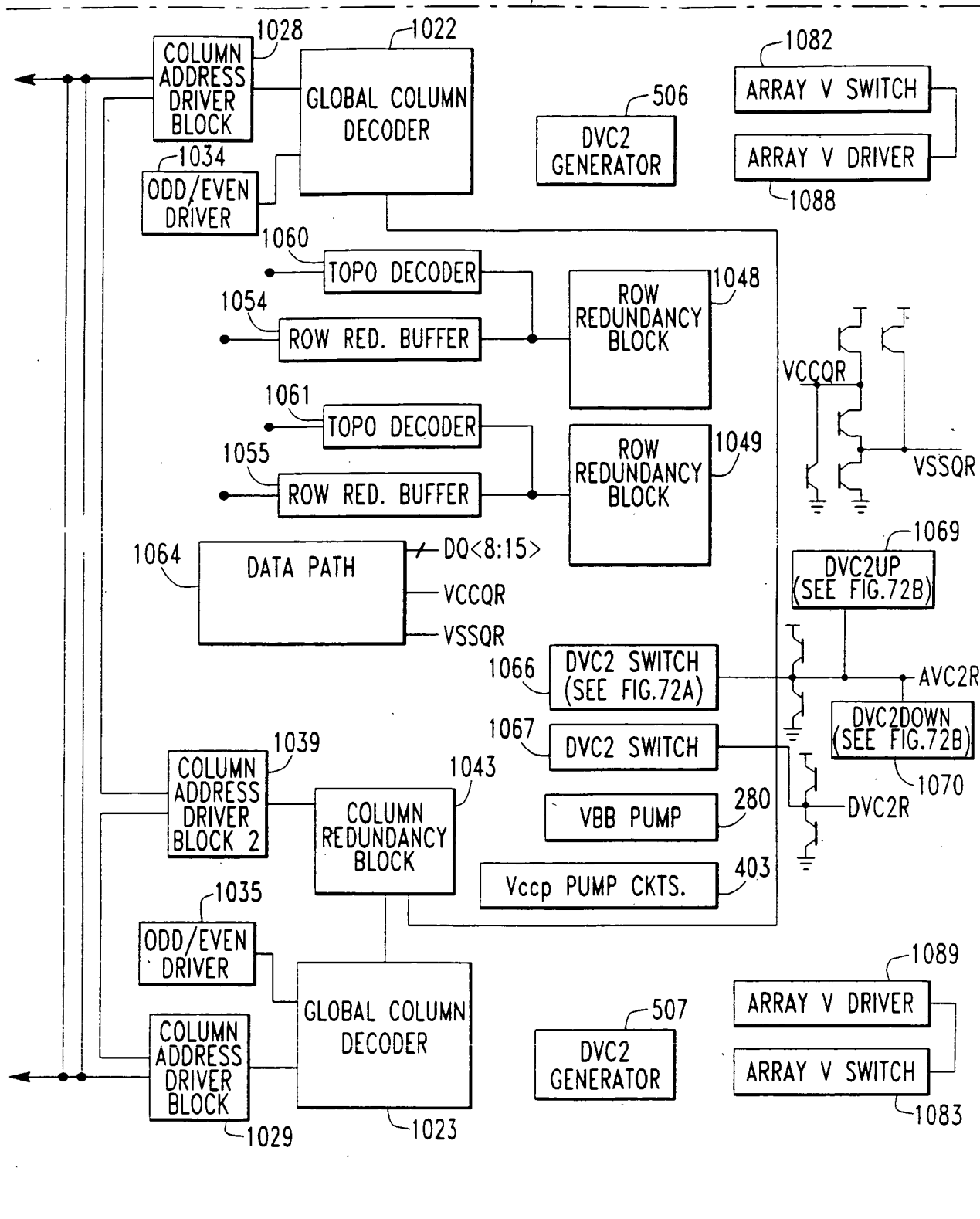


FIG. 64B

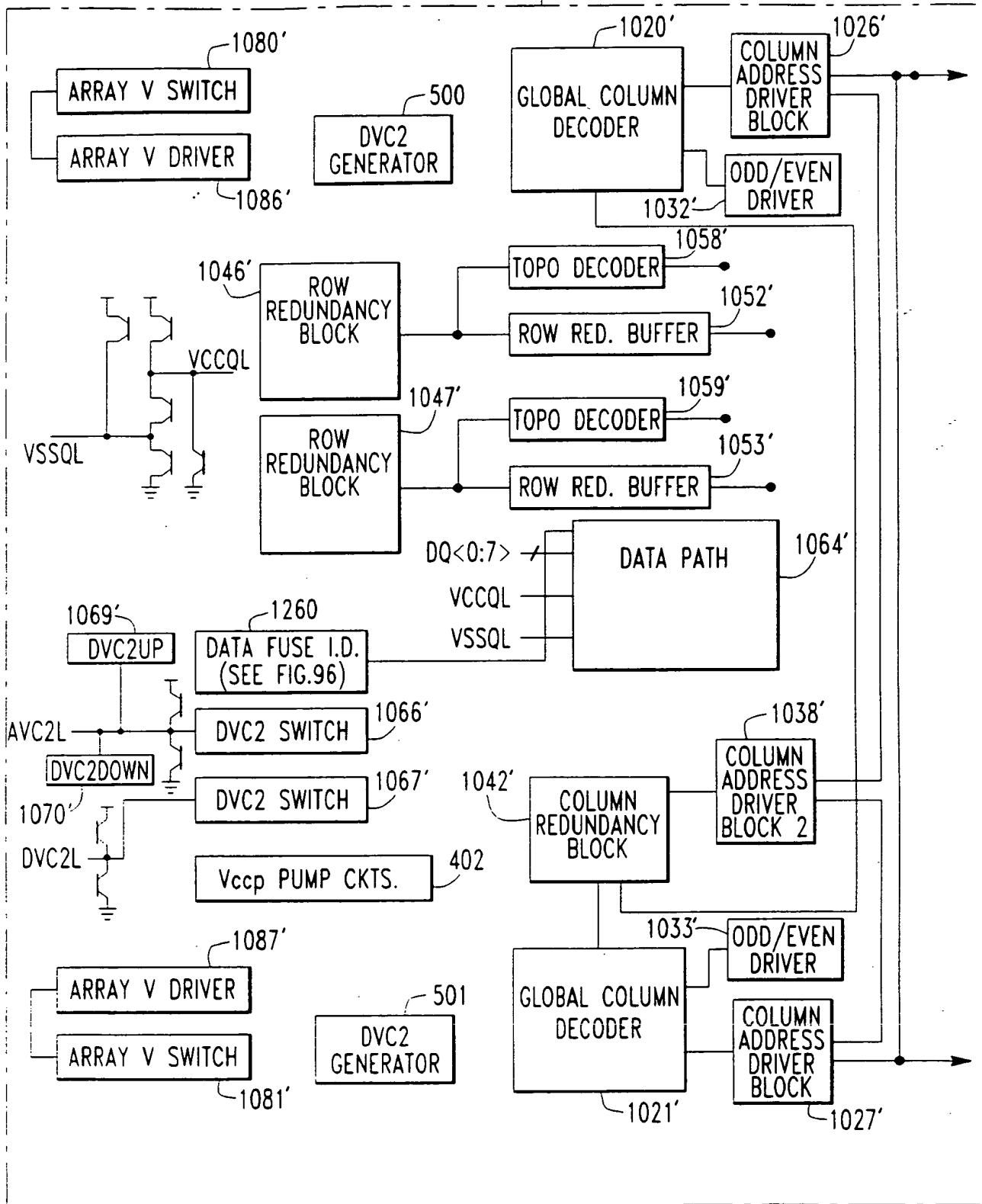


FIG. 65A

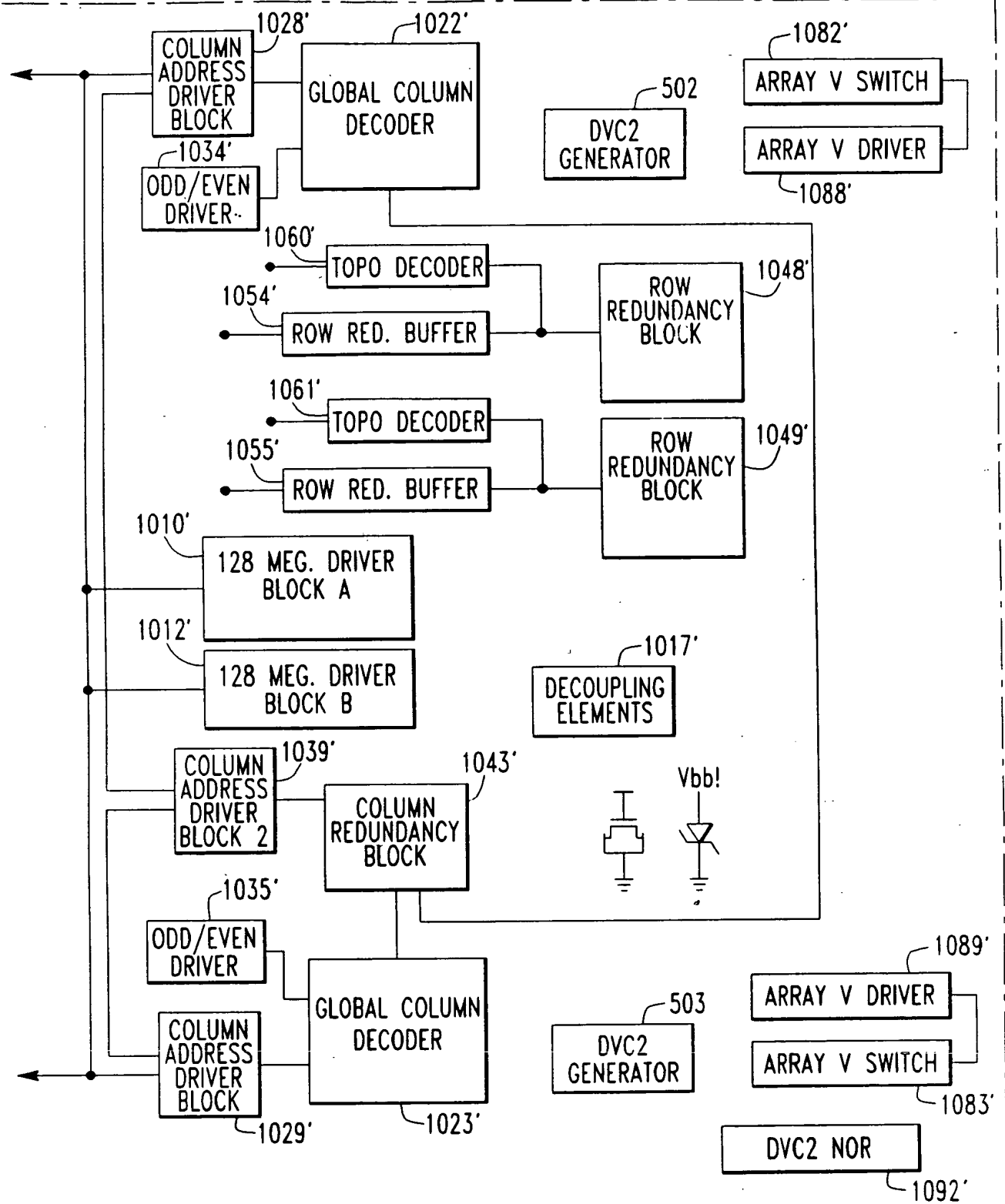


FIG. 65B

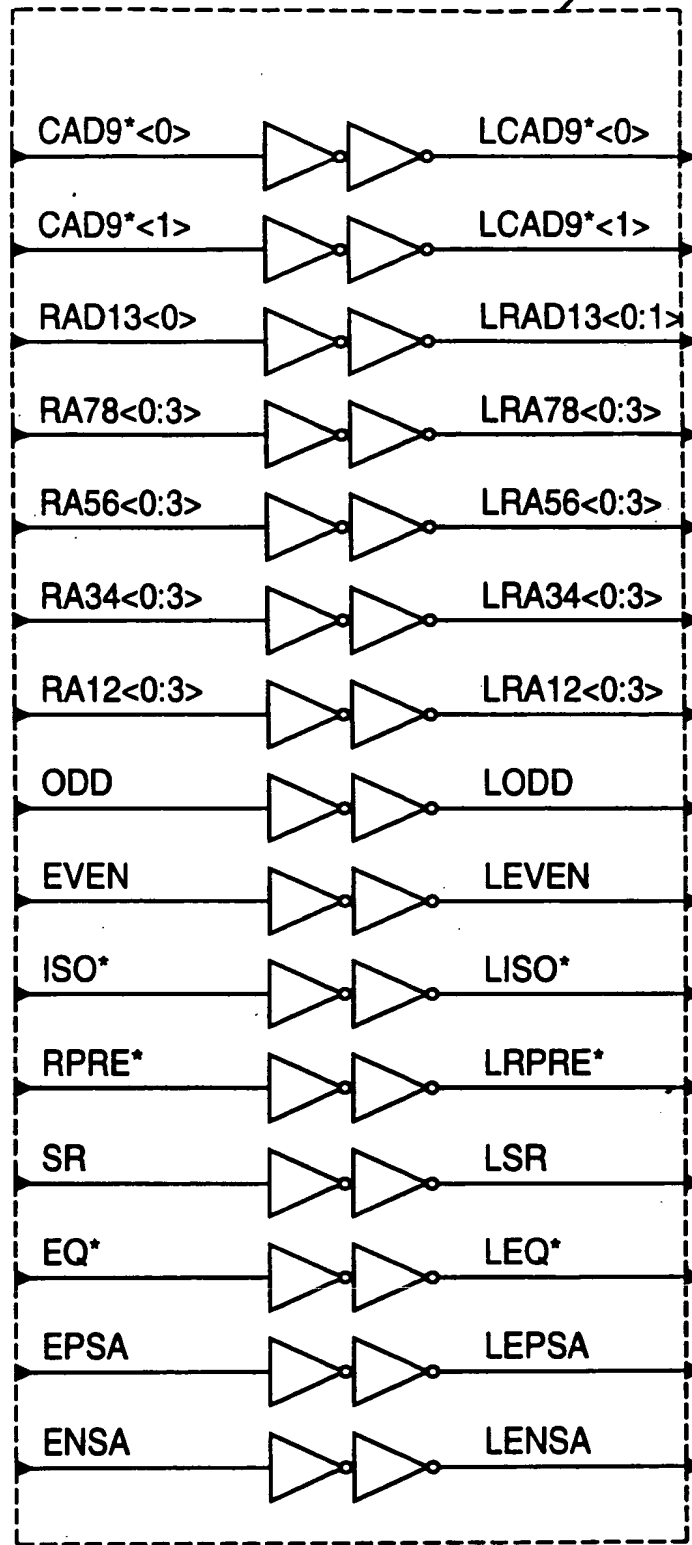


FIG. 66

FIG. 67

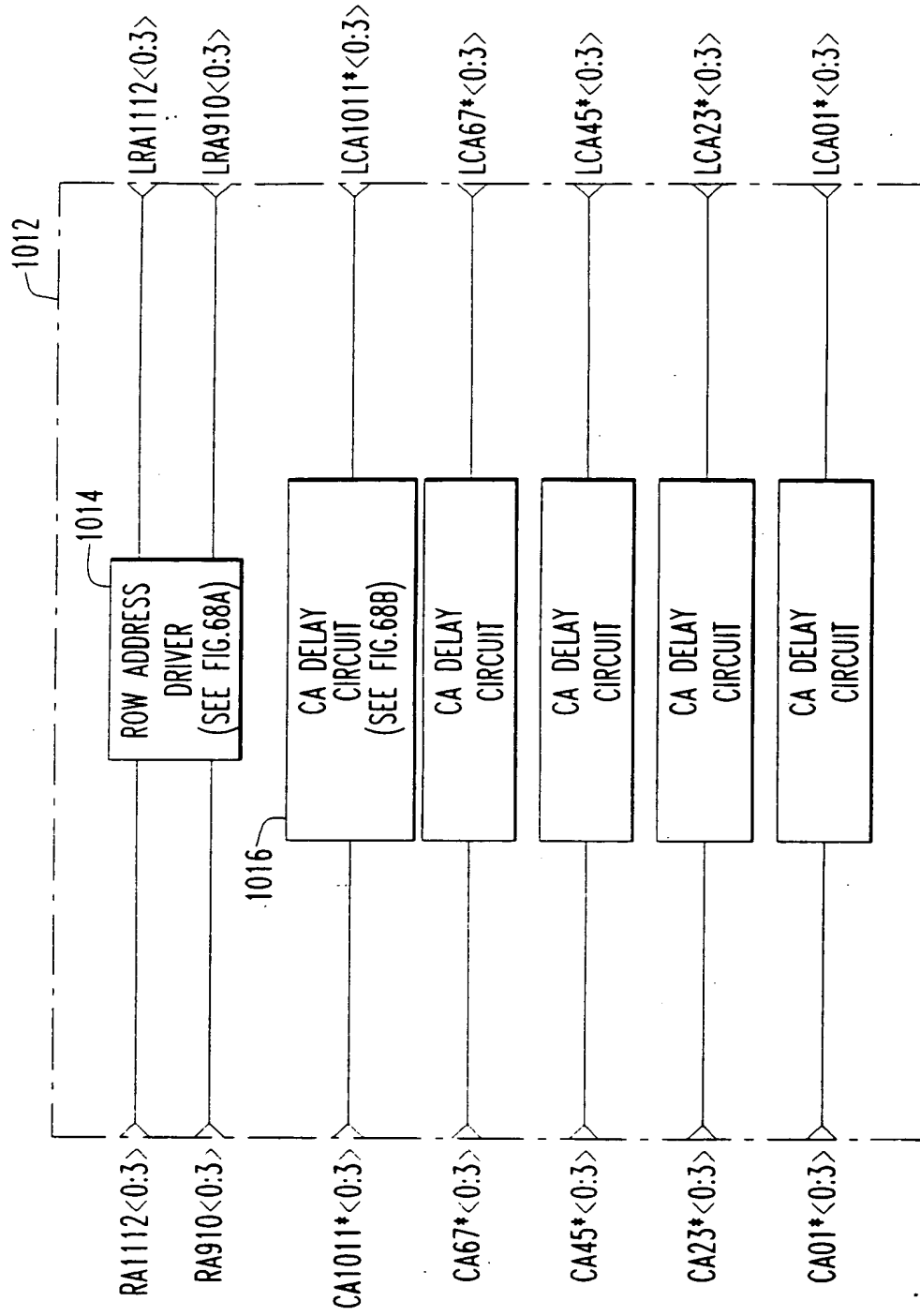
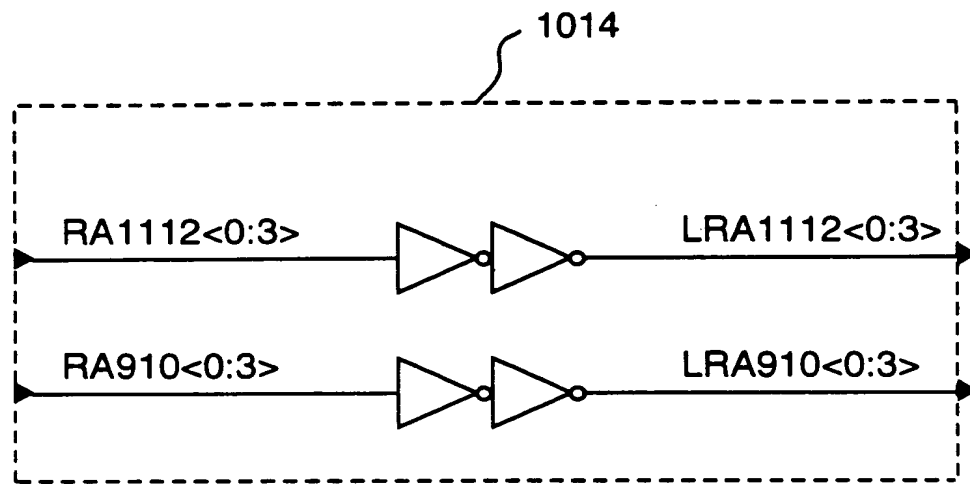


FIG. 67

**FIG. 68A**

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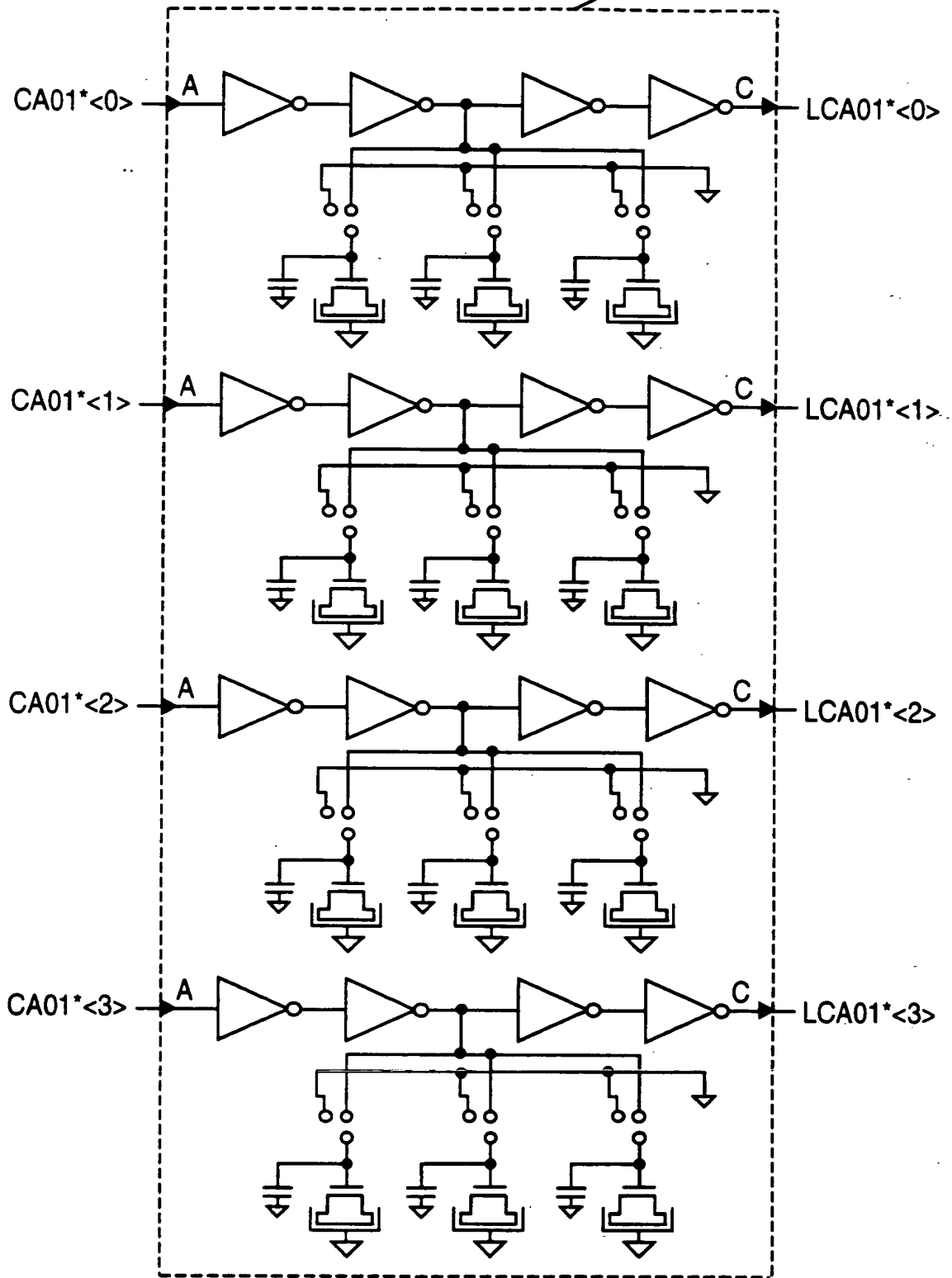
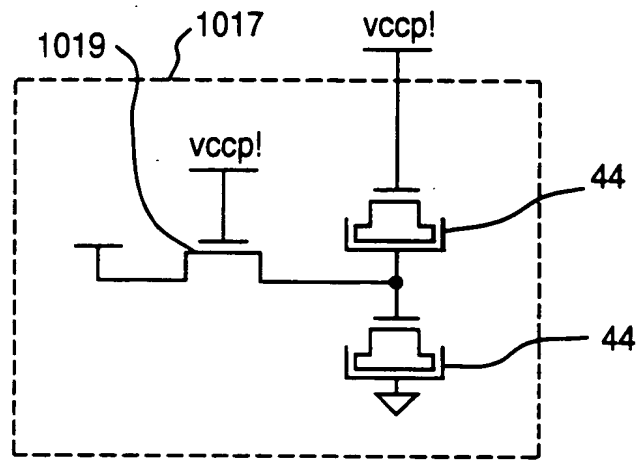
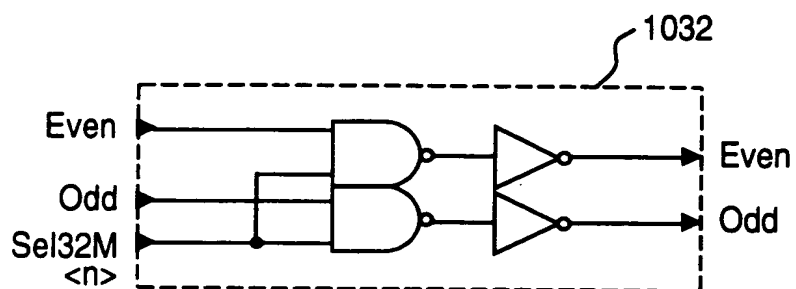


FIG. 68B

**FIG. 69**

**FIG. 70**

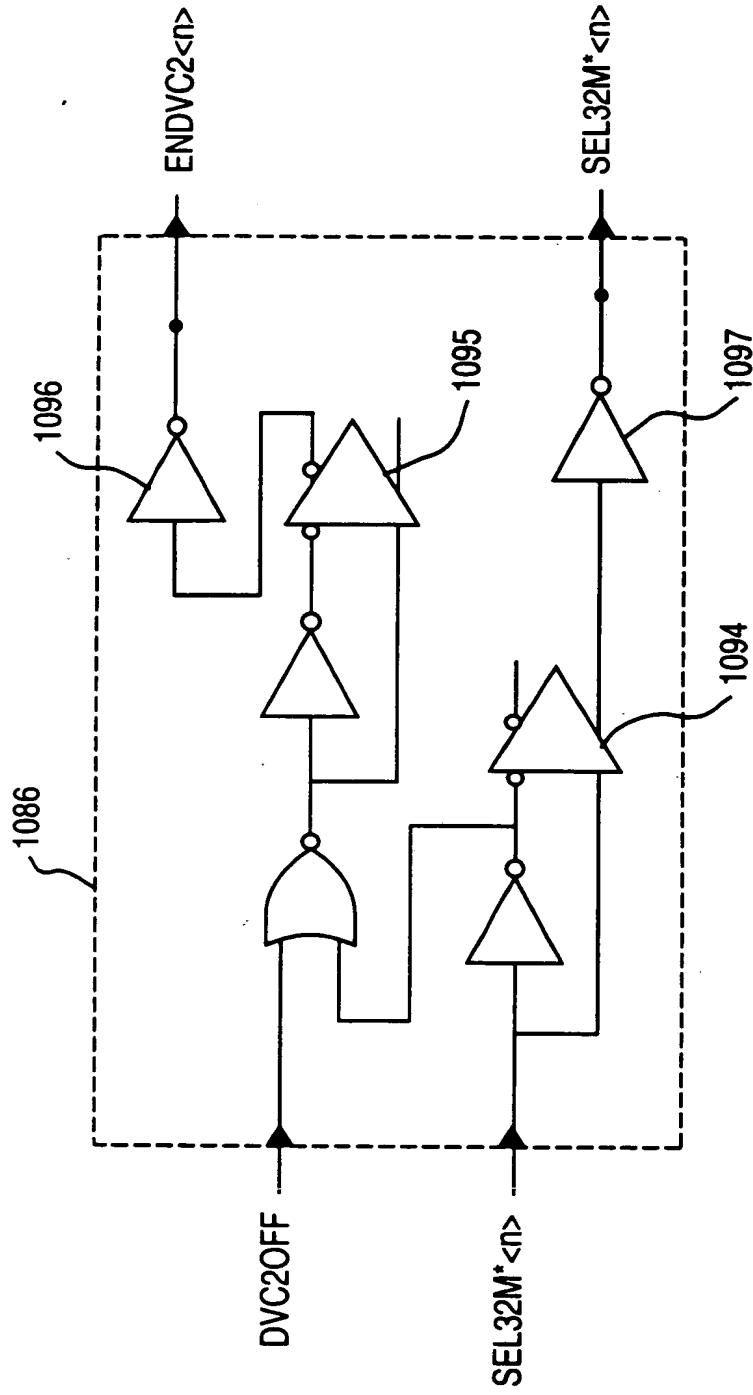
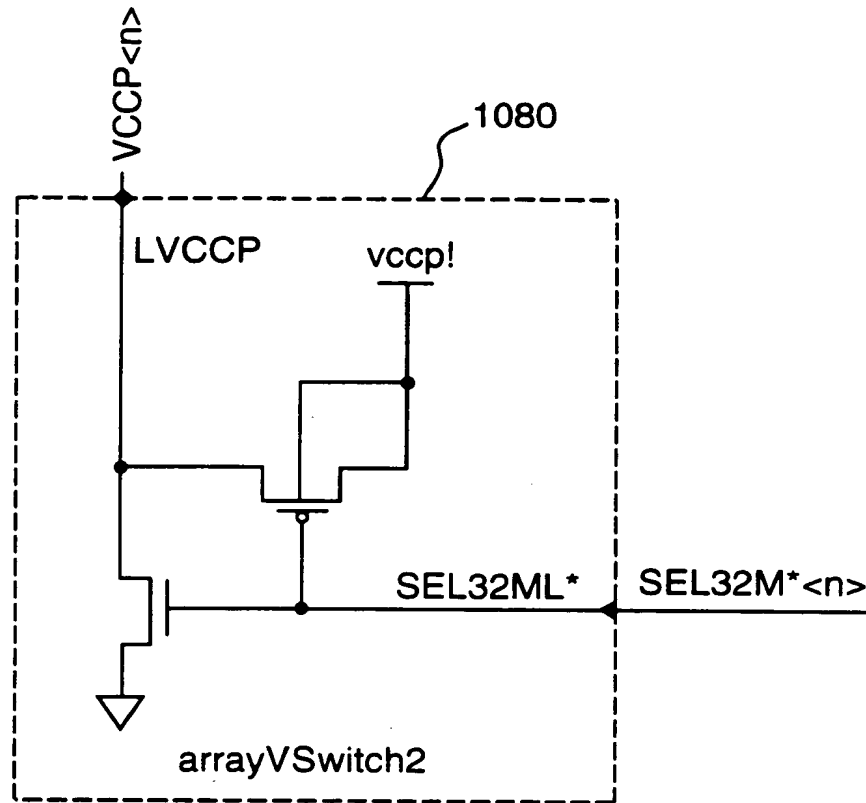


FIG. 71A

**FIG. 71B**

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102280 56/42660

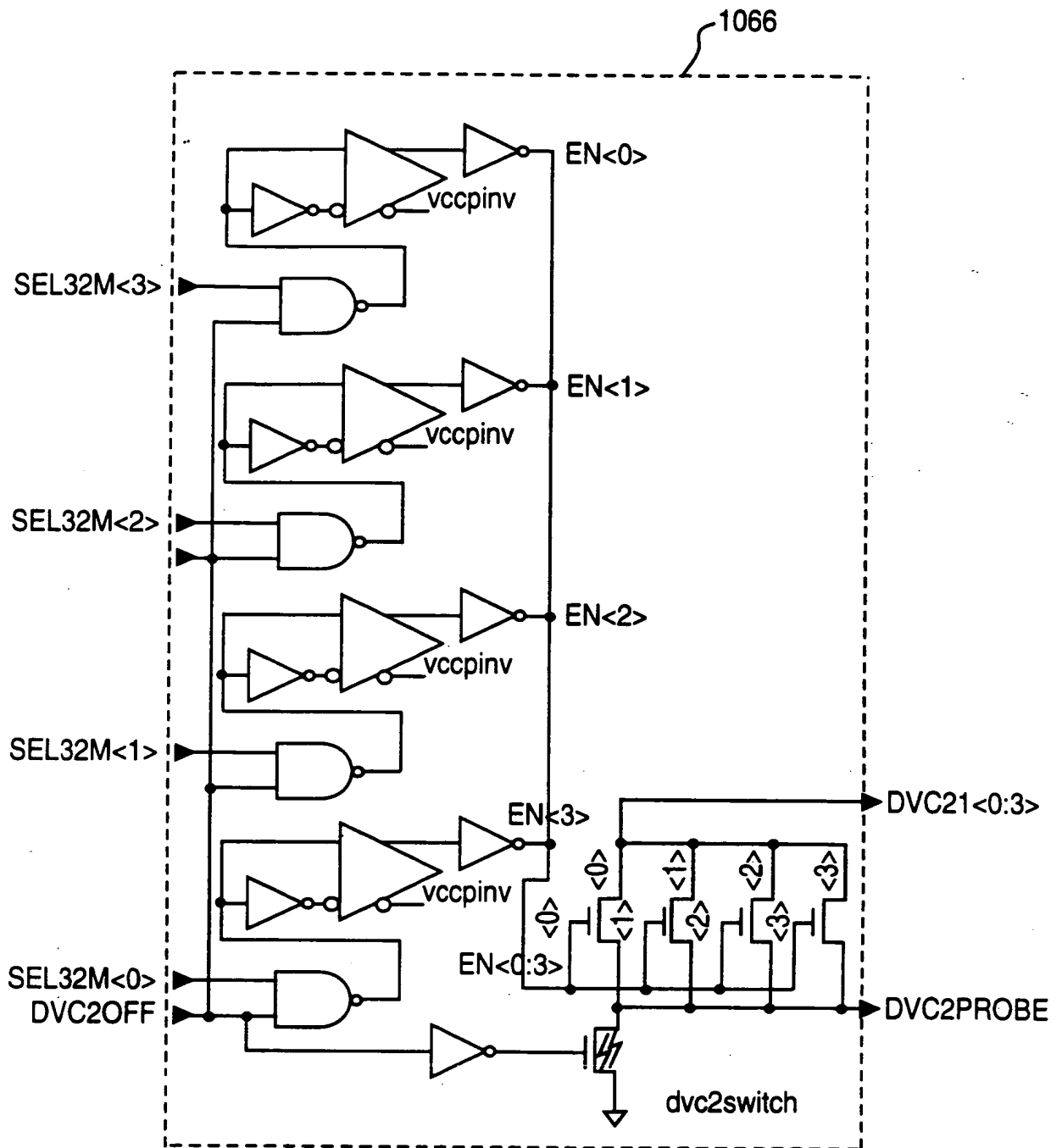
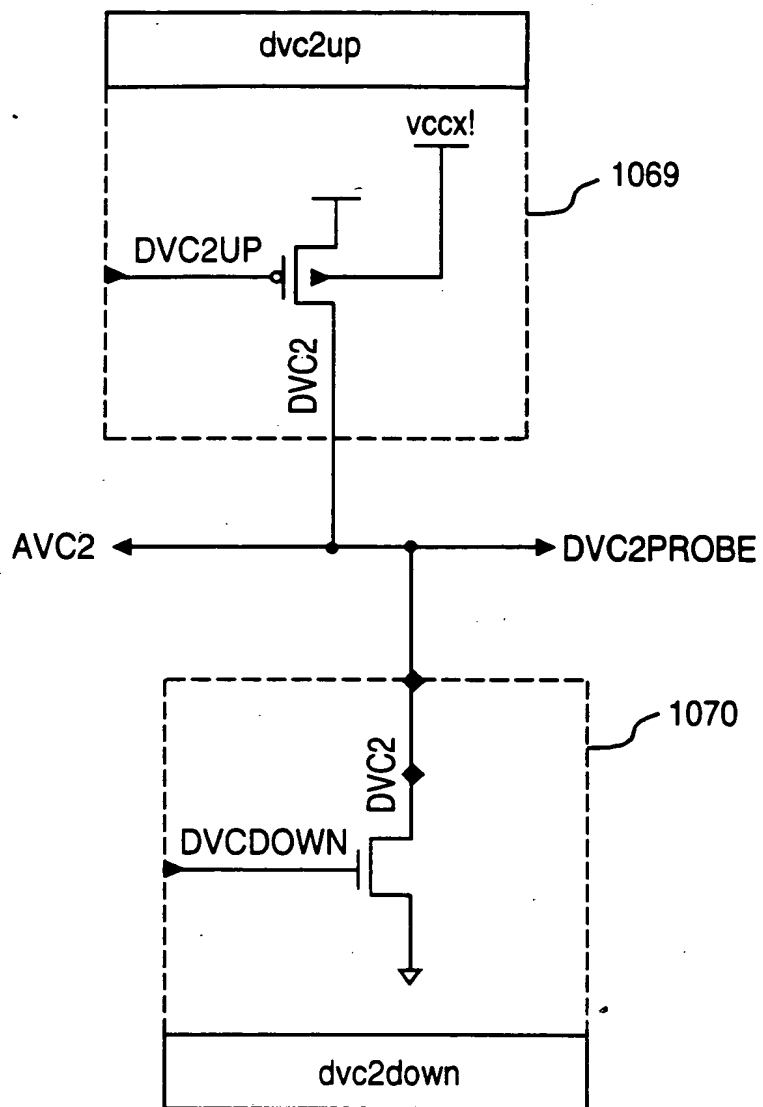


FIG. 72A

**FIG. 72B**

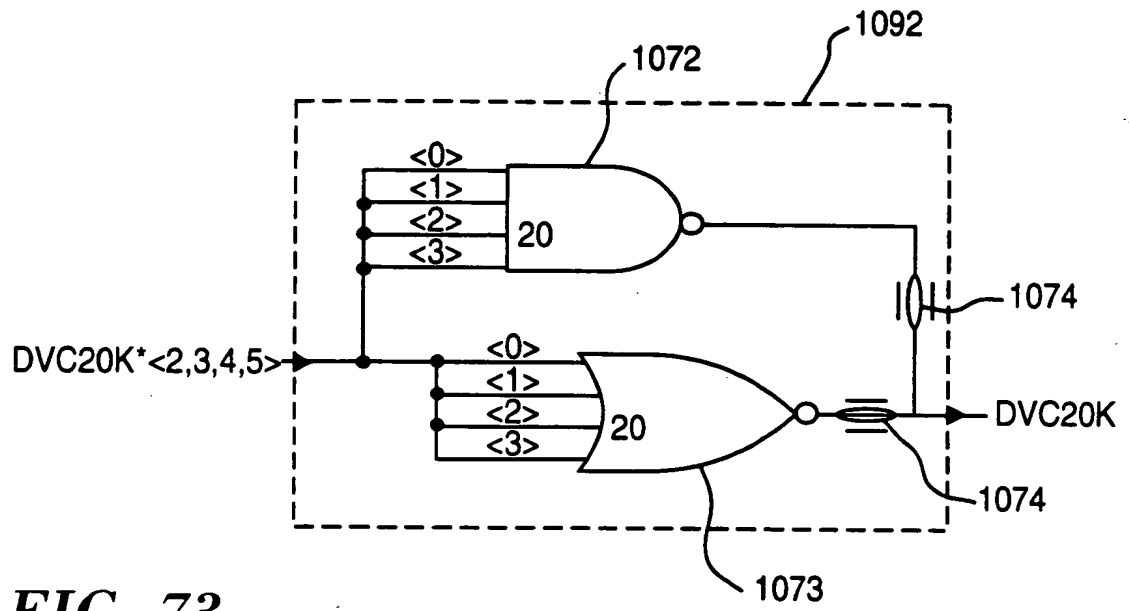


FIG. 73

FIG. 74

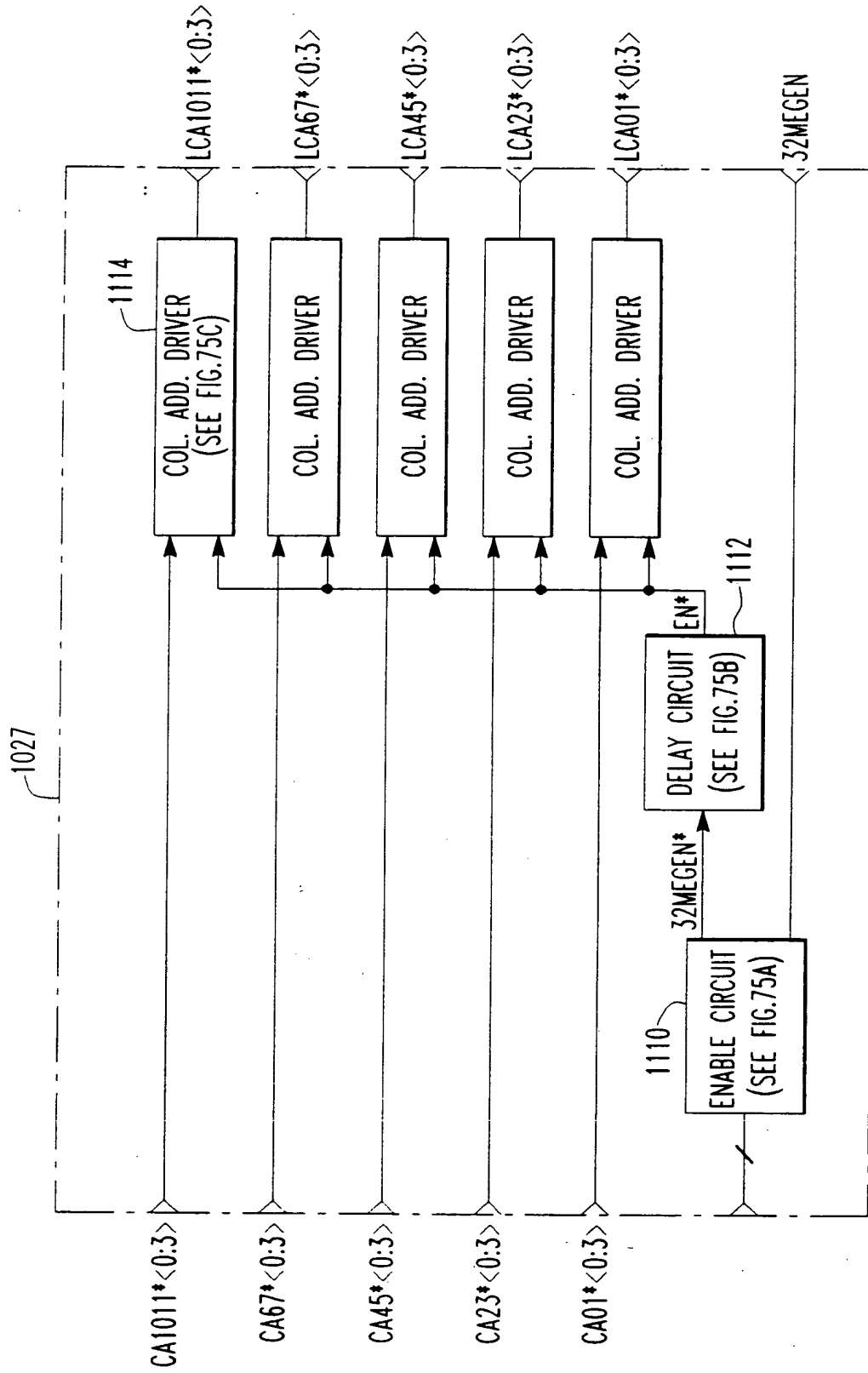


FIG. 74

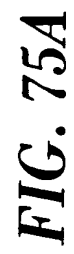


FIG. 75A

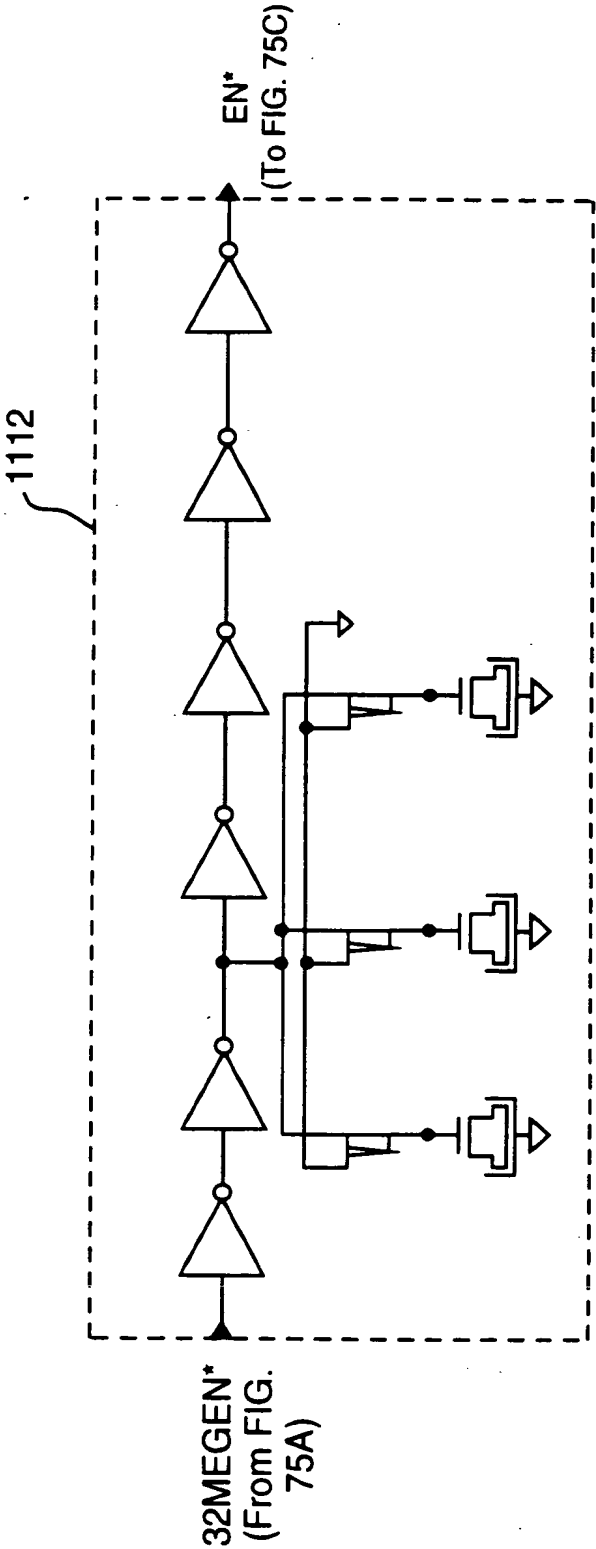


FIG. 75B

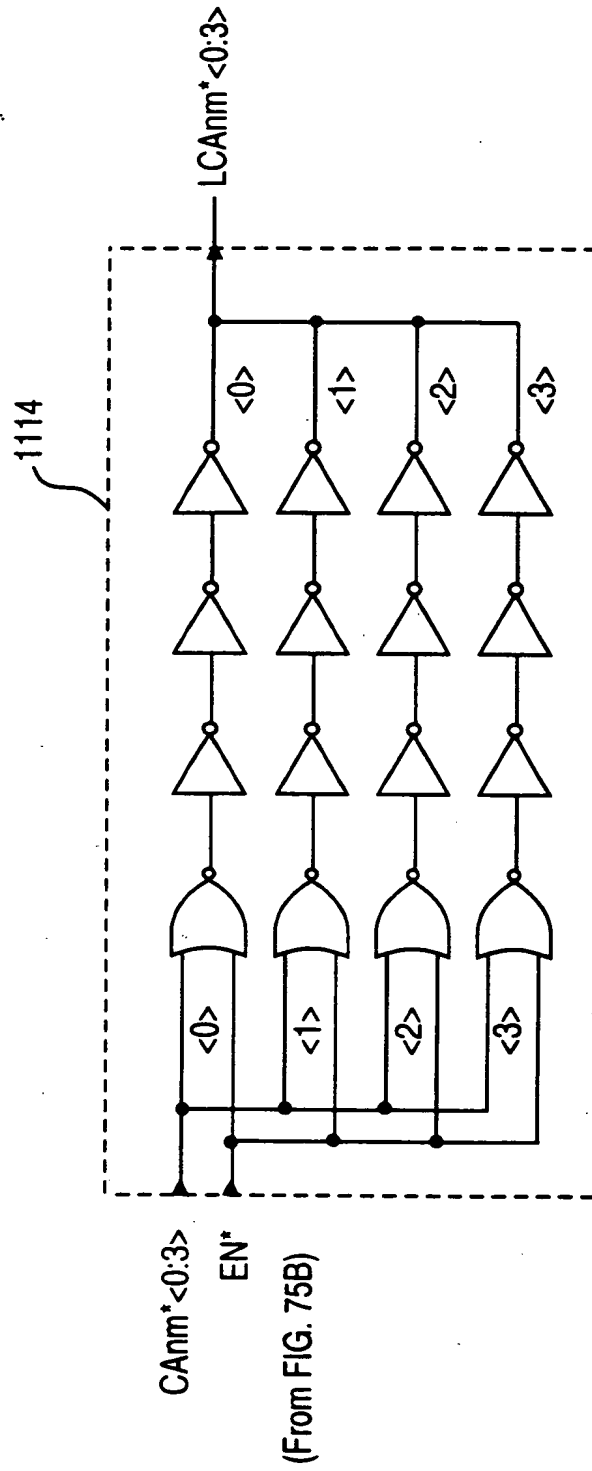


FIG. 75C

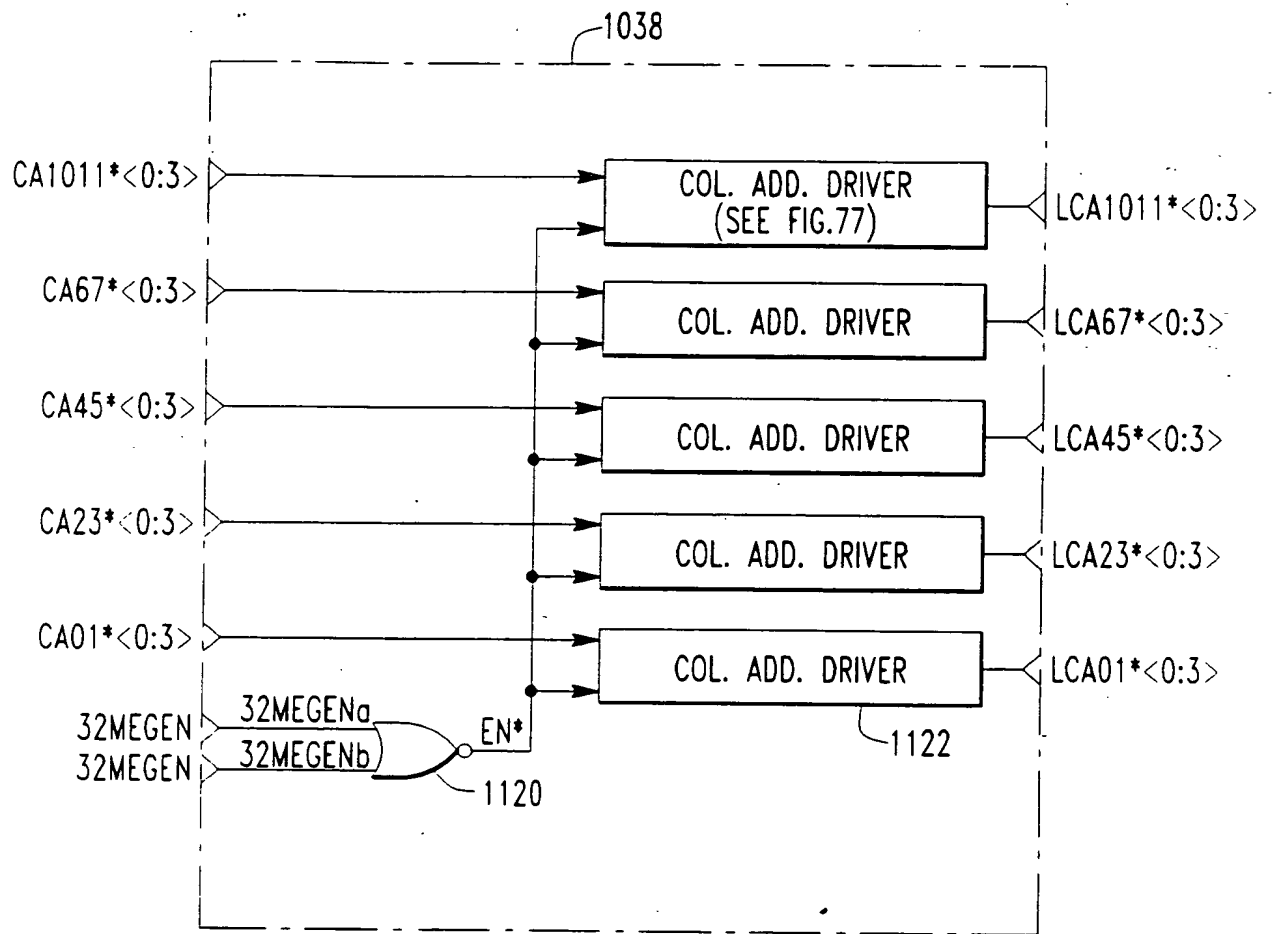
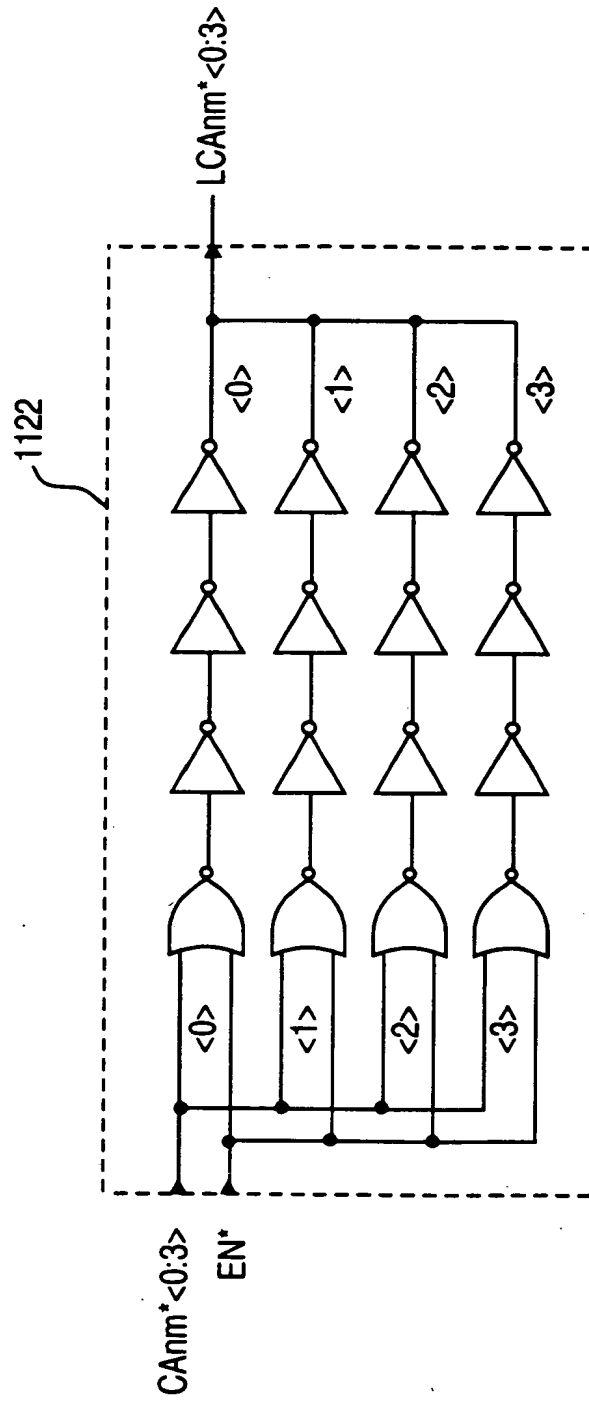


FIG. 76



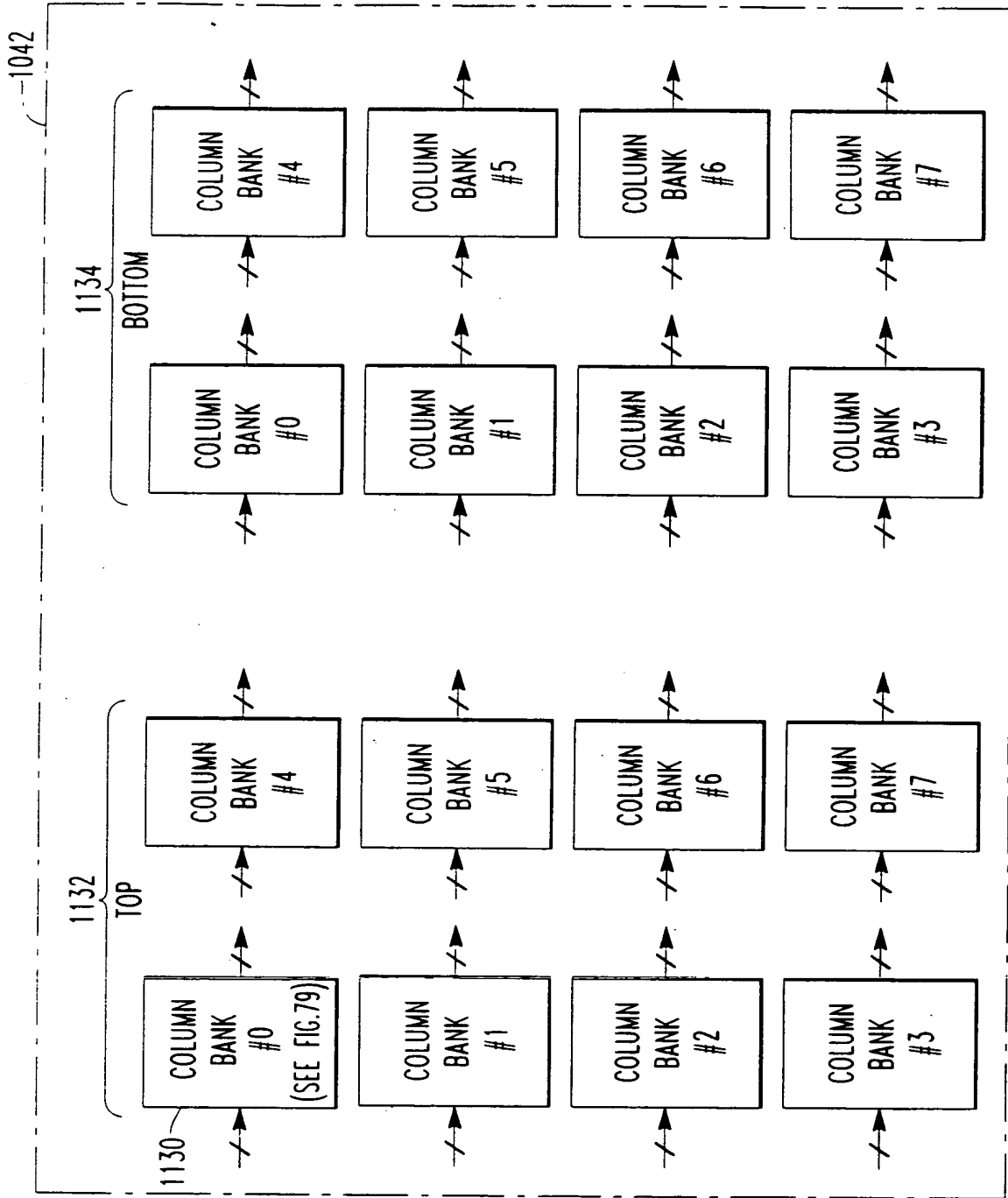
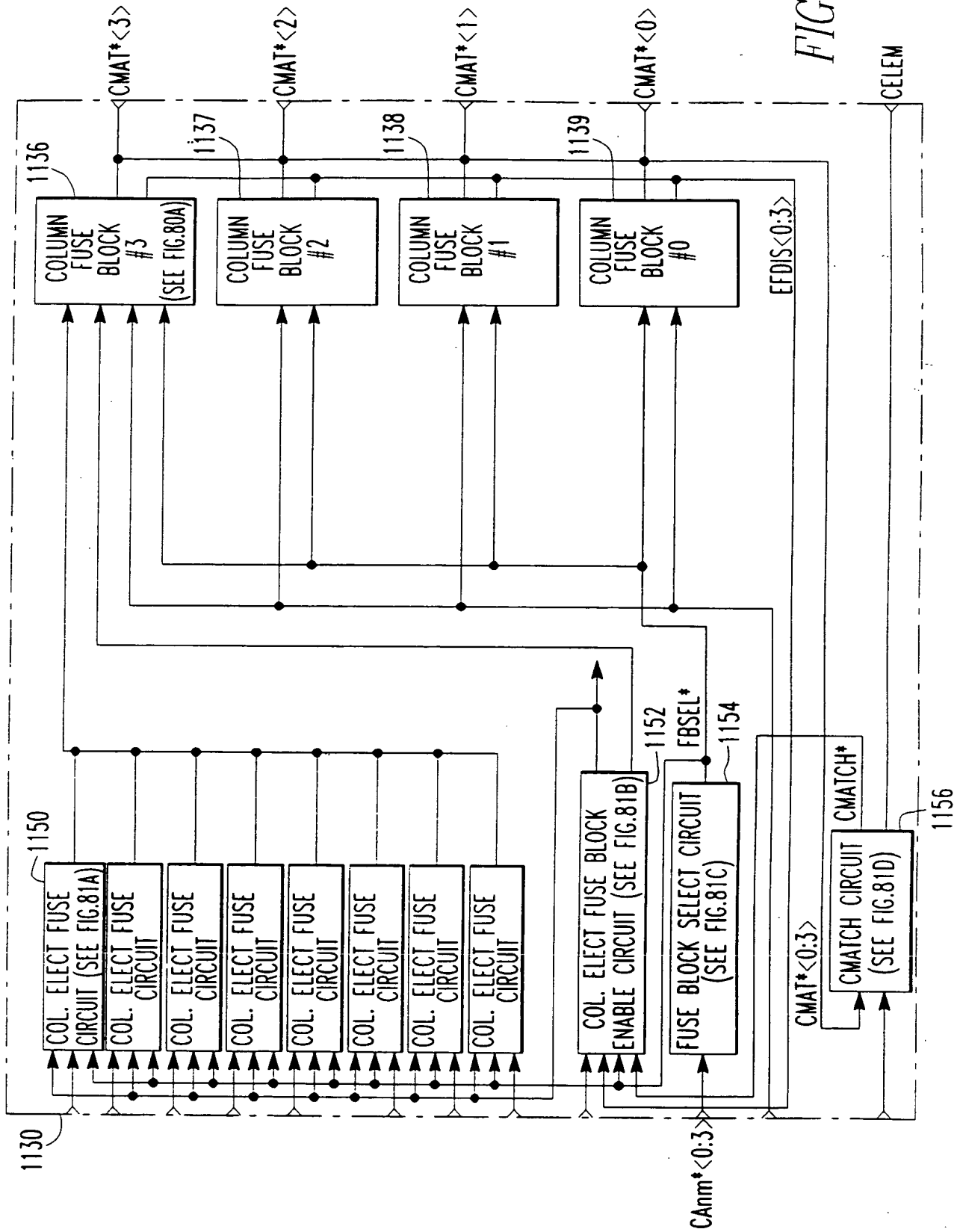


FIG. 78

FIG. 79



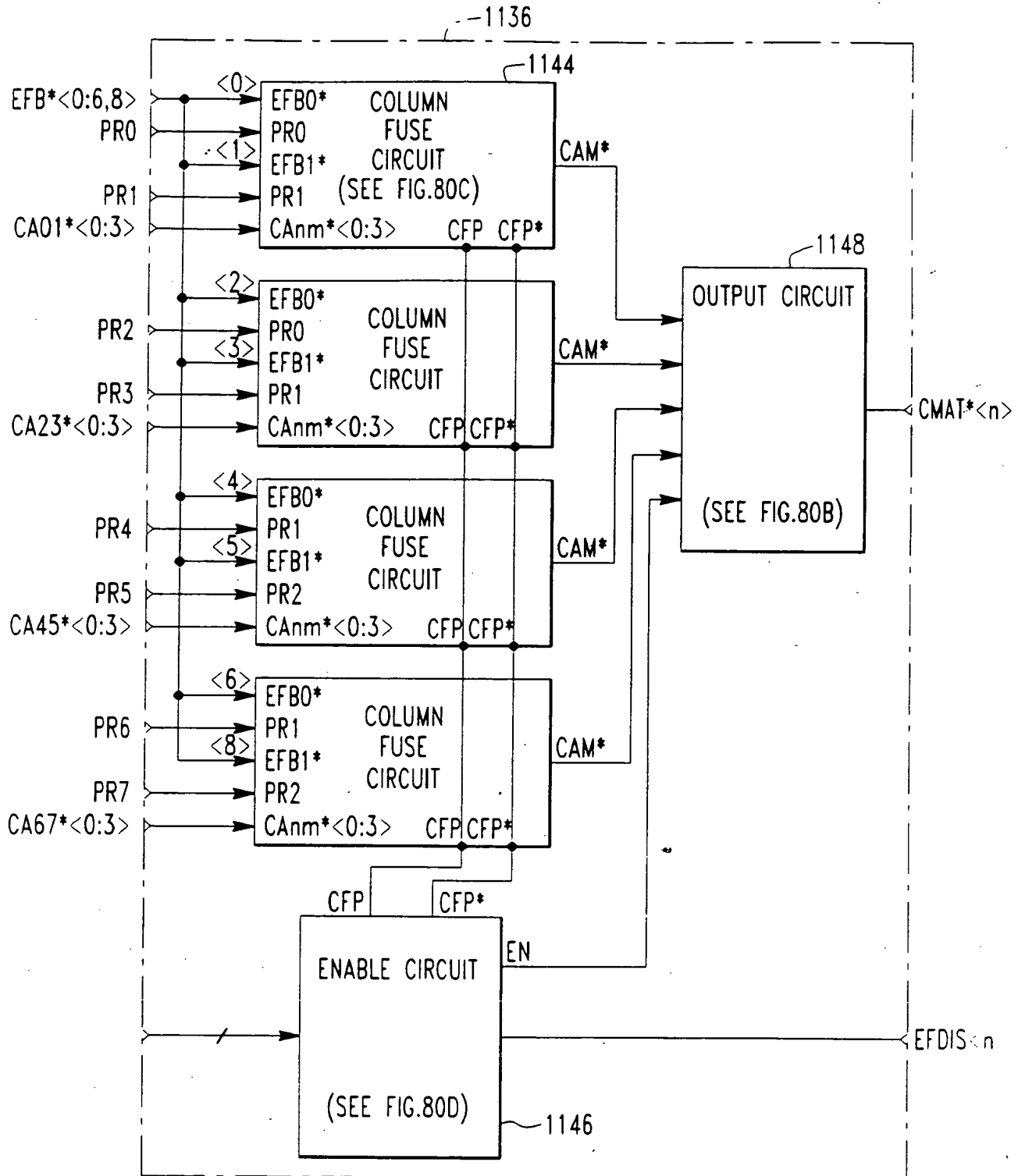
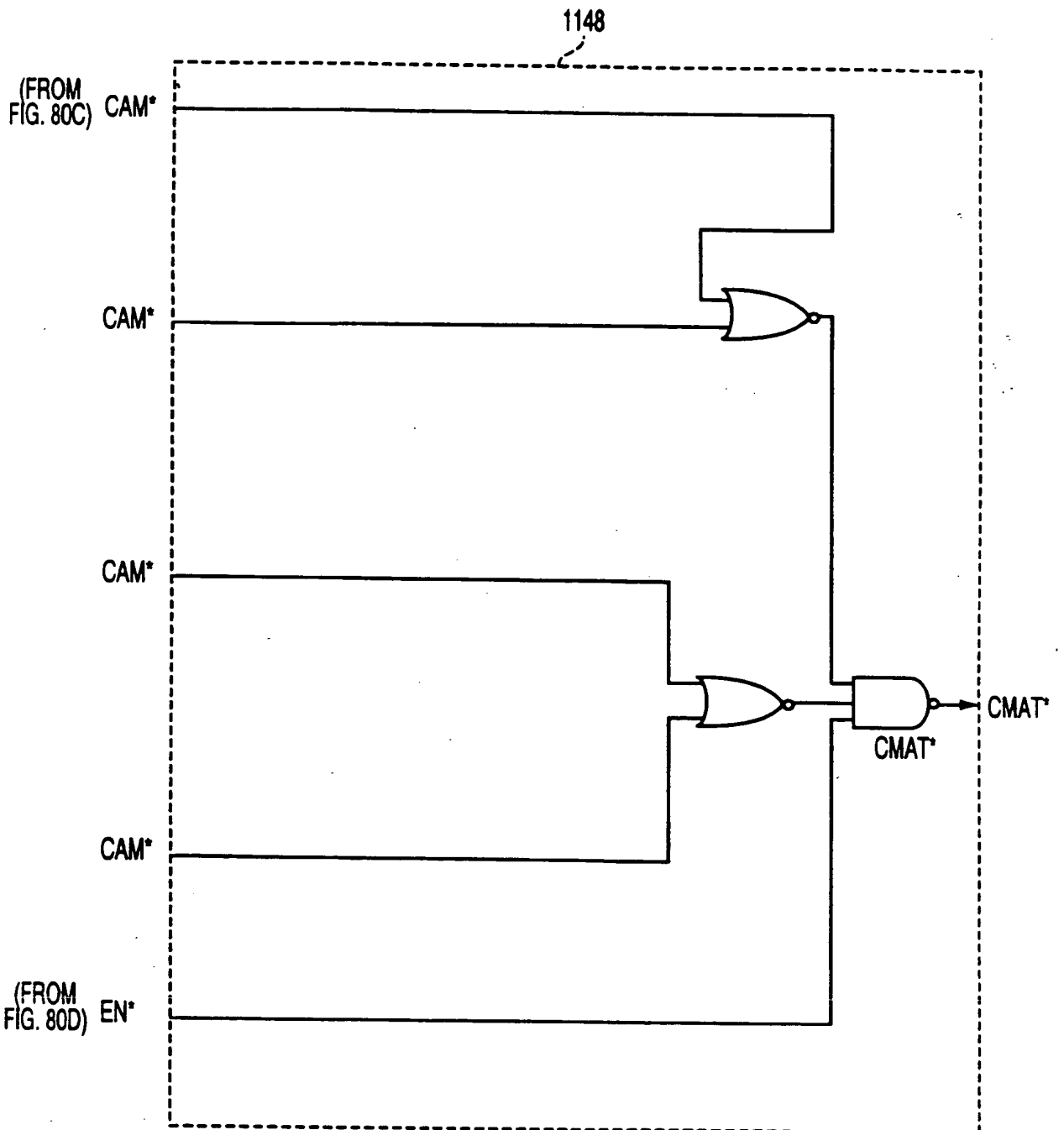
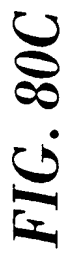


FIG. 80A

**FIG. 80B**



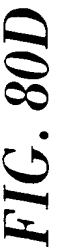


FIG. 81A

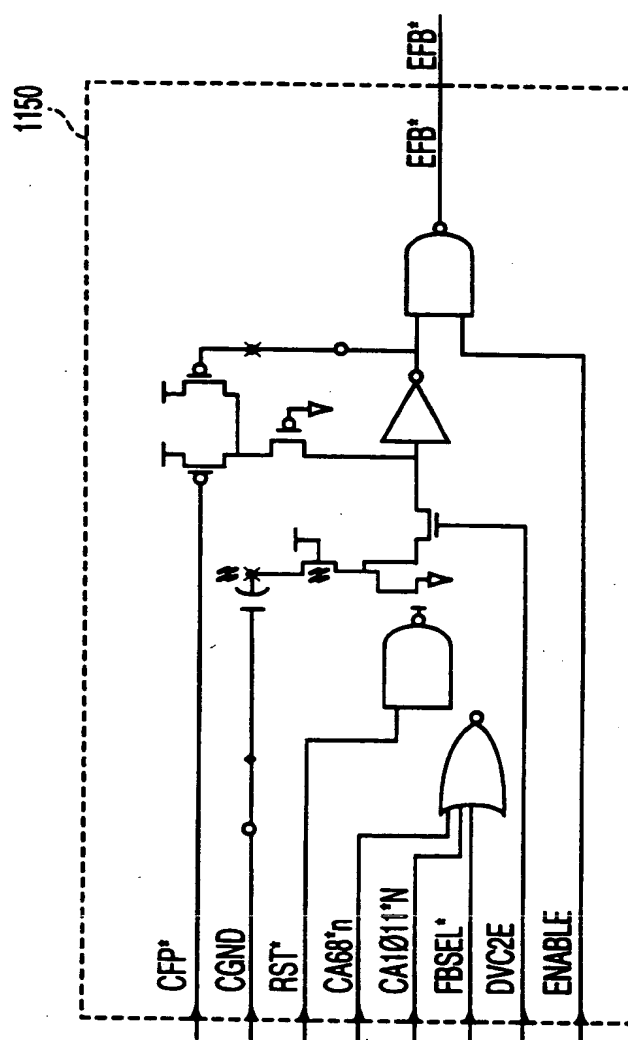


FIG. 81A

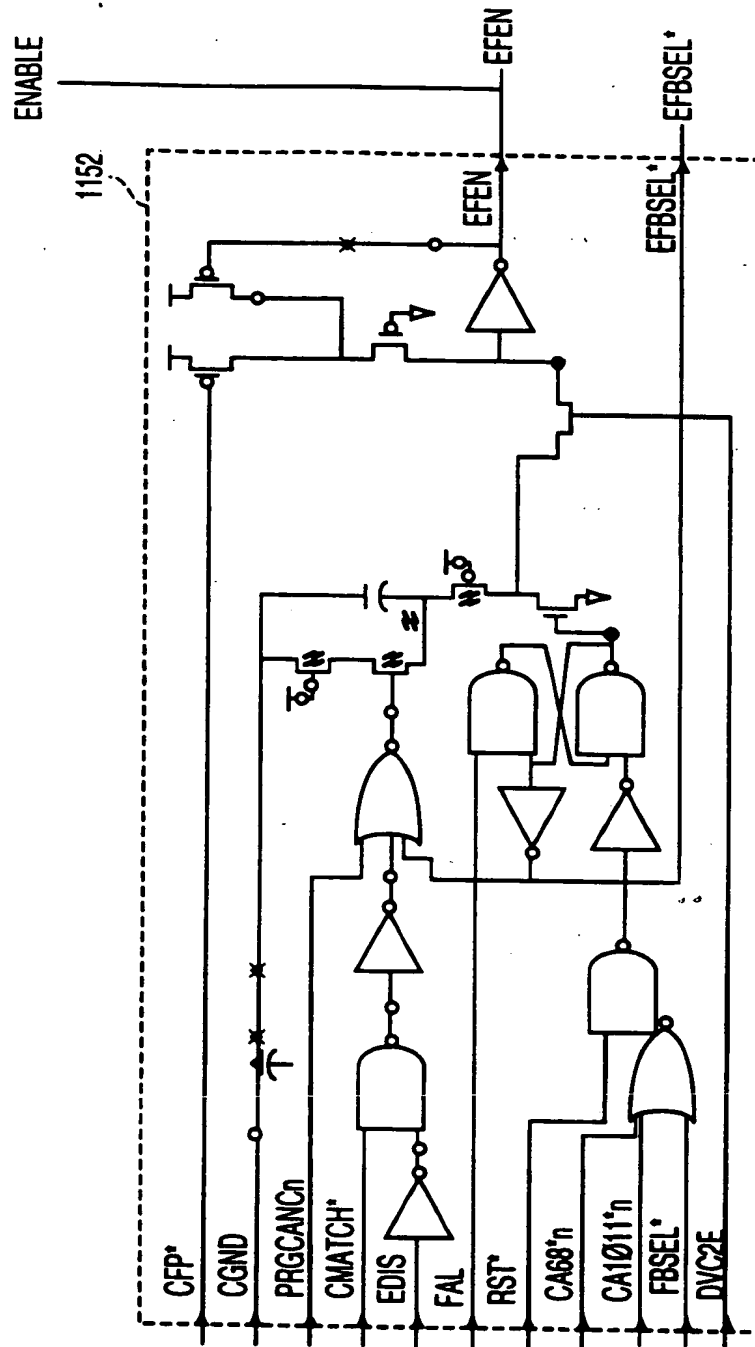


FIG. 81B

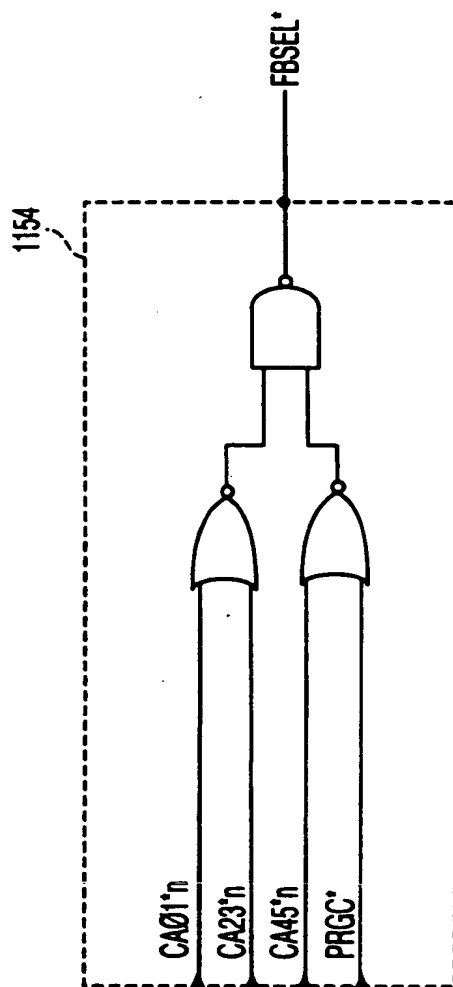


FIG. 81C

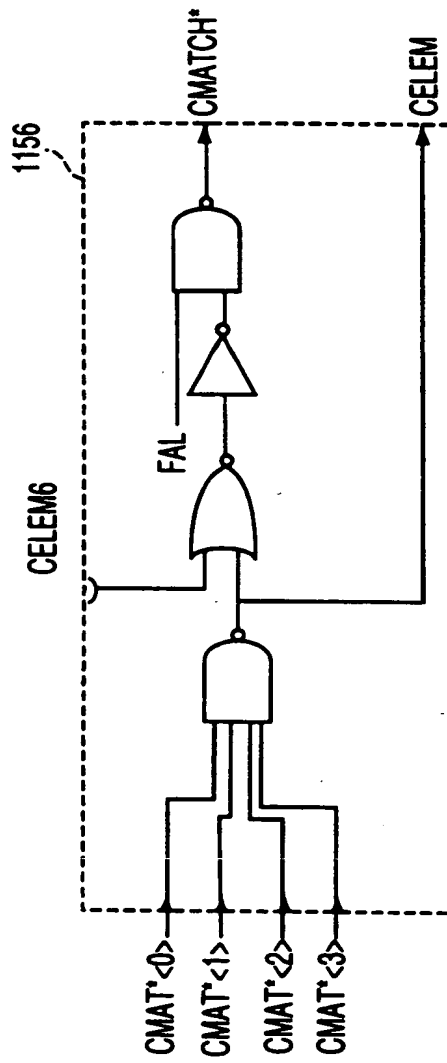


FIG. 81D

FIG. 81D 56/4E660

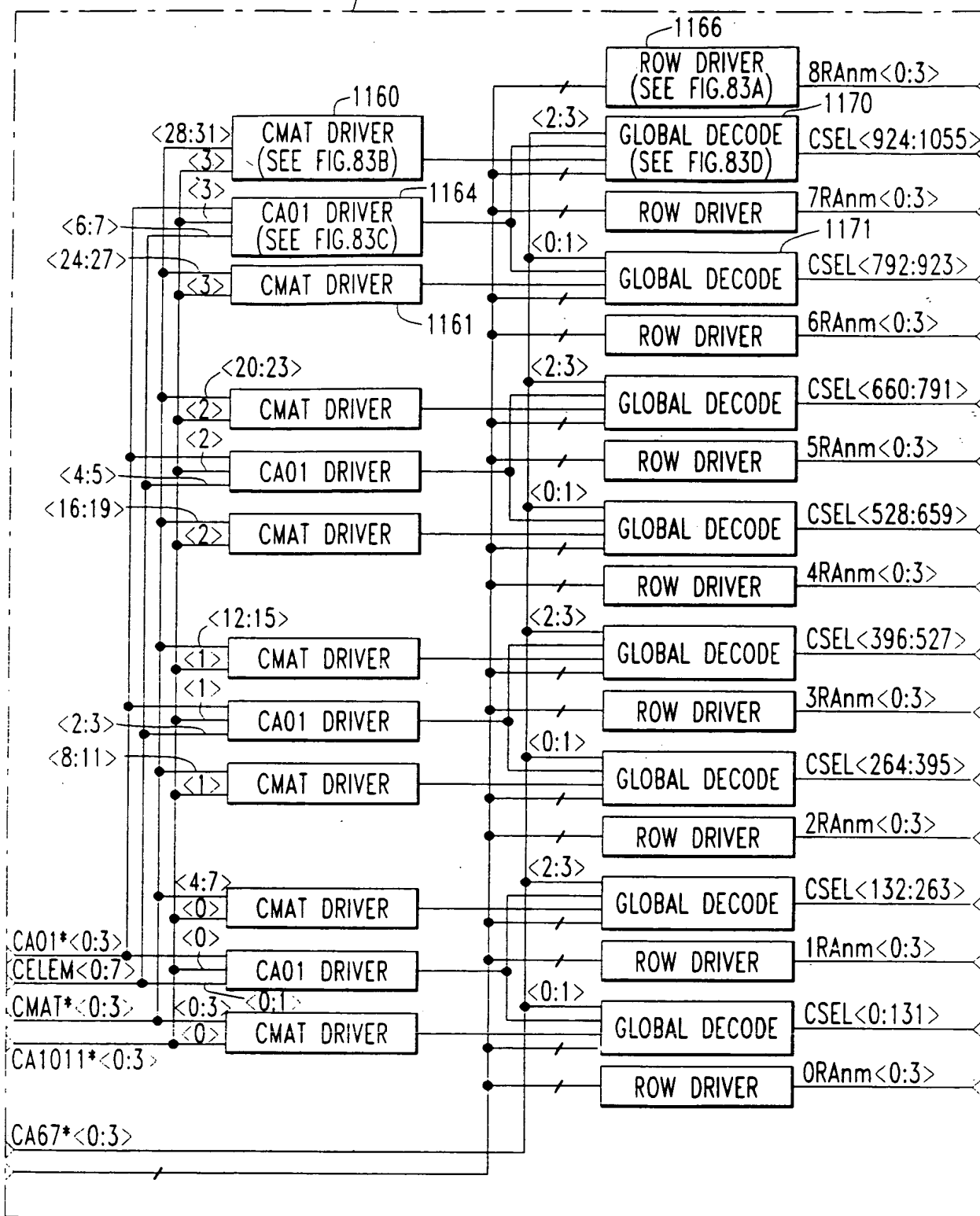


FIG. 82

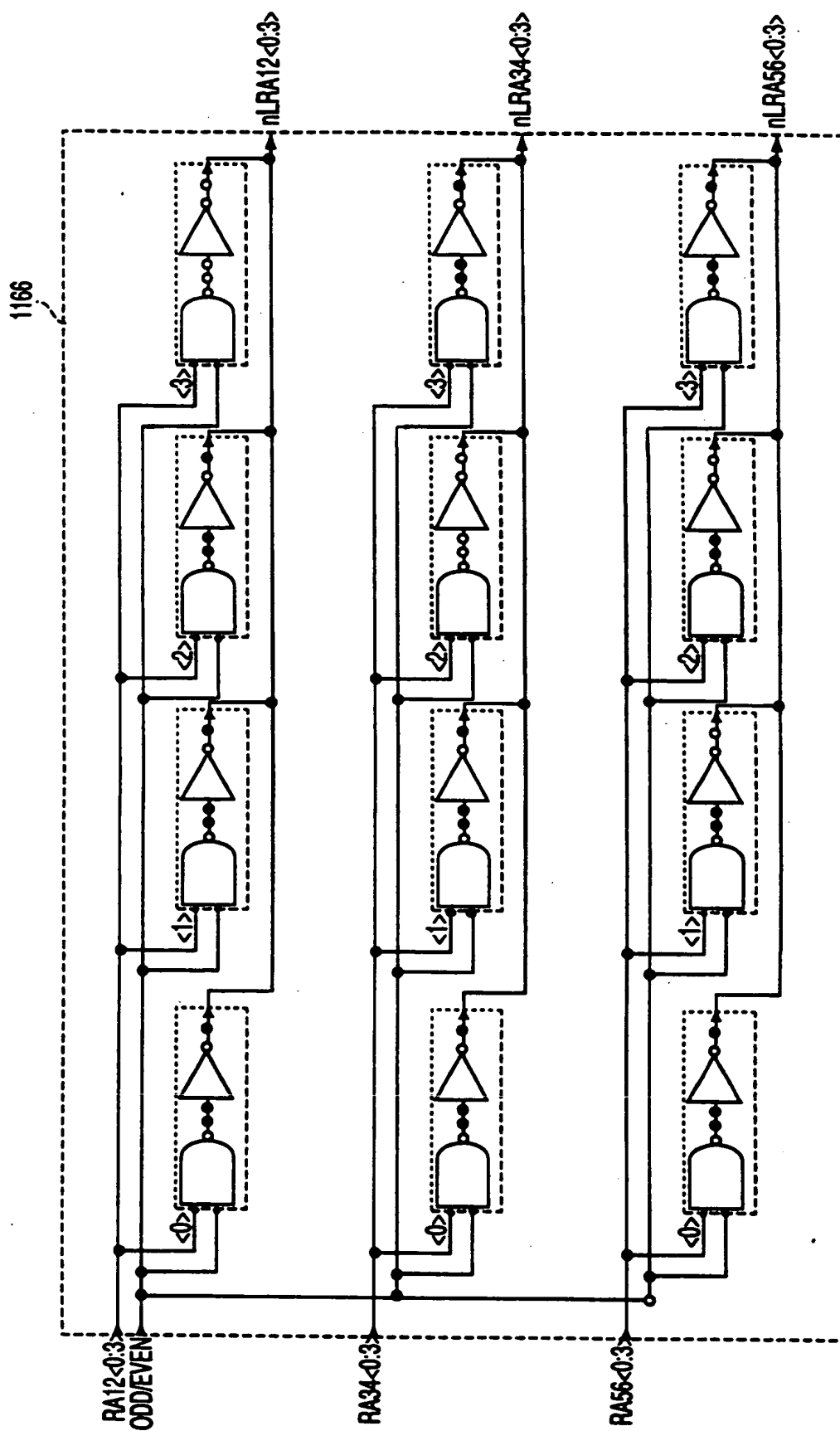


FIG. 83A

FO2280 5624E660

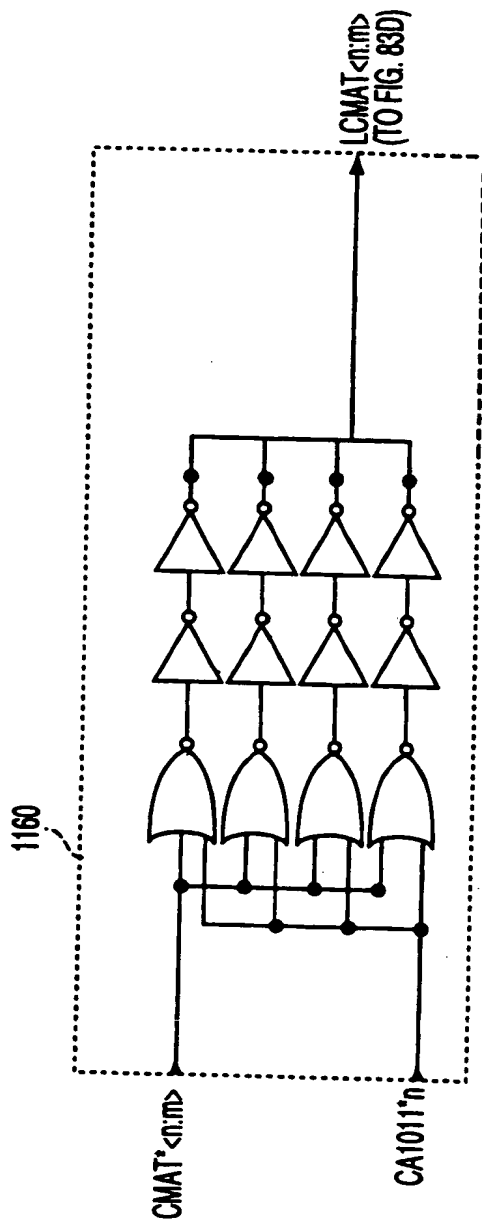


FIG. 83B

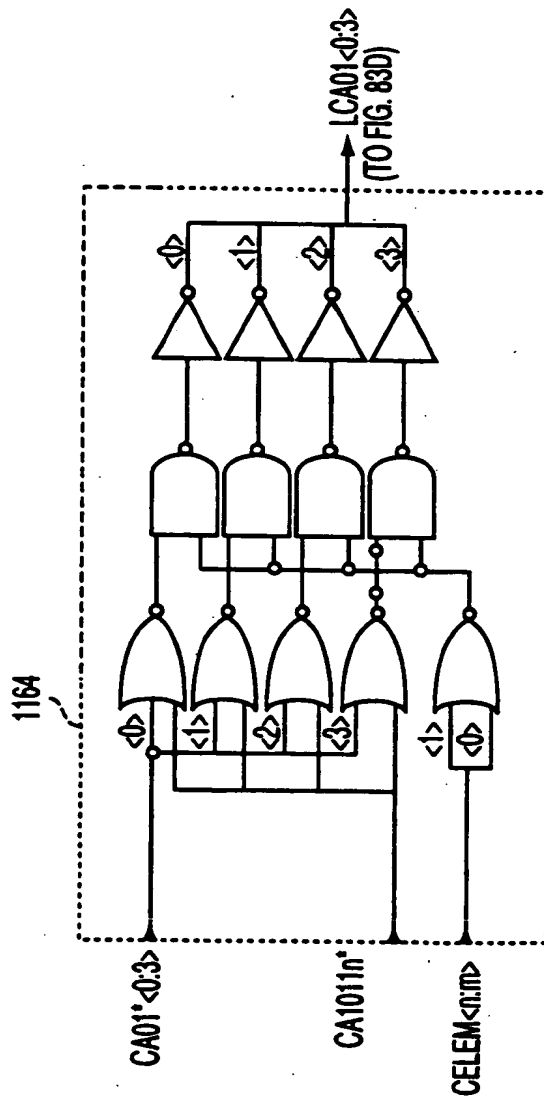
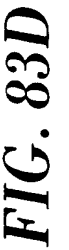


FIG. 83C



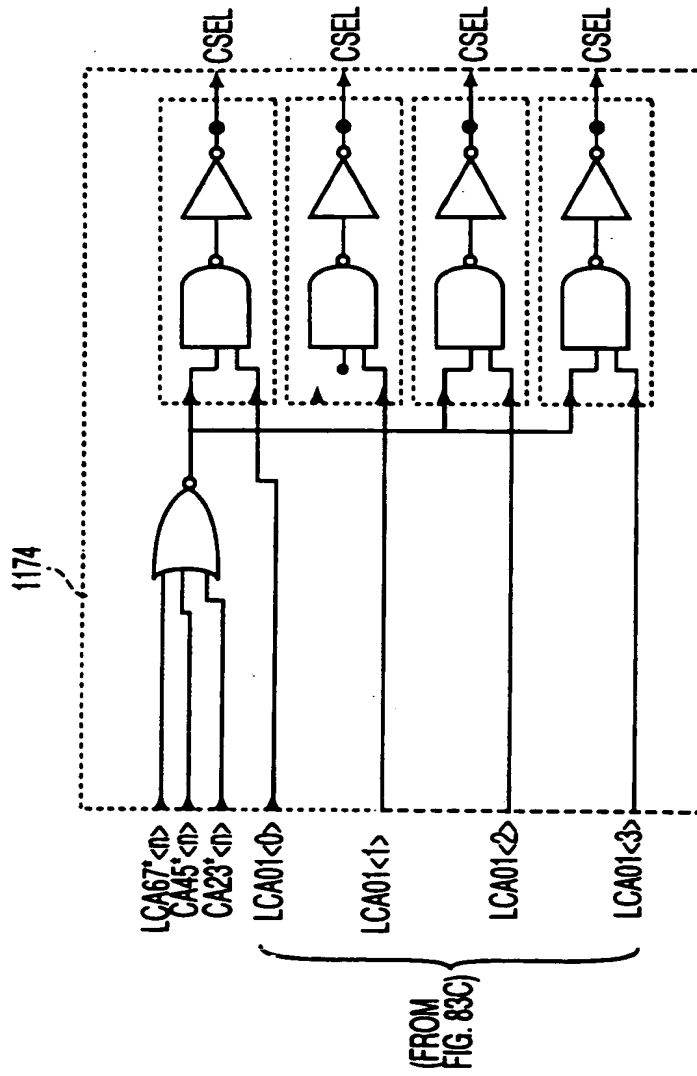


FIG. 84A

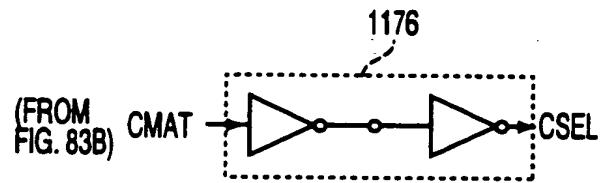


FIG. 84B

09474660 5624E660

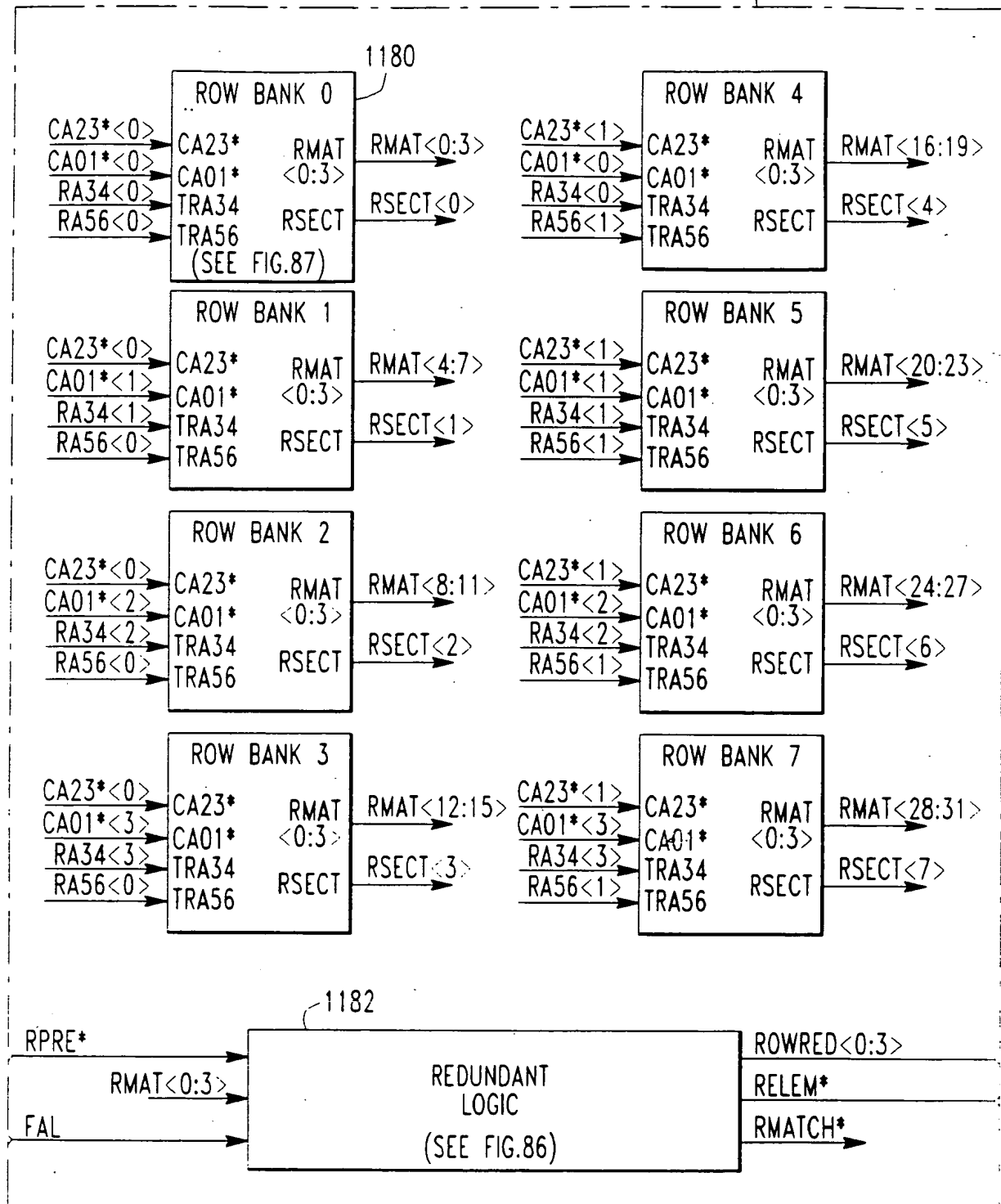


FIG. 85

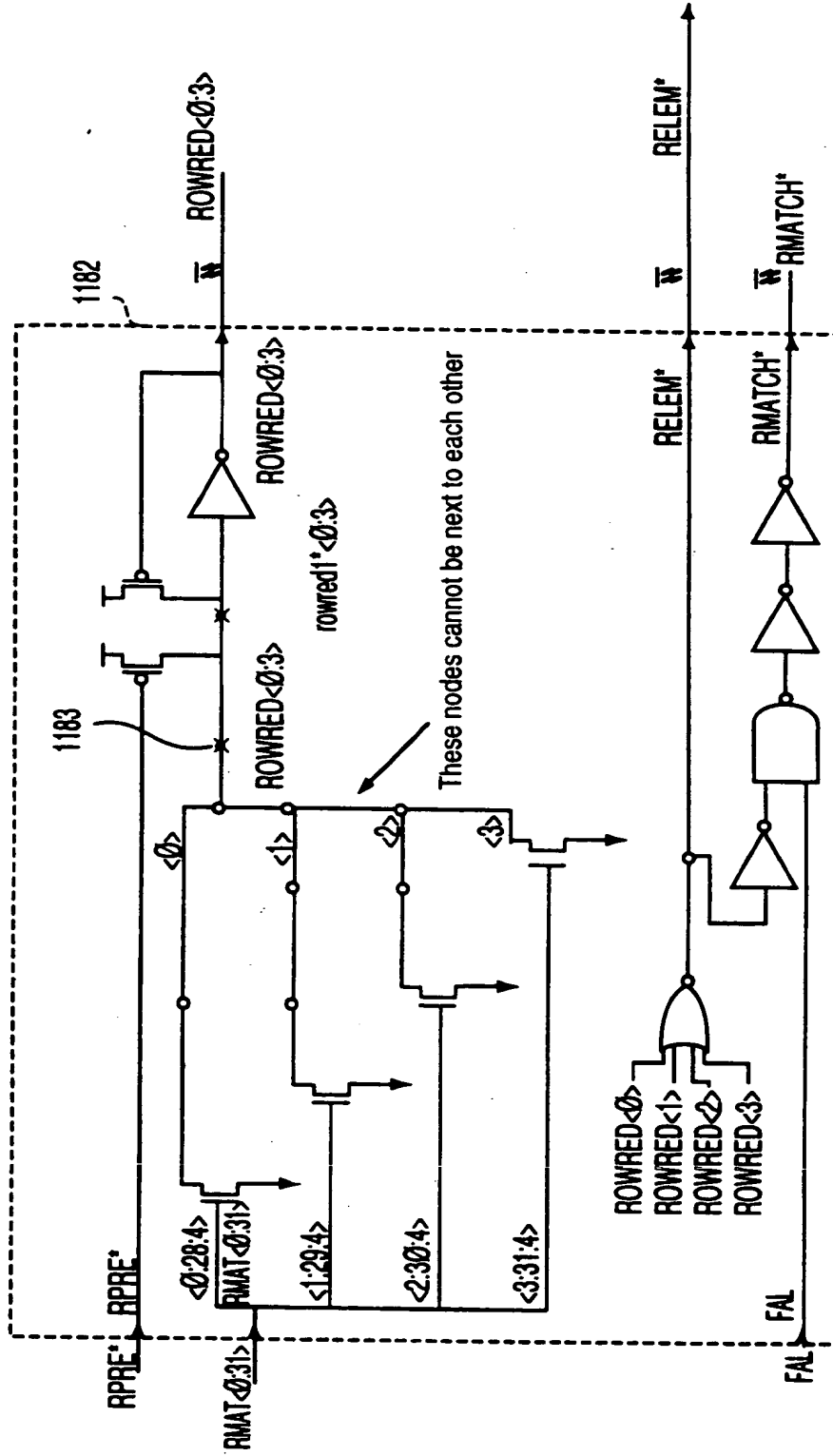


FIG. 86

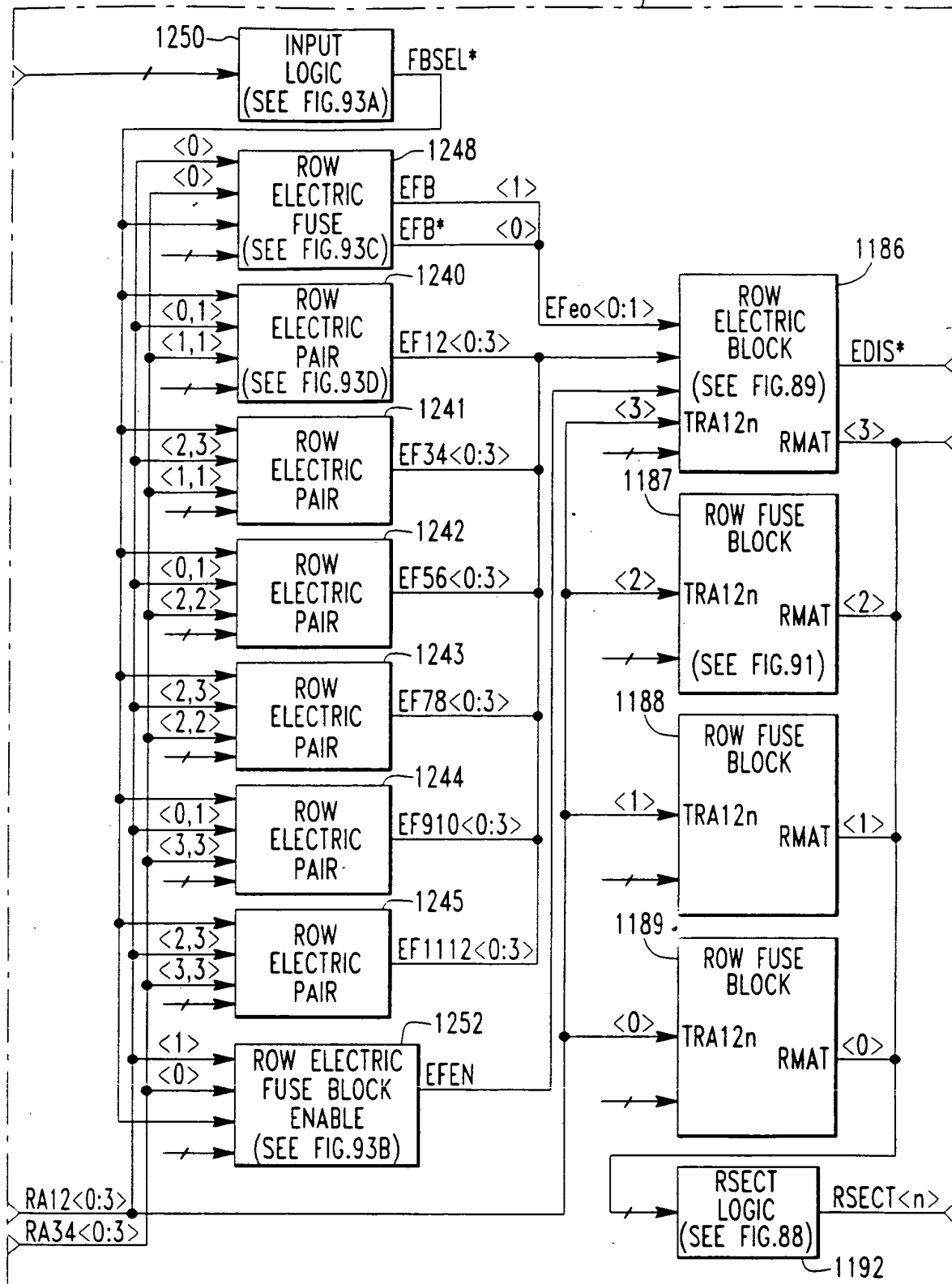
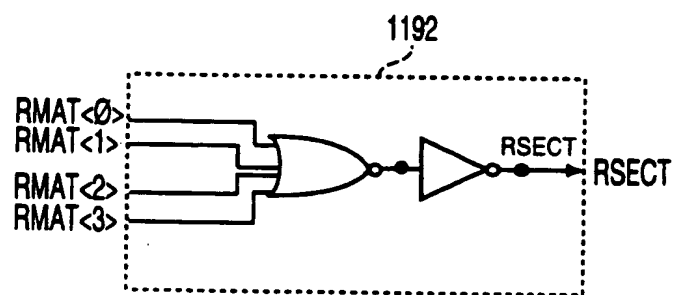


FIG. 87

**FIG. 88**

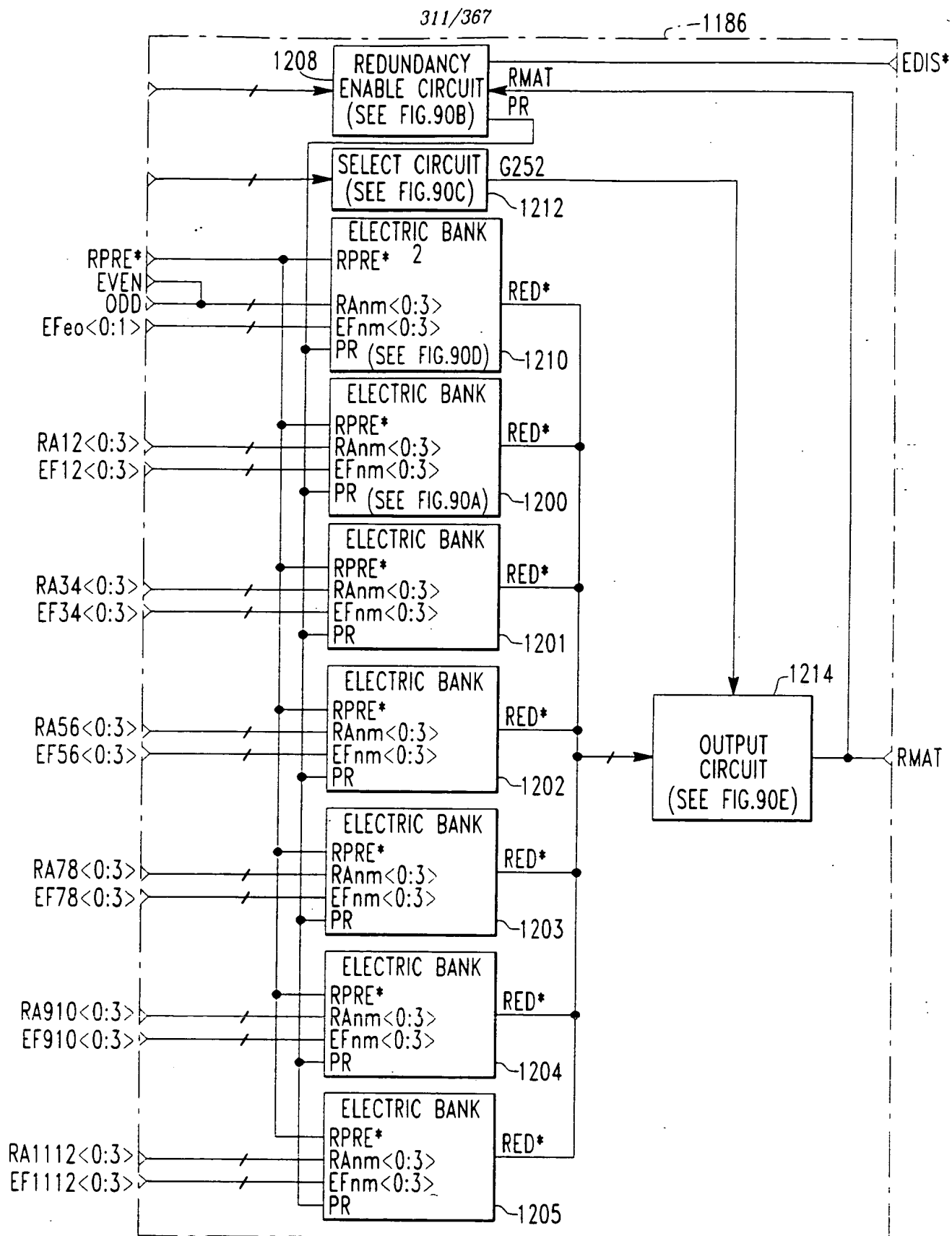


FIG. 89

FIG. 90A

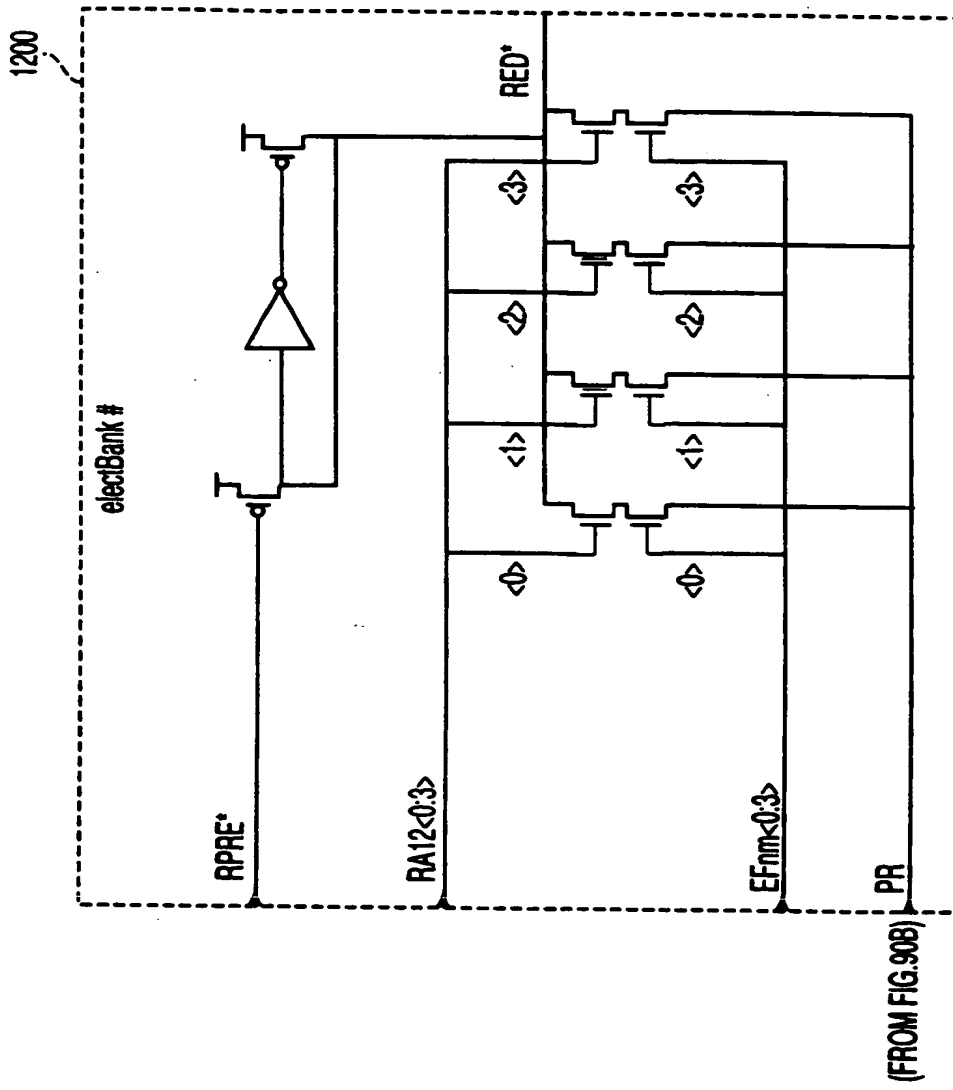


FIG. 90A

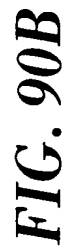


FIG. 90B

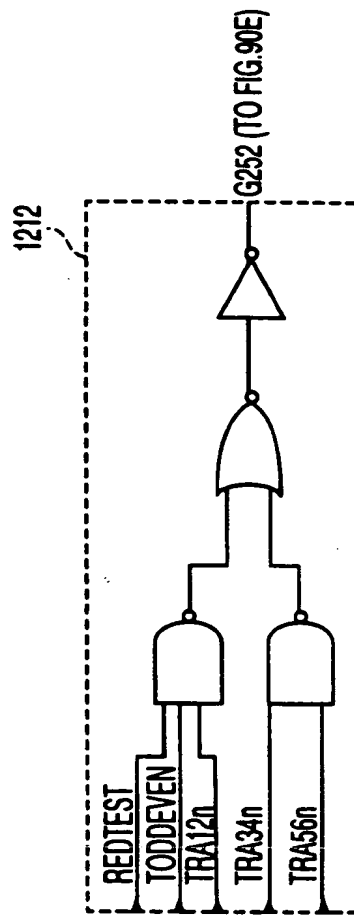


FIG. 90C

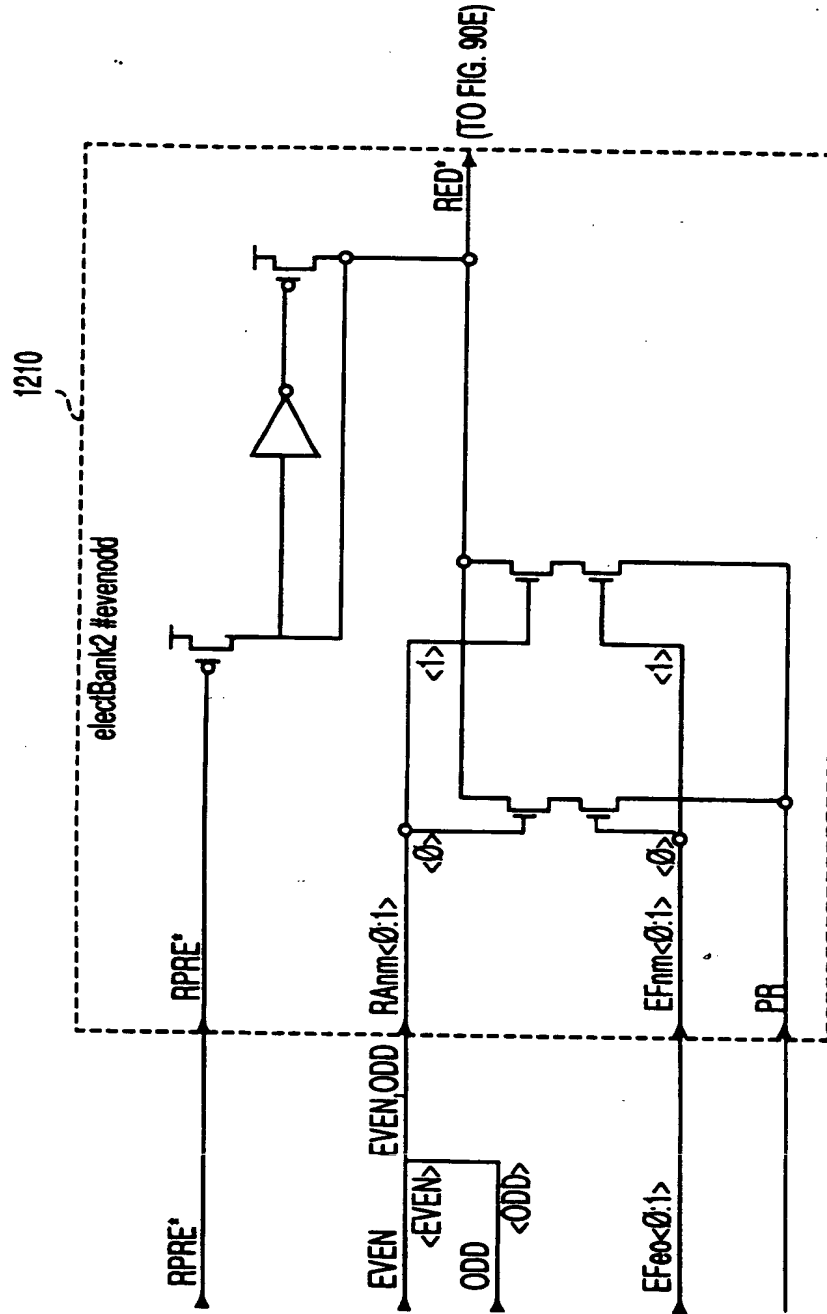


FIG. 90D

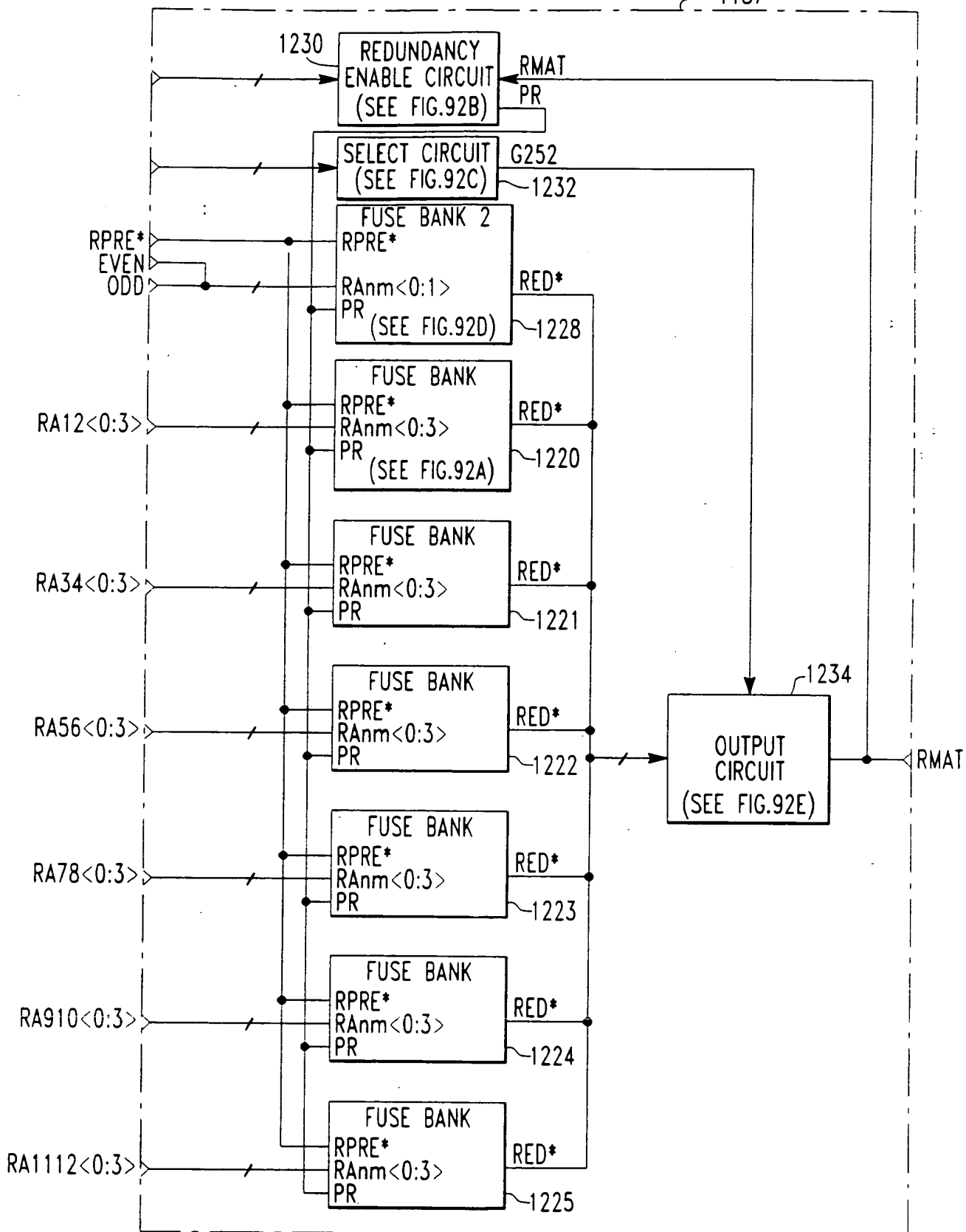


FIG. 91

FIG. 92A

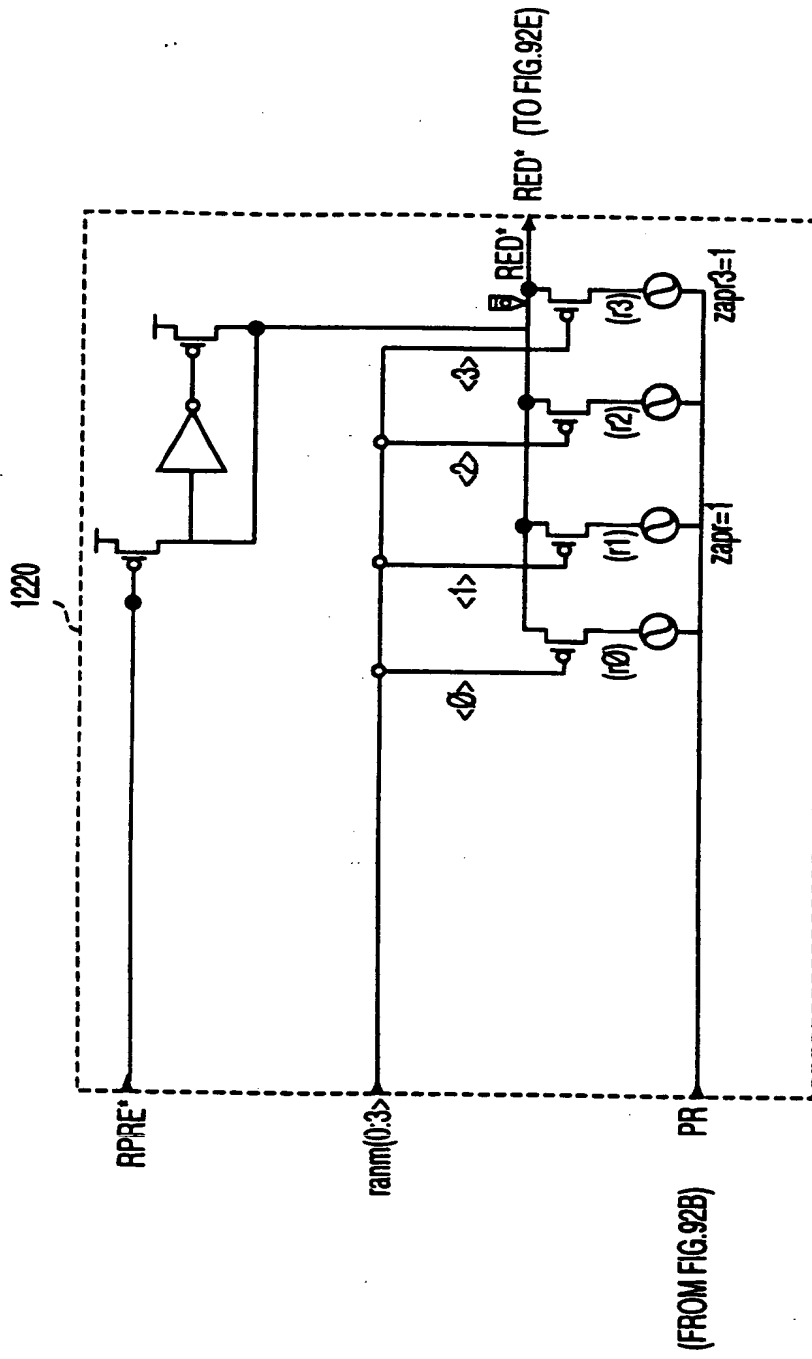


FIG. 92A

FIG. 92B

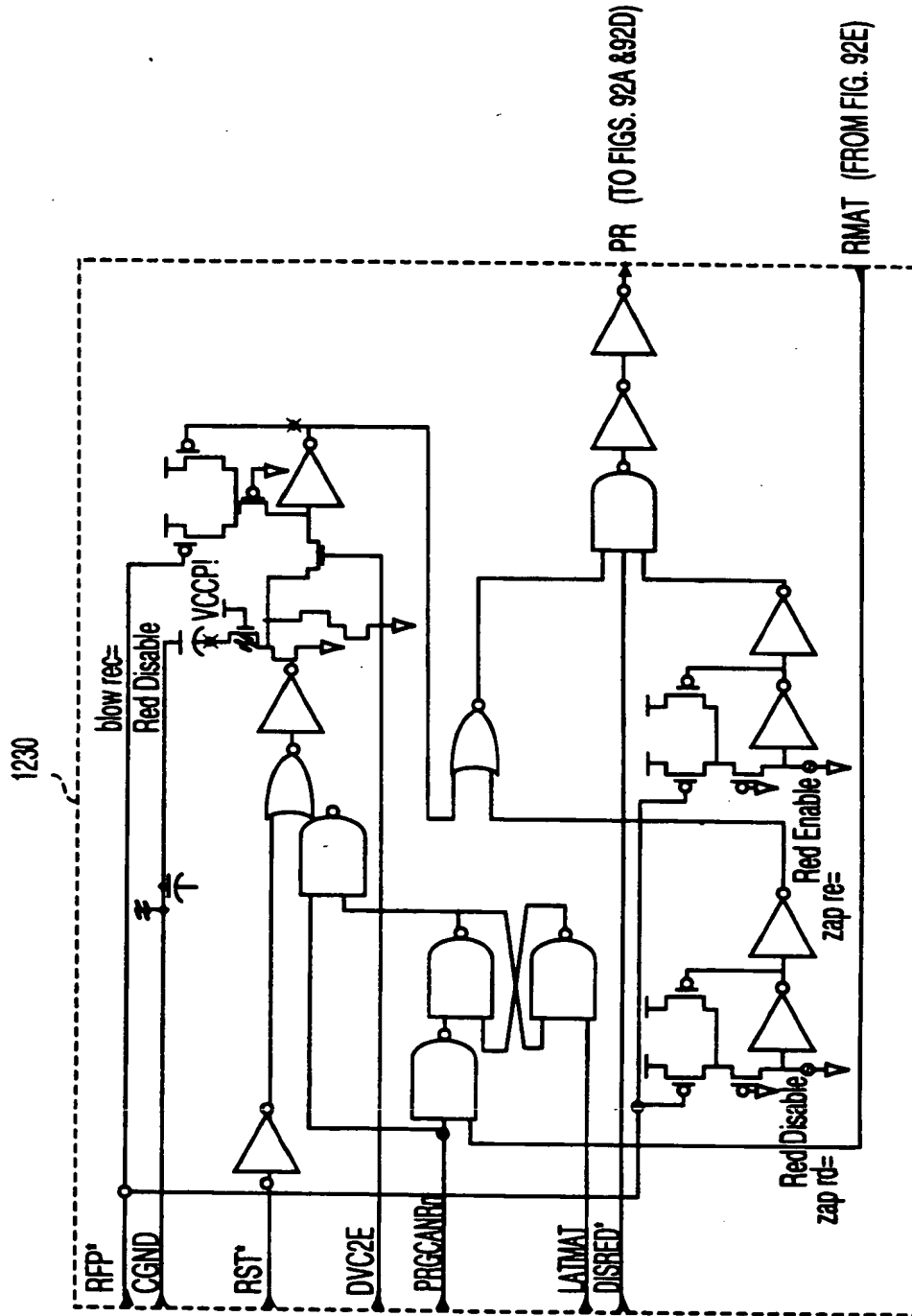


FIG. 92B

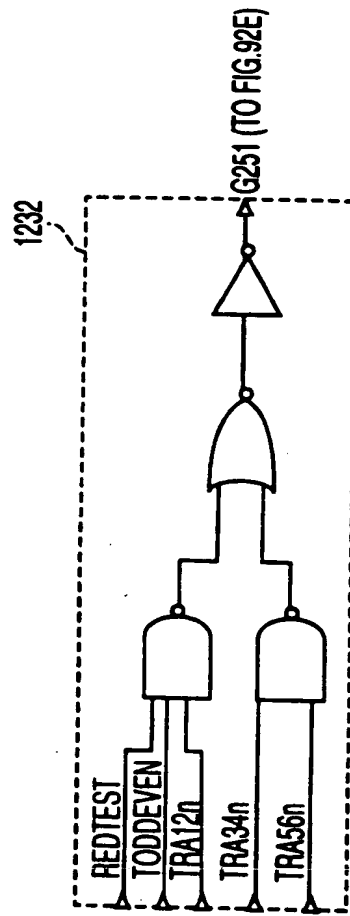


FIG. 92C

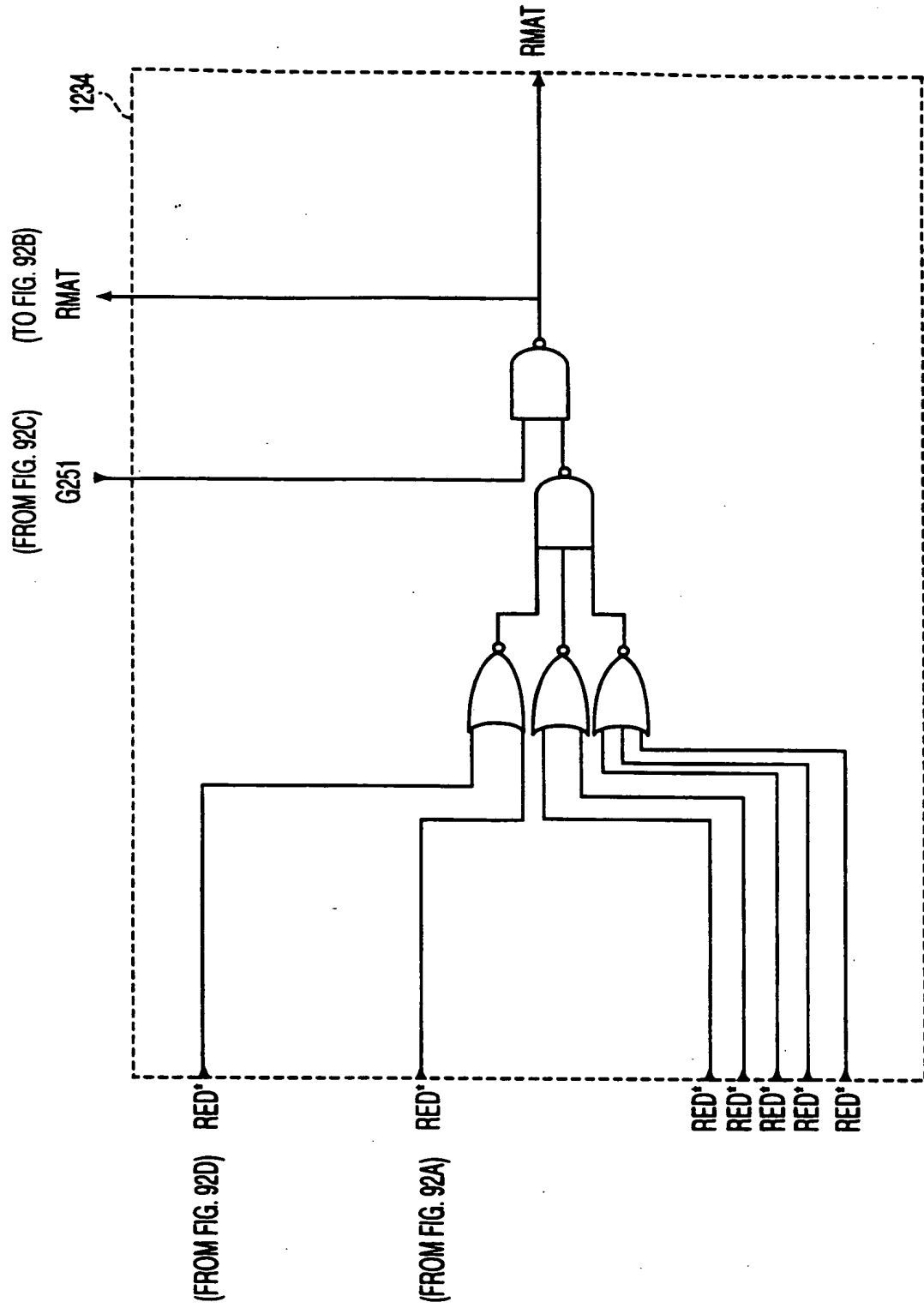
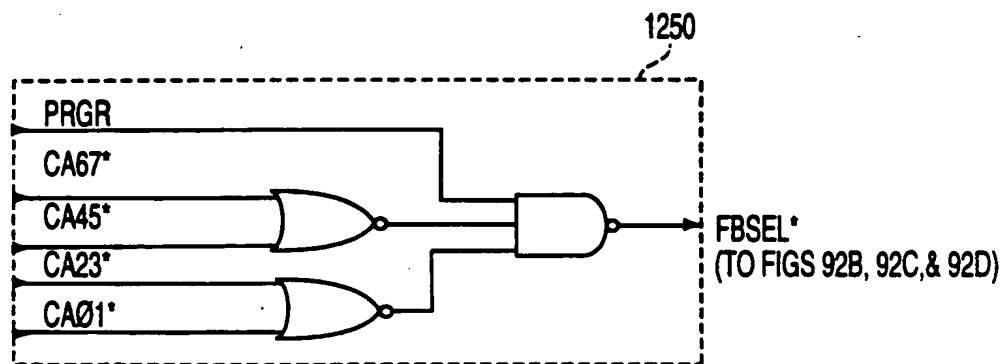
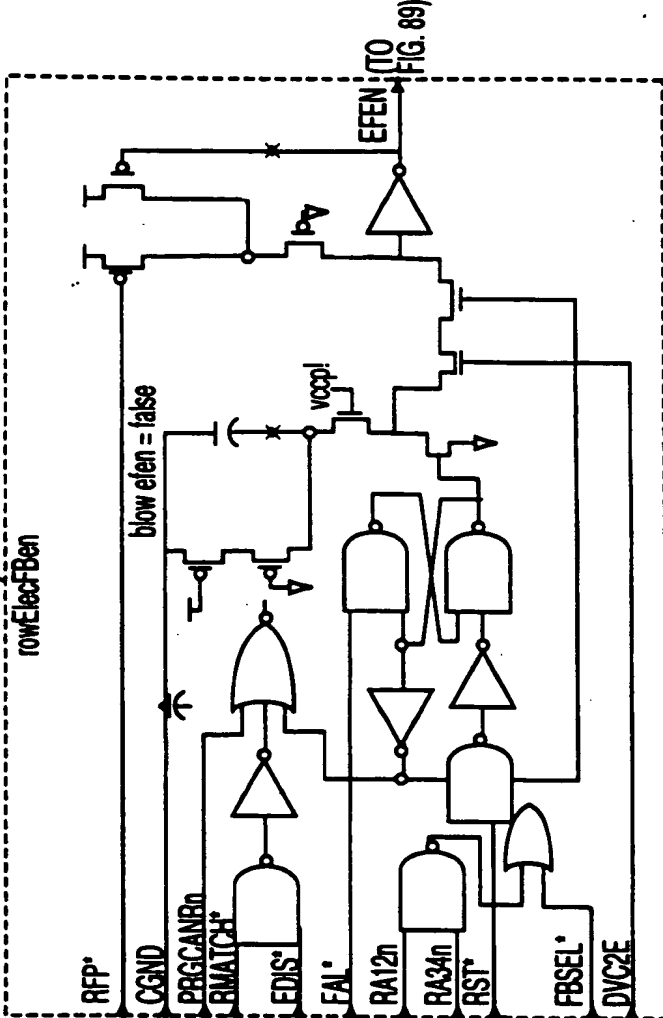


FIG. 92E

**FIG. 93A**

1252



(FROM
FIG. 93A)

RA12<0:3>
RA34<0:3>

FIG. 93B

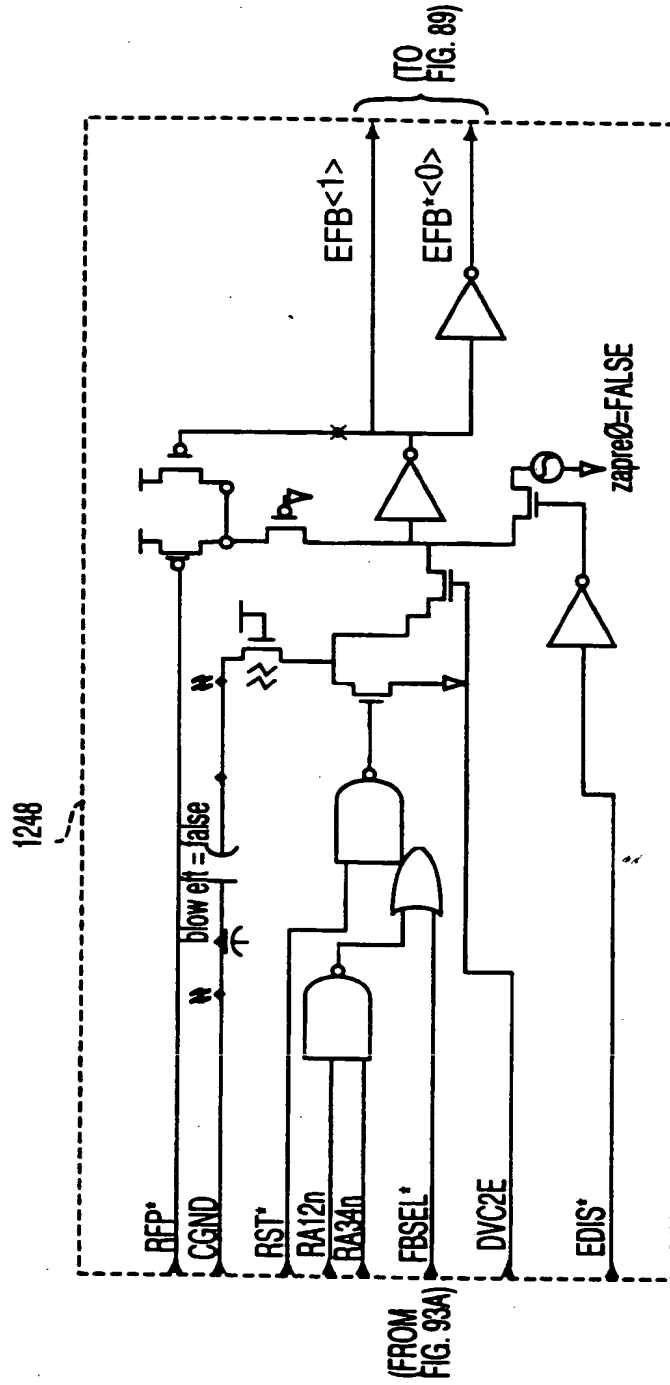


FIG. 93C

1240

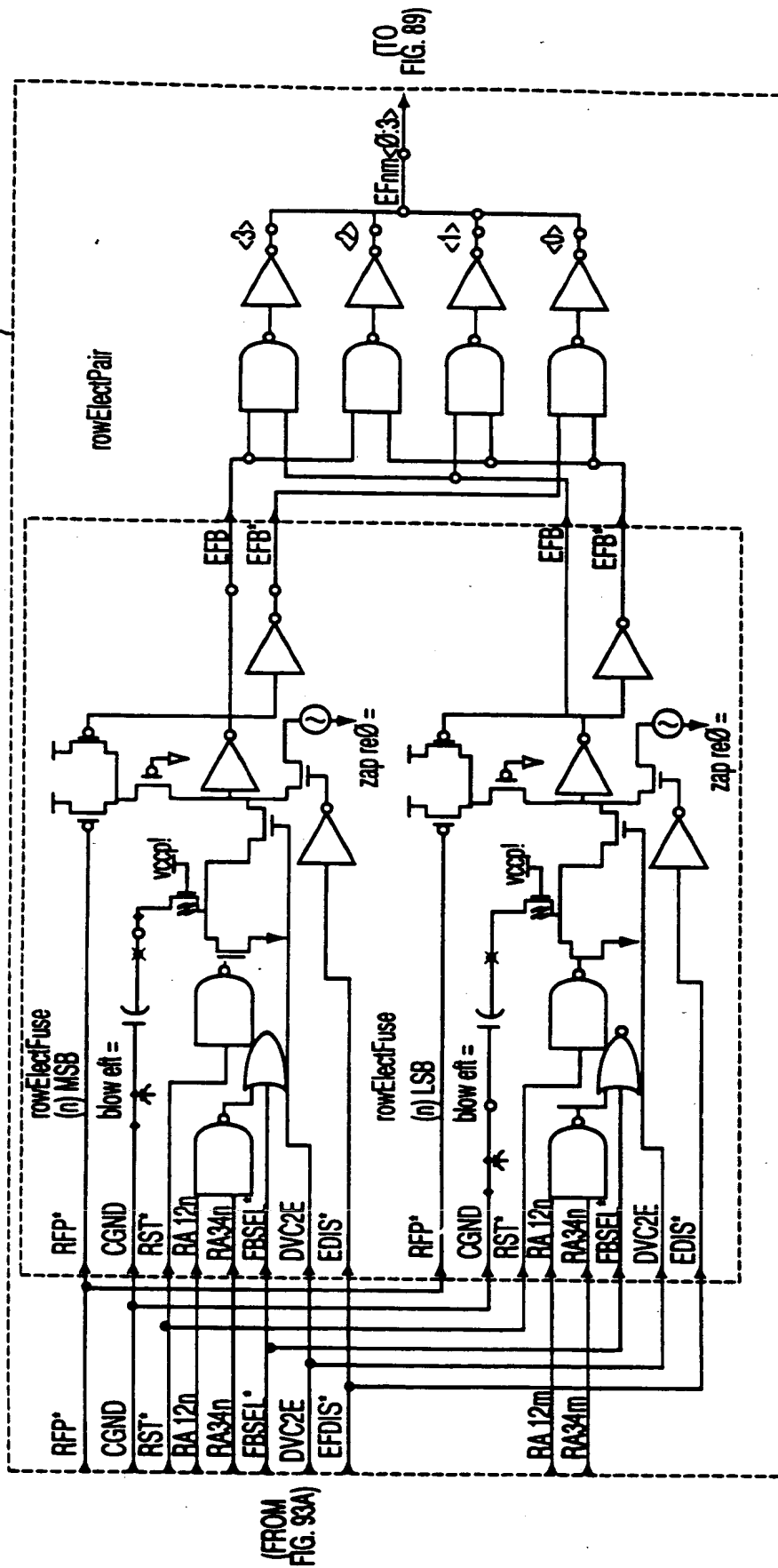
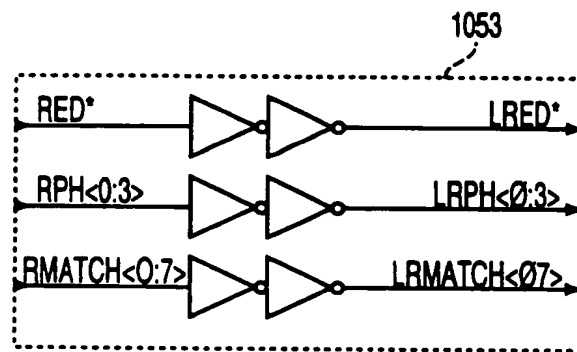


FIG. 93D

**FIG. 94**

1059

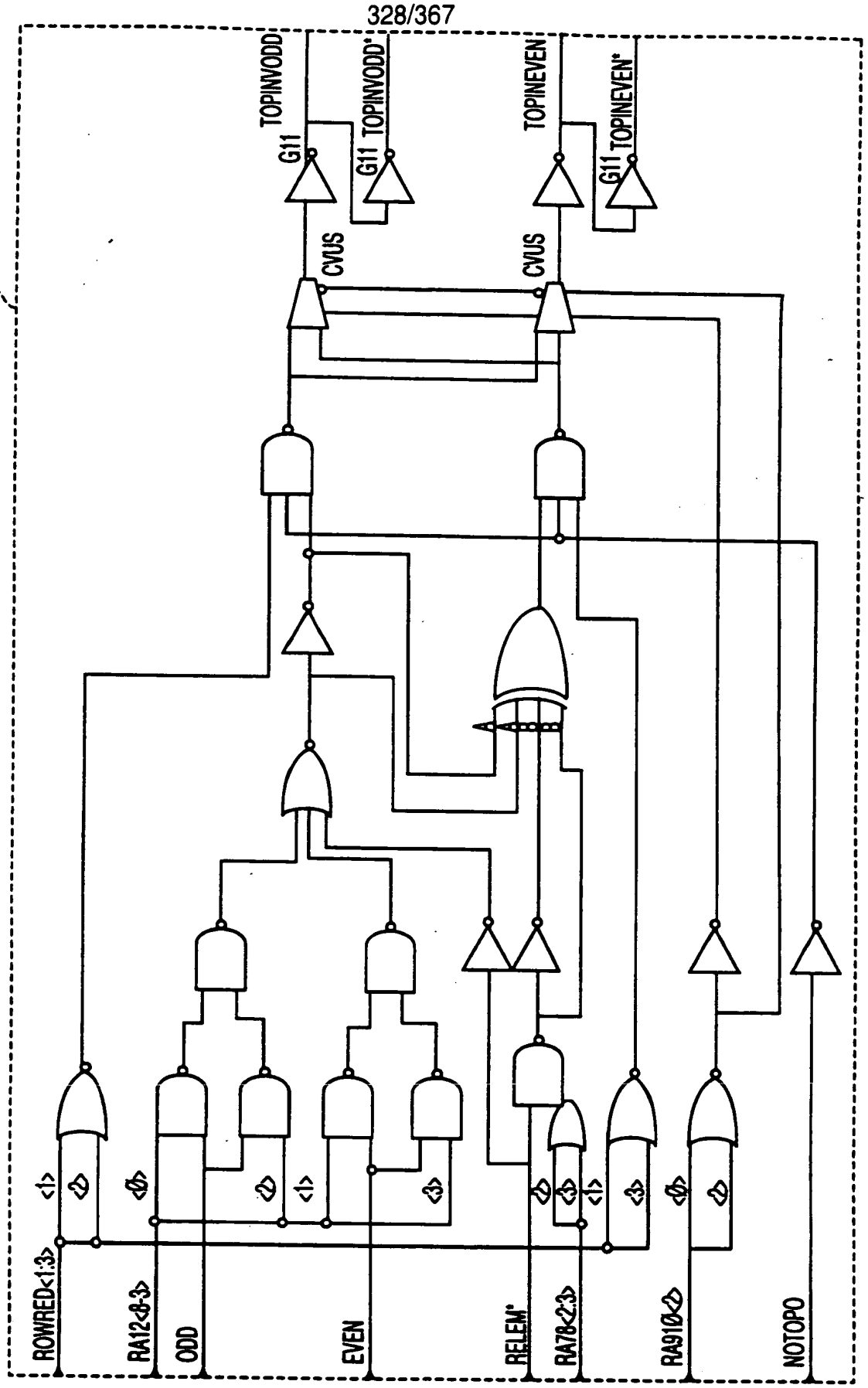


FIG. 95

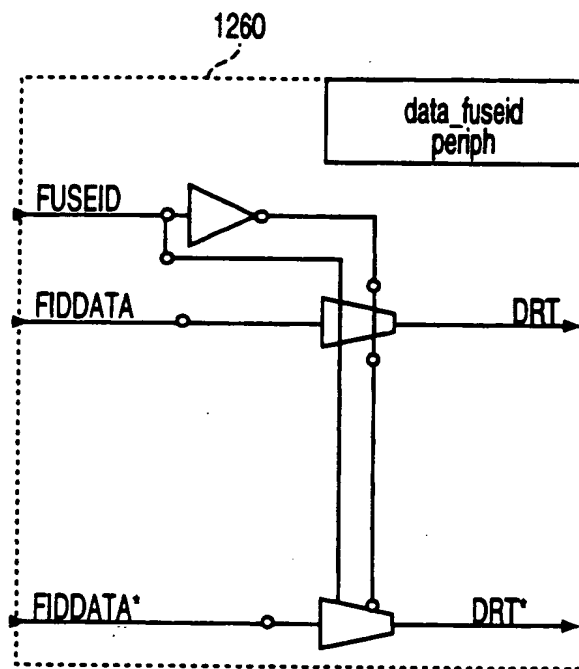
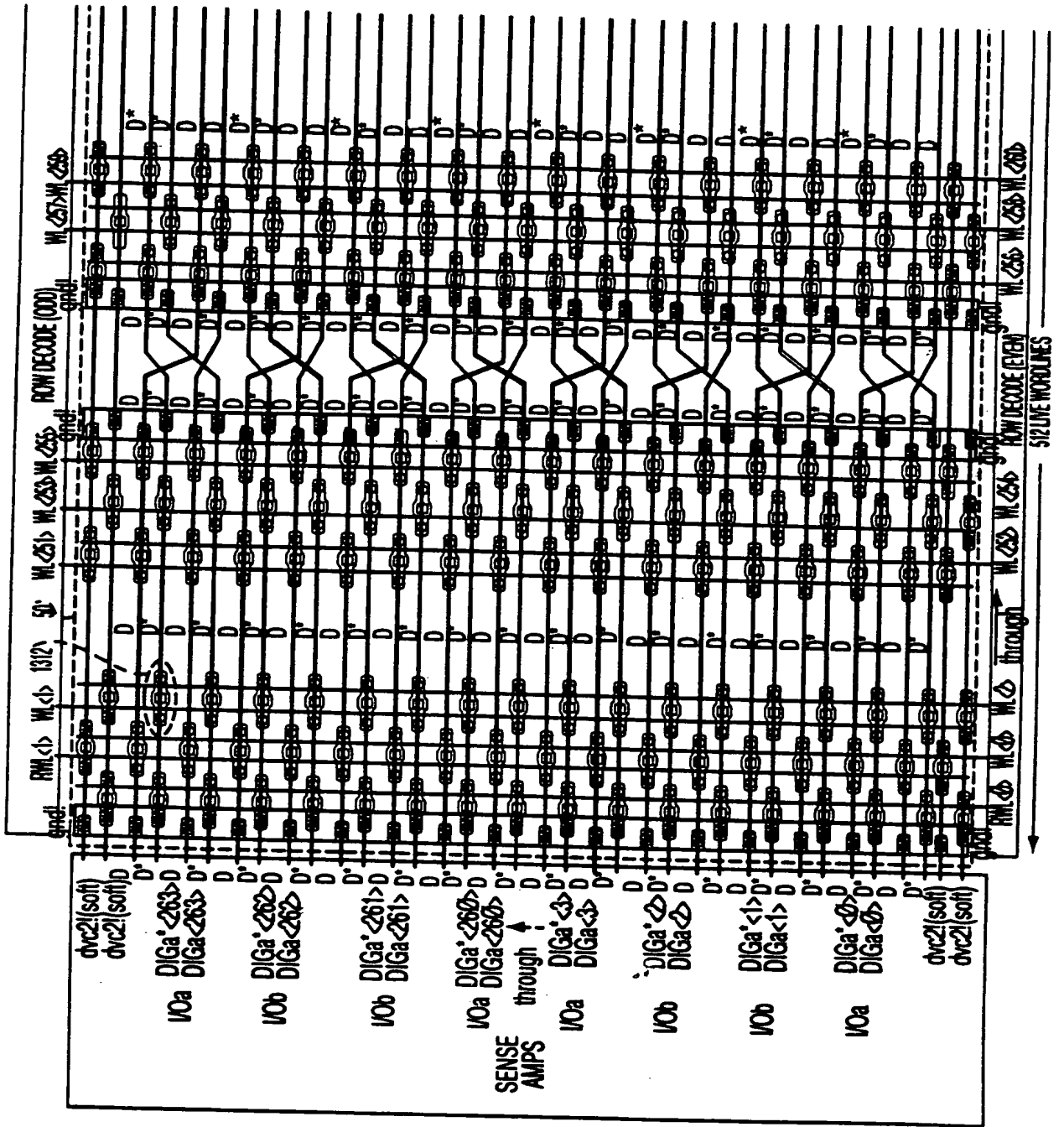
**FIG. 96**

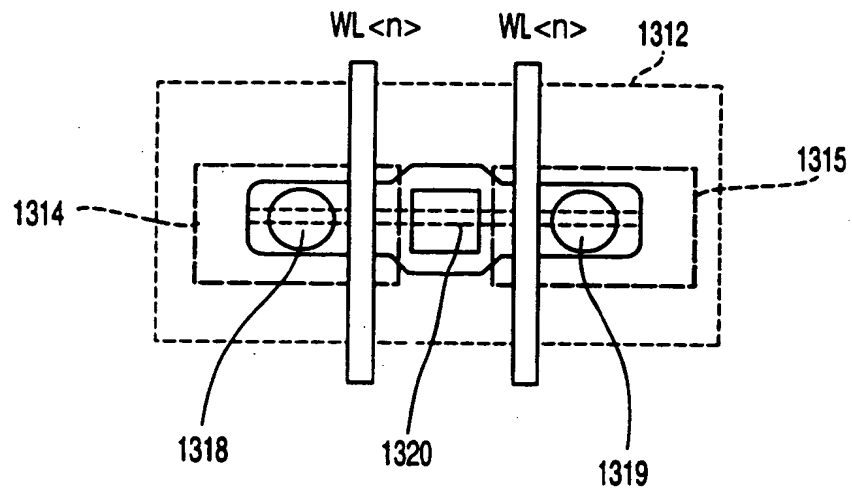
FIG. 97-1



512 NORMAL DIGIT PAIRS
32 REDUNDANT DIGIT PAIRS

FIG. 97-1 FIG. 97-2

FIG. 97-1

**FIG. 98**

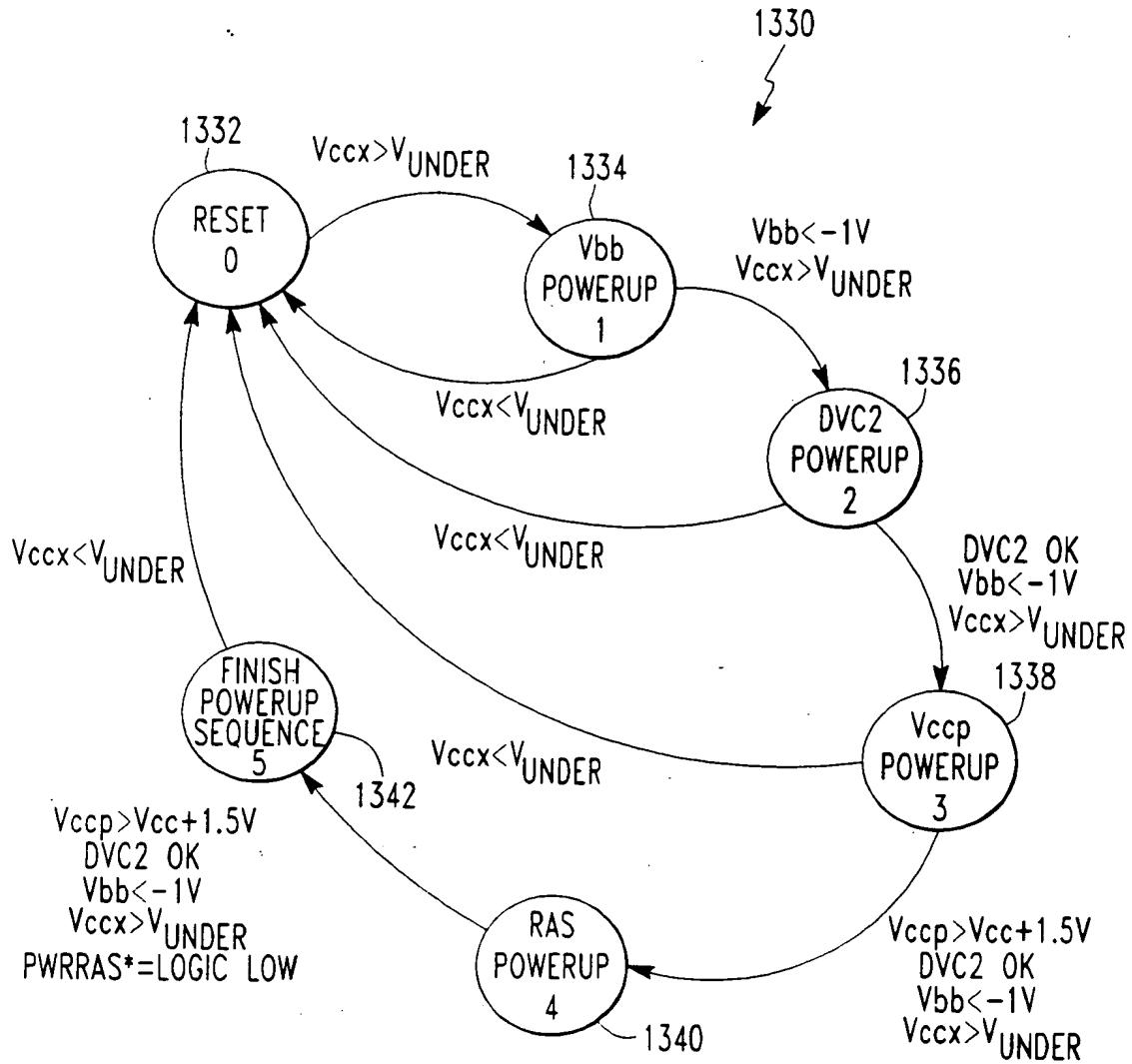


FIG. 99

1348

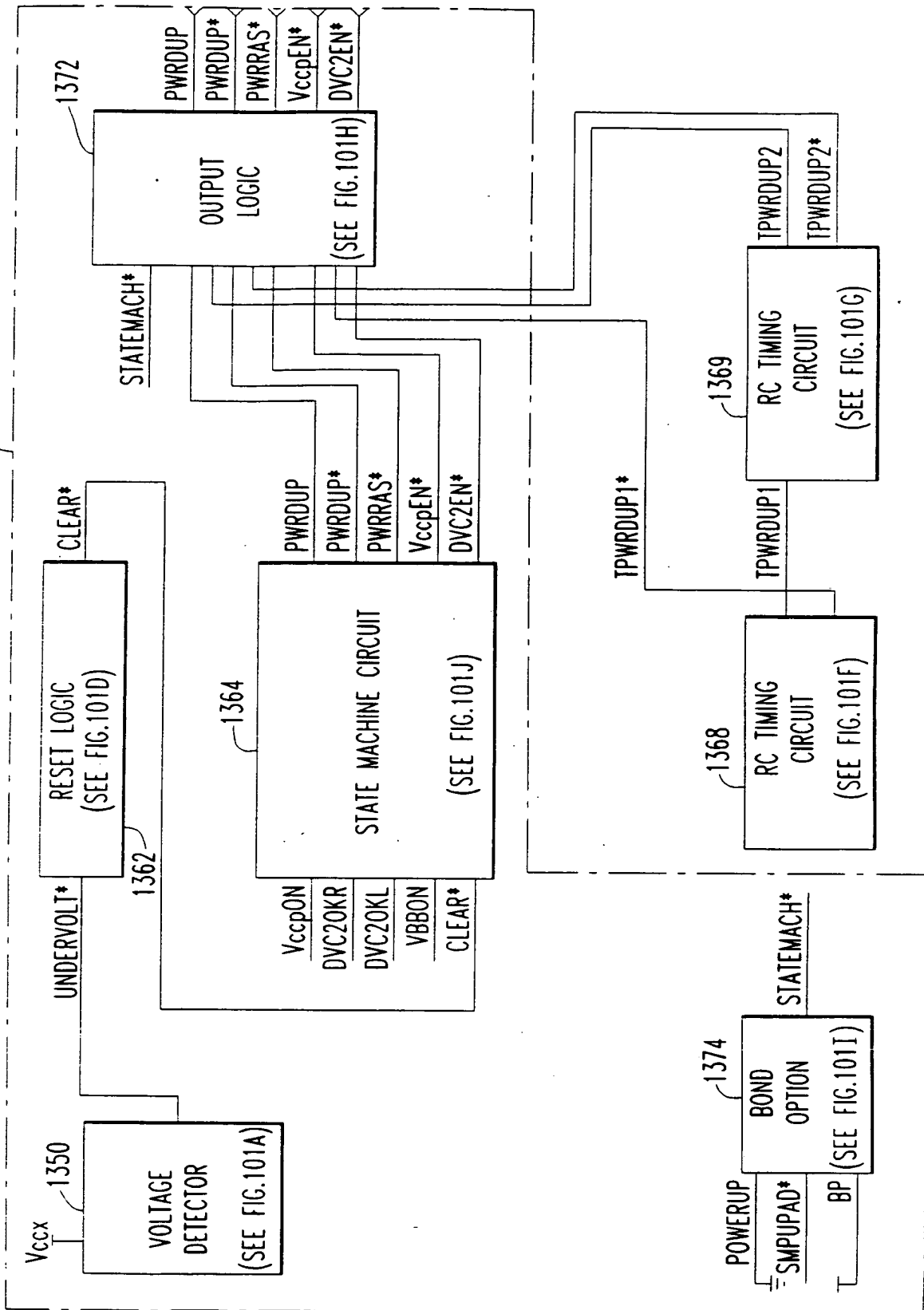


FIG. 100

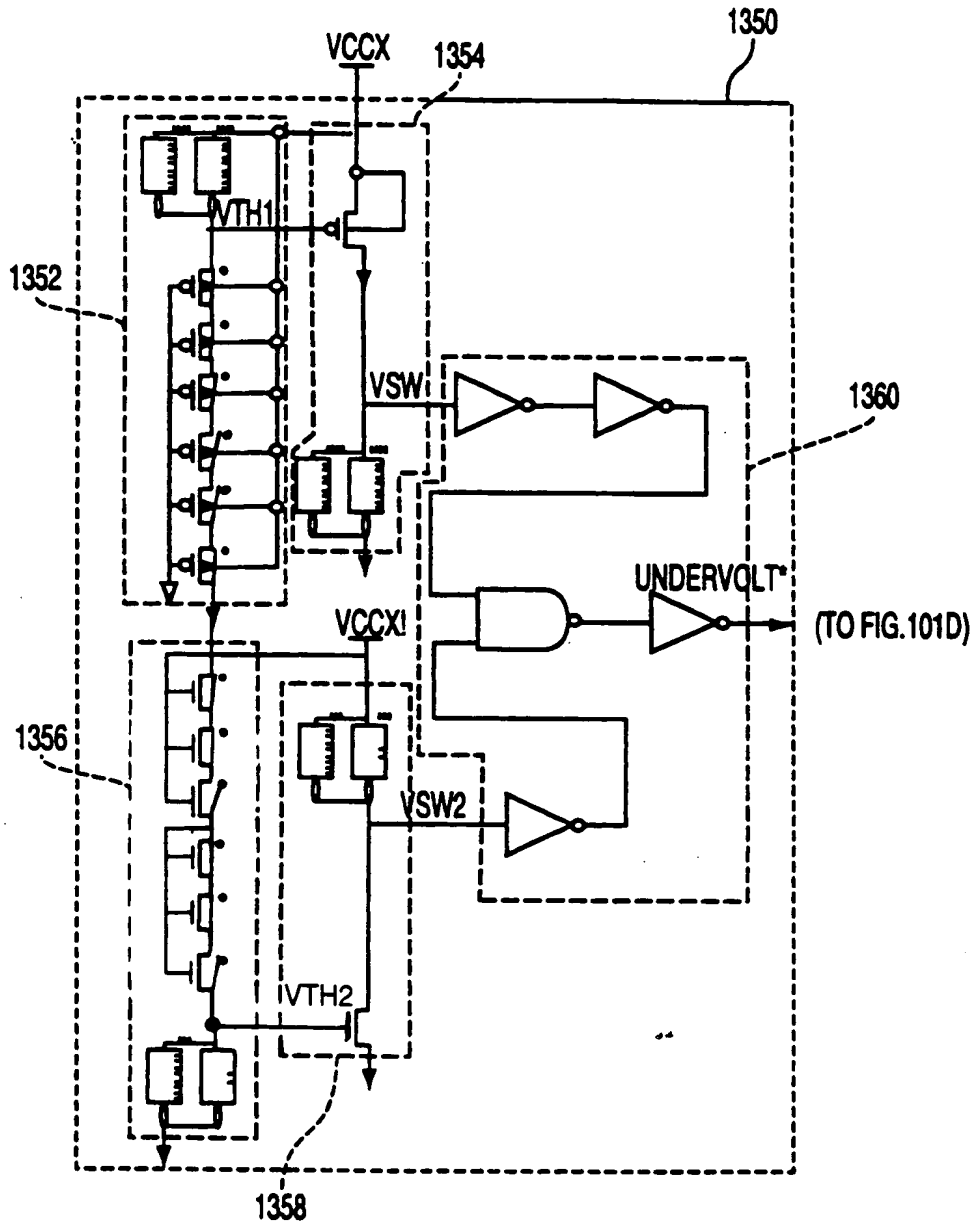
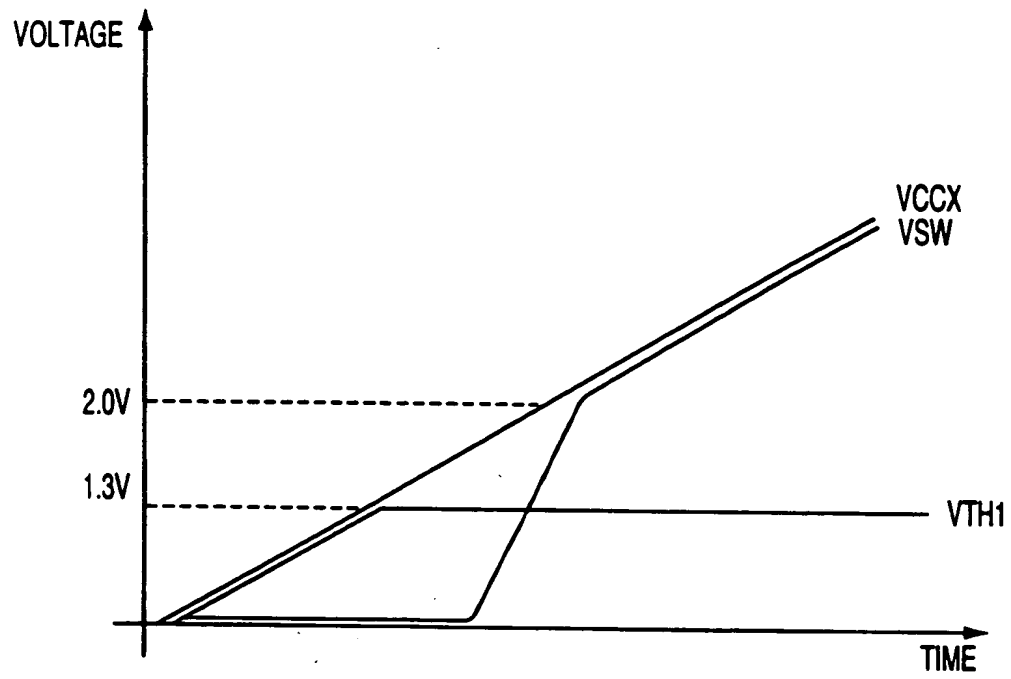
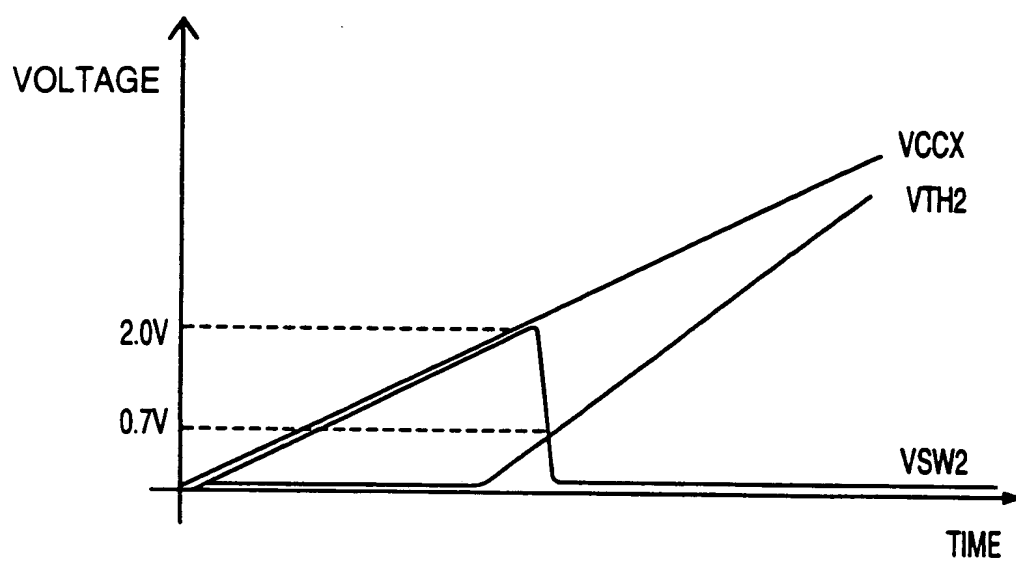


FIG. 101A

**FIG. 101B**

**FIG. 101C**

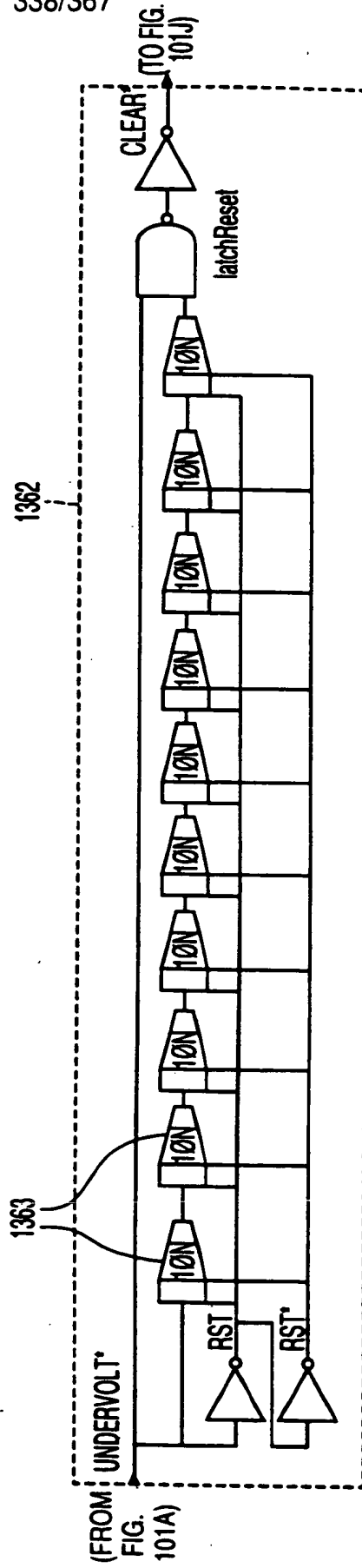


FIG. 101D

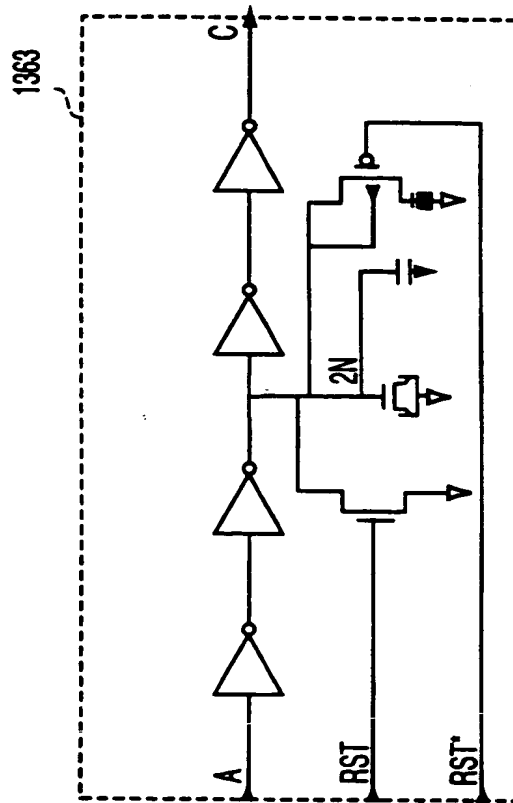


FIG. 101E

FIG. 101E

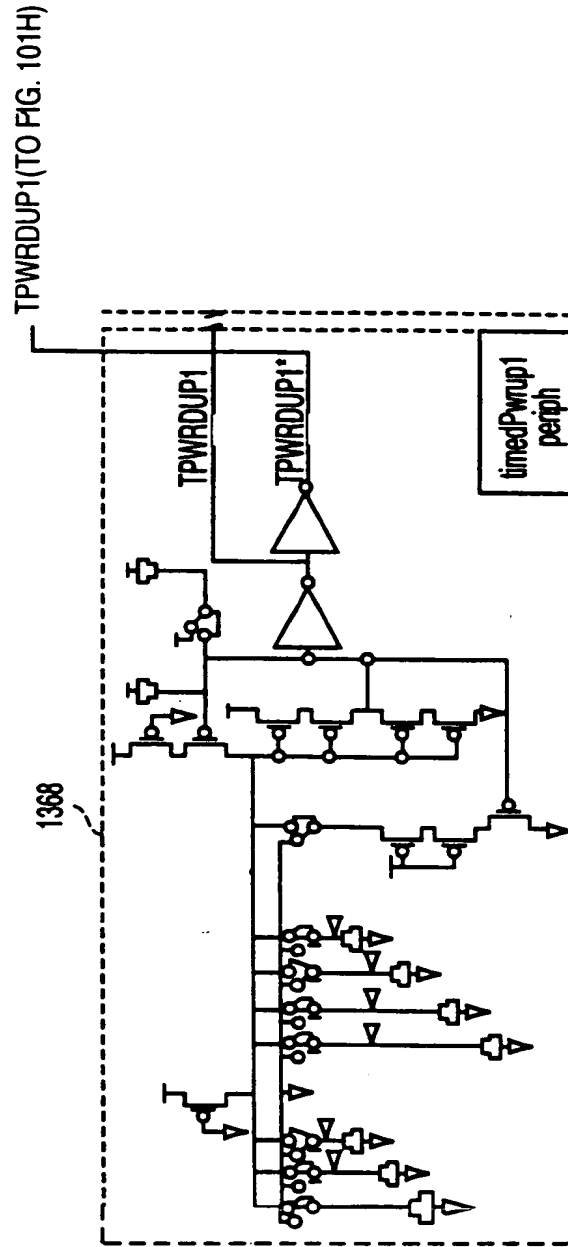


FIG. 101F

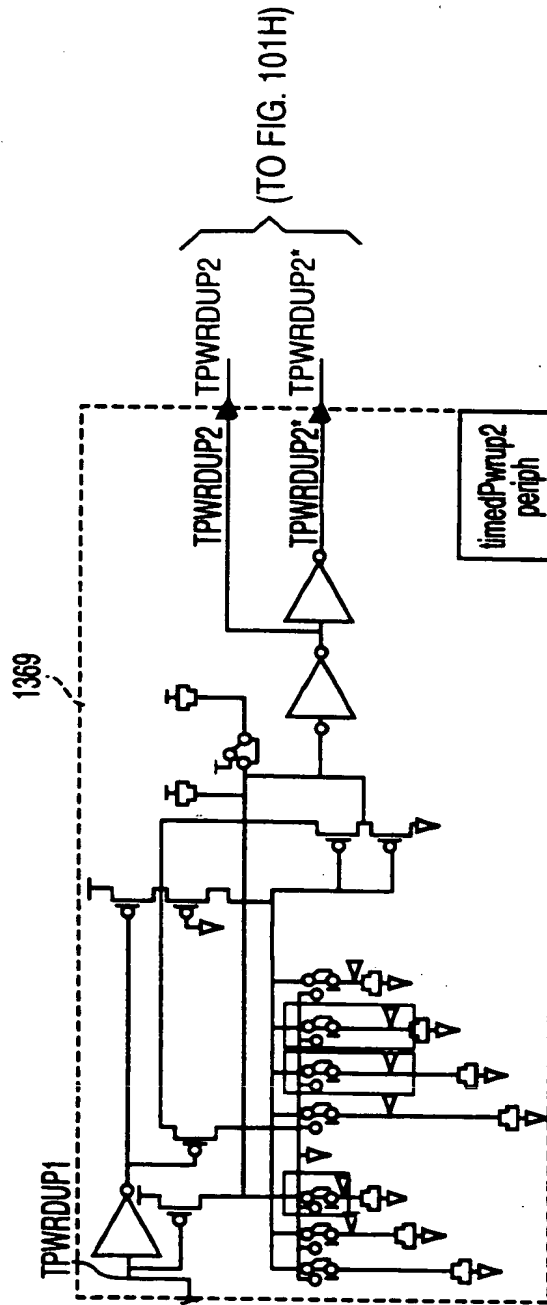
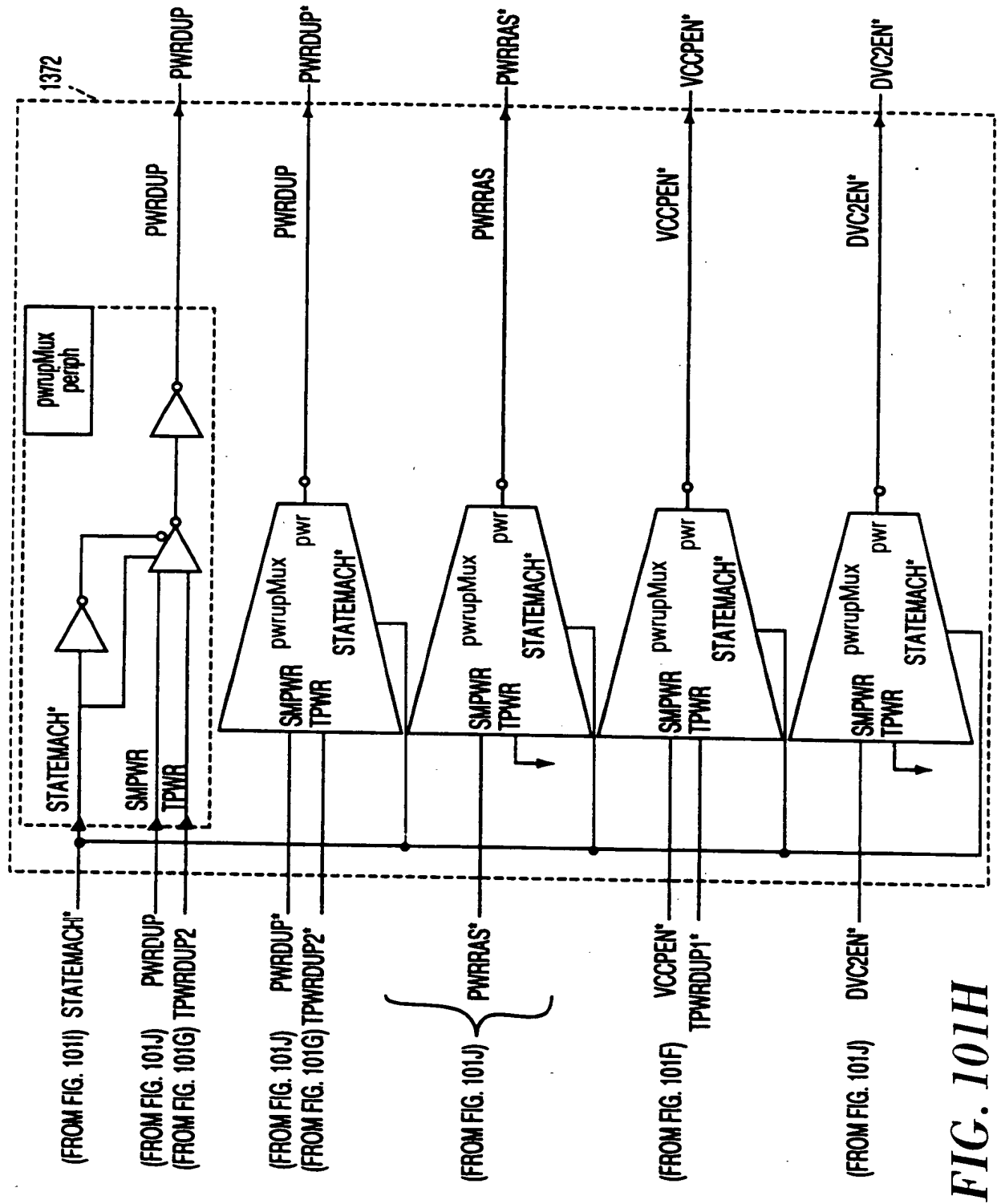


FIG. 101G



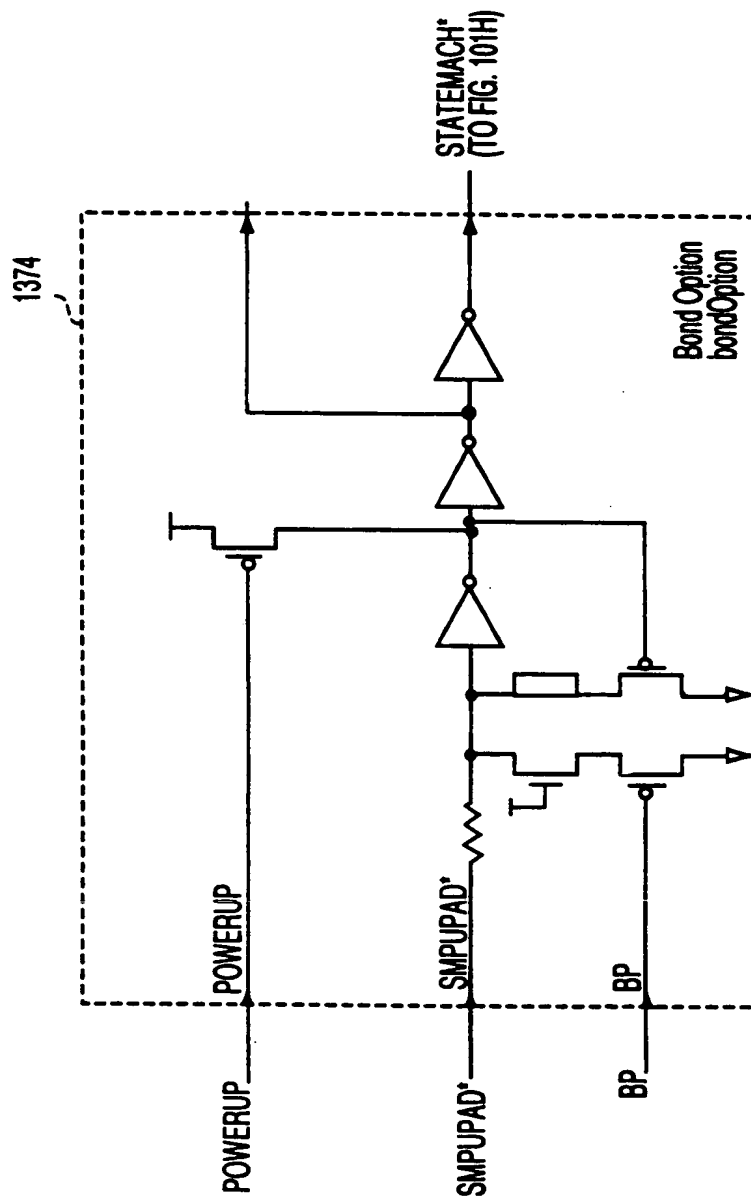


FIG. 101I

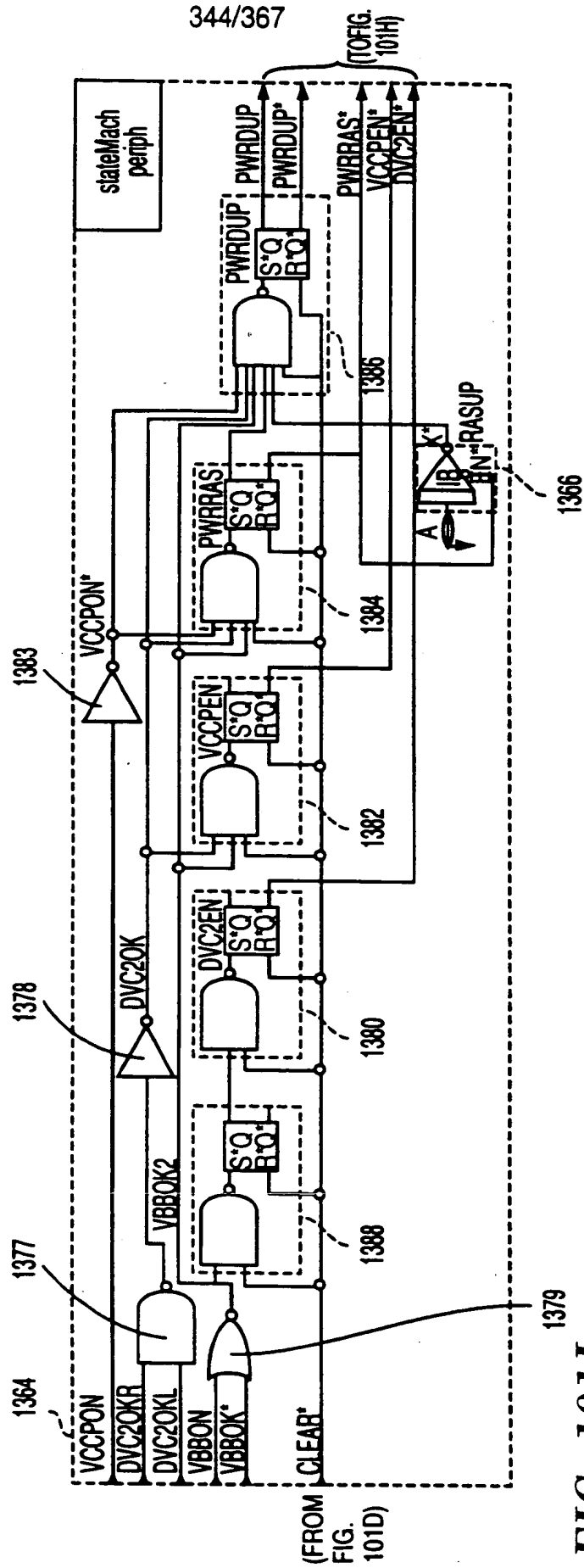
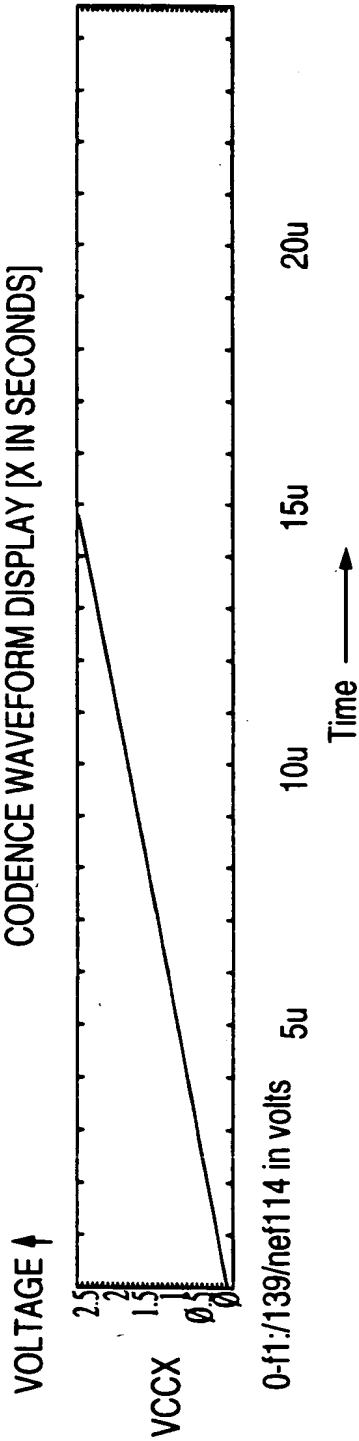
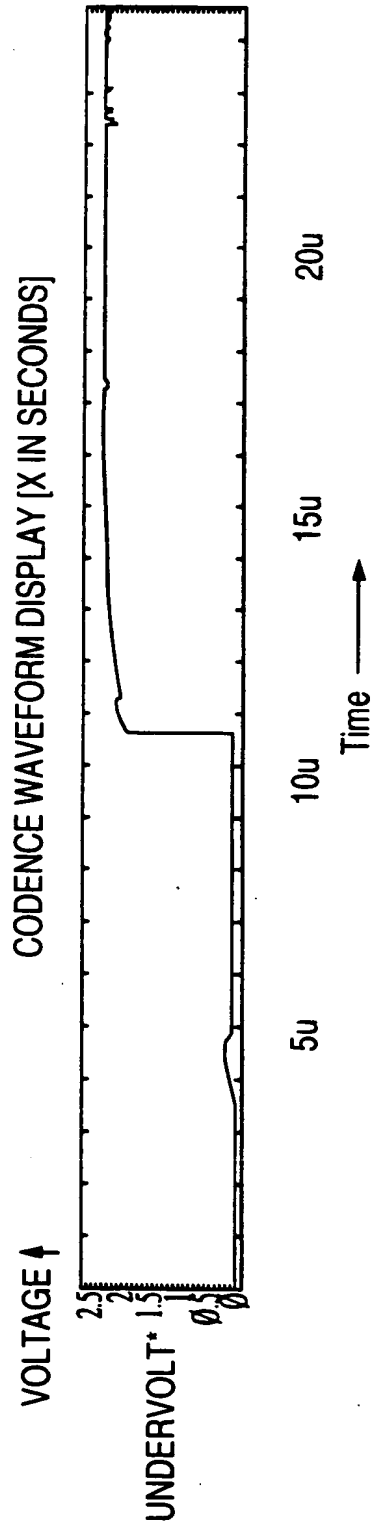


FIG. 101J



NOTE THAT PWRRAS* WAITED FOR DVC20KR

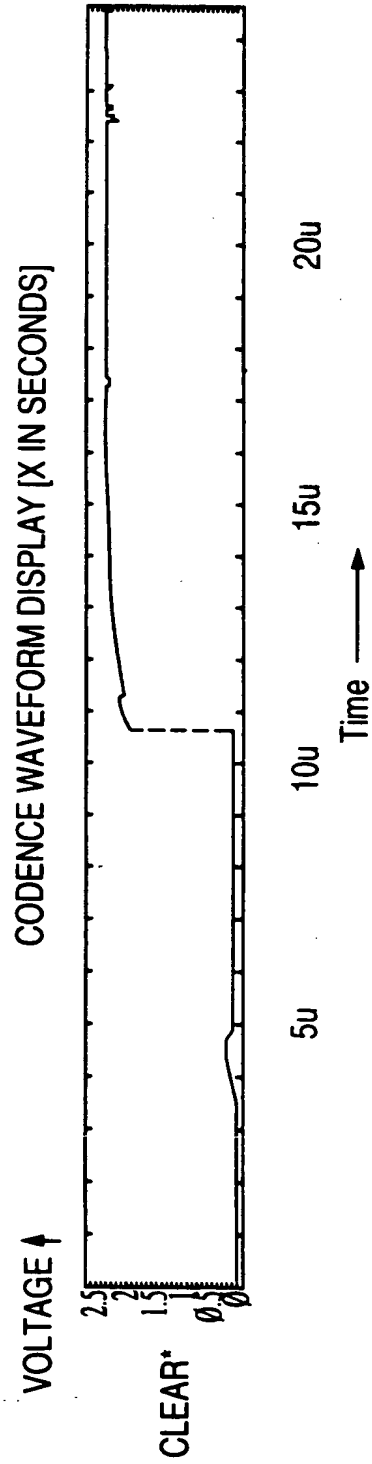
FIG. 102A



NOTE THAT PWRRAS* WAITED FOR DVC20KR

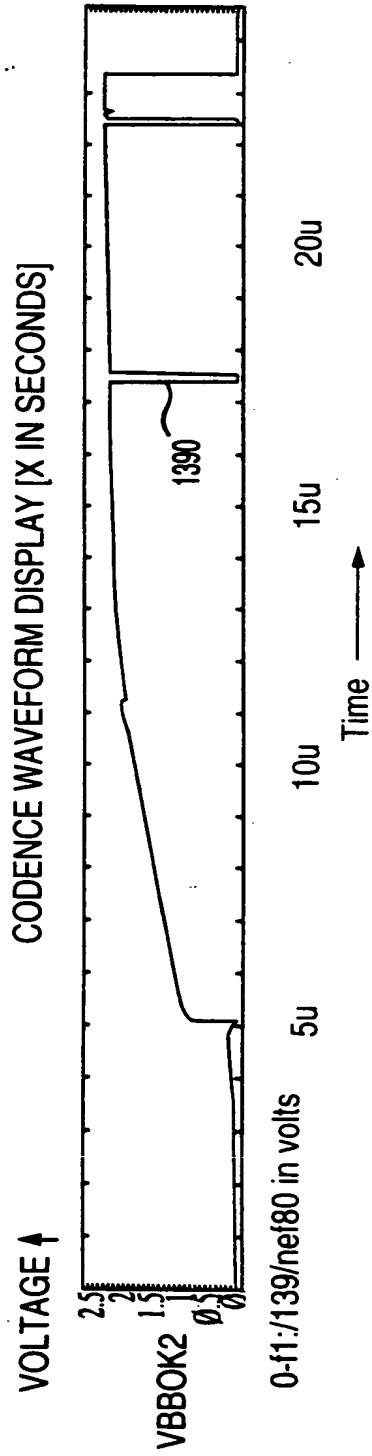
FIG. 102B

FOZZO-5624E650



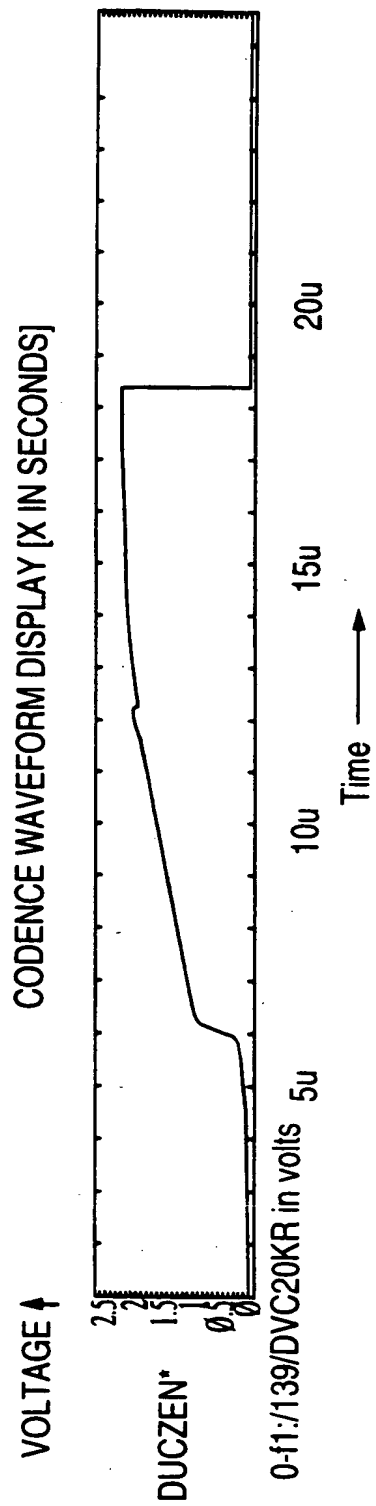
NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102C



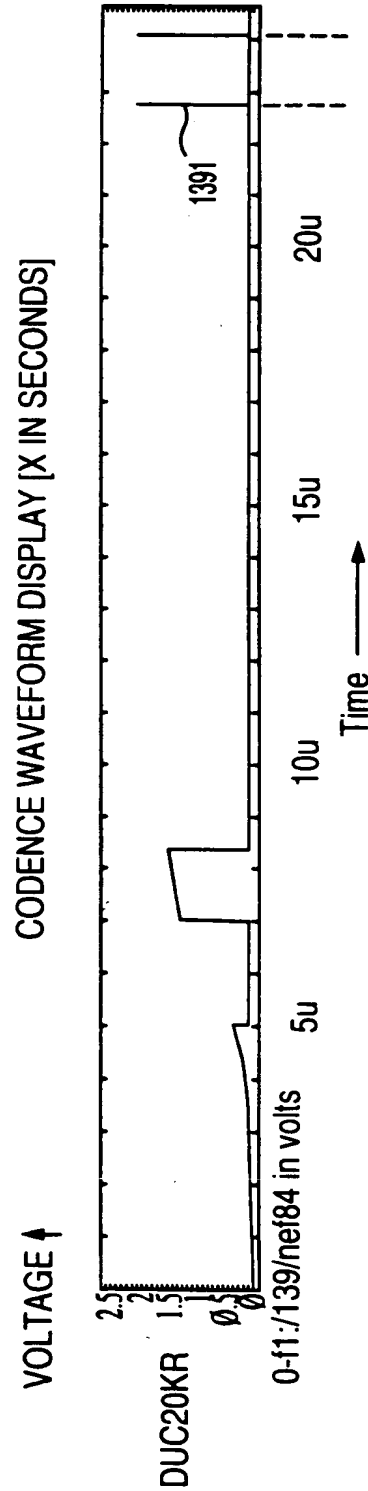
NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102D



NOTE THAT PWRRAS* WAITED FOR DVC20KR

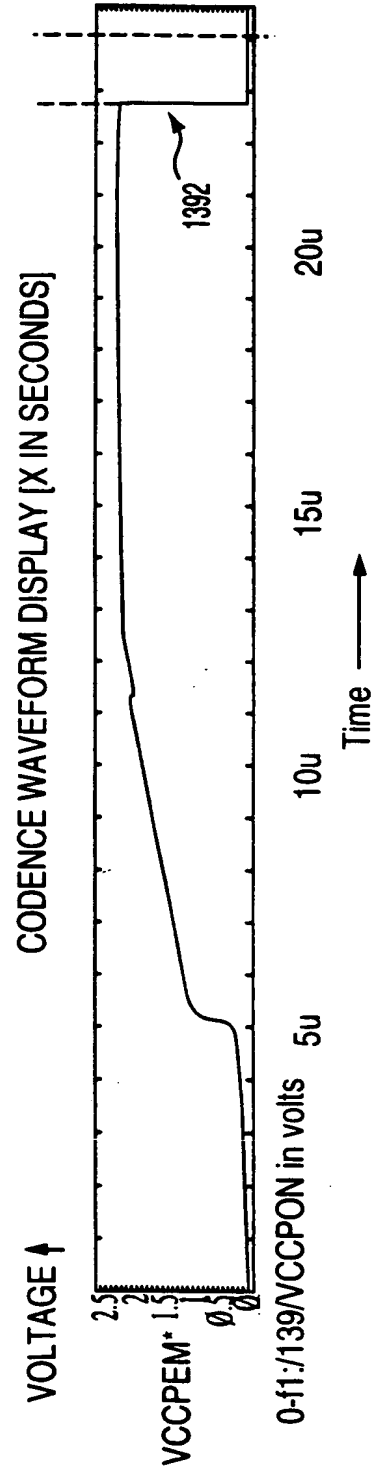
FIG. 102E



NOTE THAT PWRRAS* WAITED FOR DVC20KR

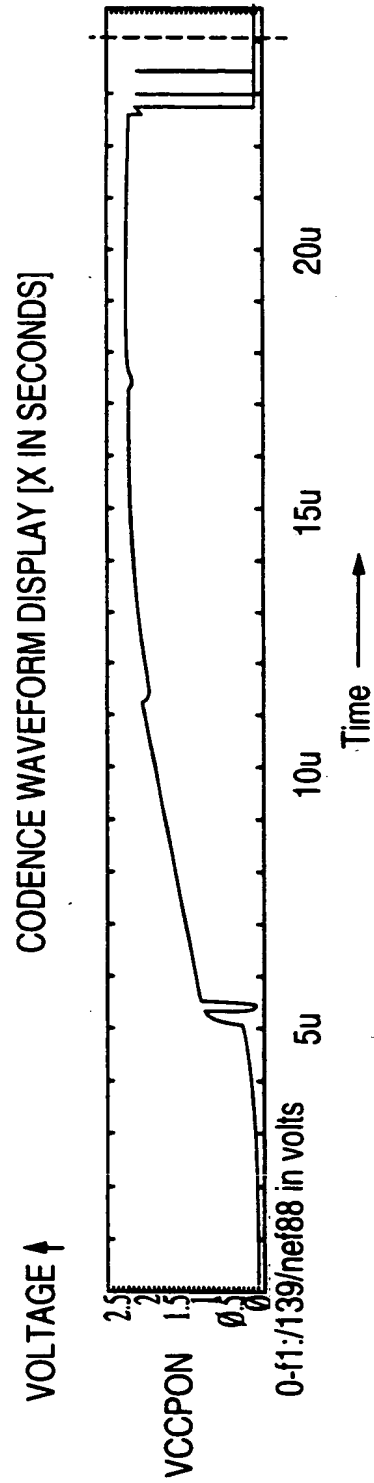
FIG. 102F

FORERO-564E660



NOTE THAT PWRRAS* WAITED FOR DVC20KR

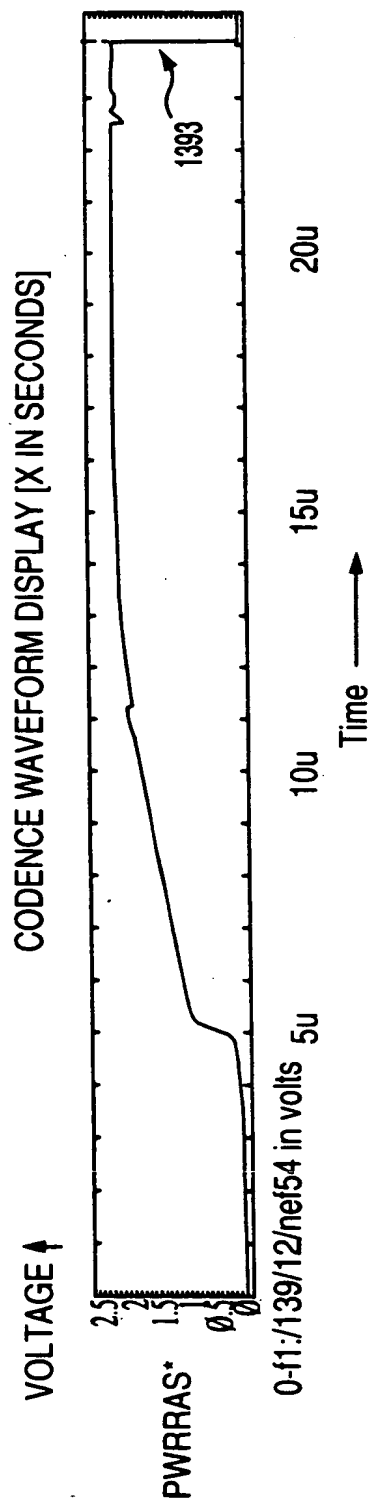
FIG. 102G



NOTE THAT PWRRAS* WAITED FOR DVC20KR

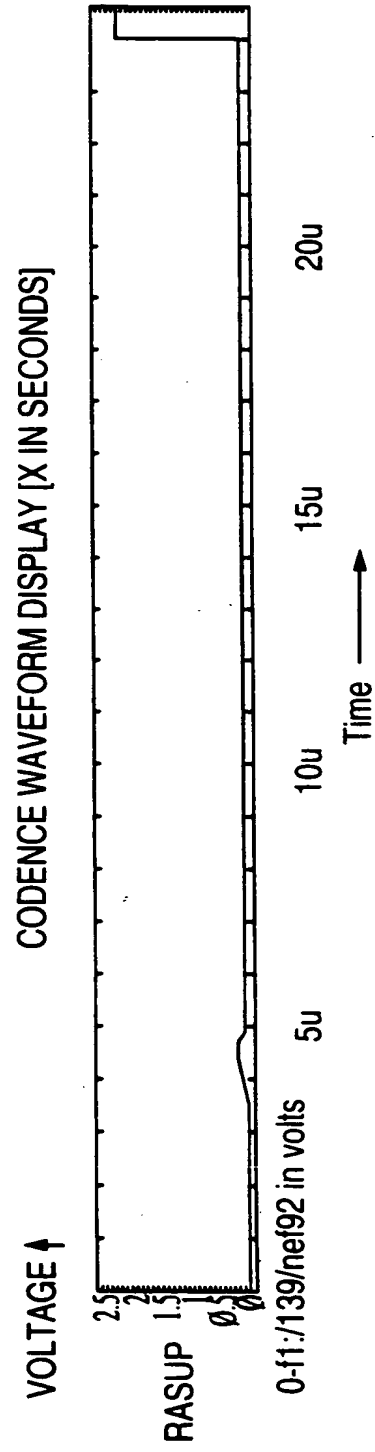
FIG. 102H

FOUO-564E660



NOTE THAT PWRRAS* WAITED FOR DVC20KR

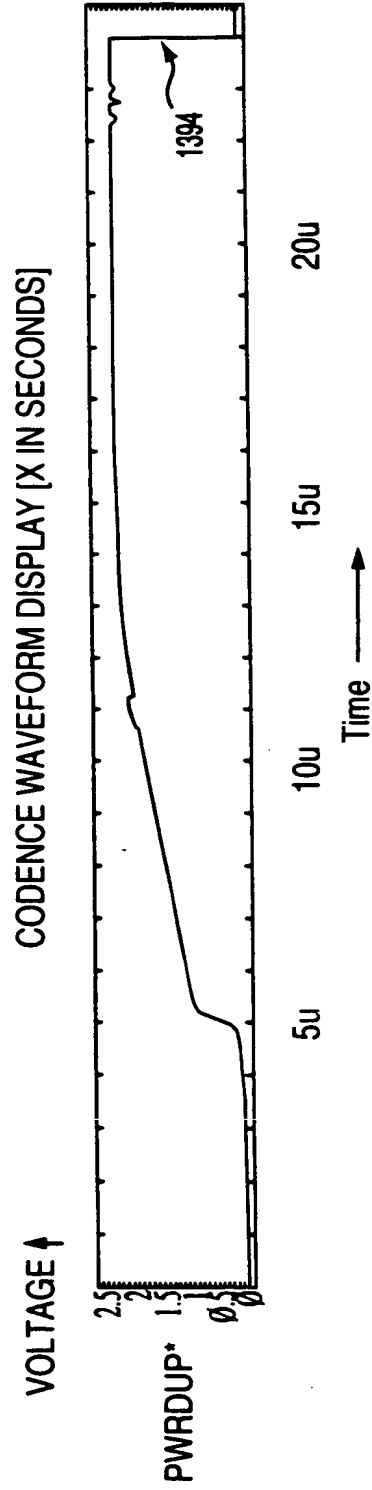
FIG. 102I



NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102J

FORM 56-4E660



NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102K

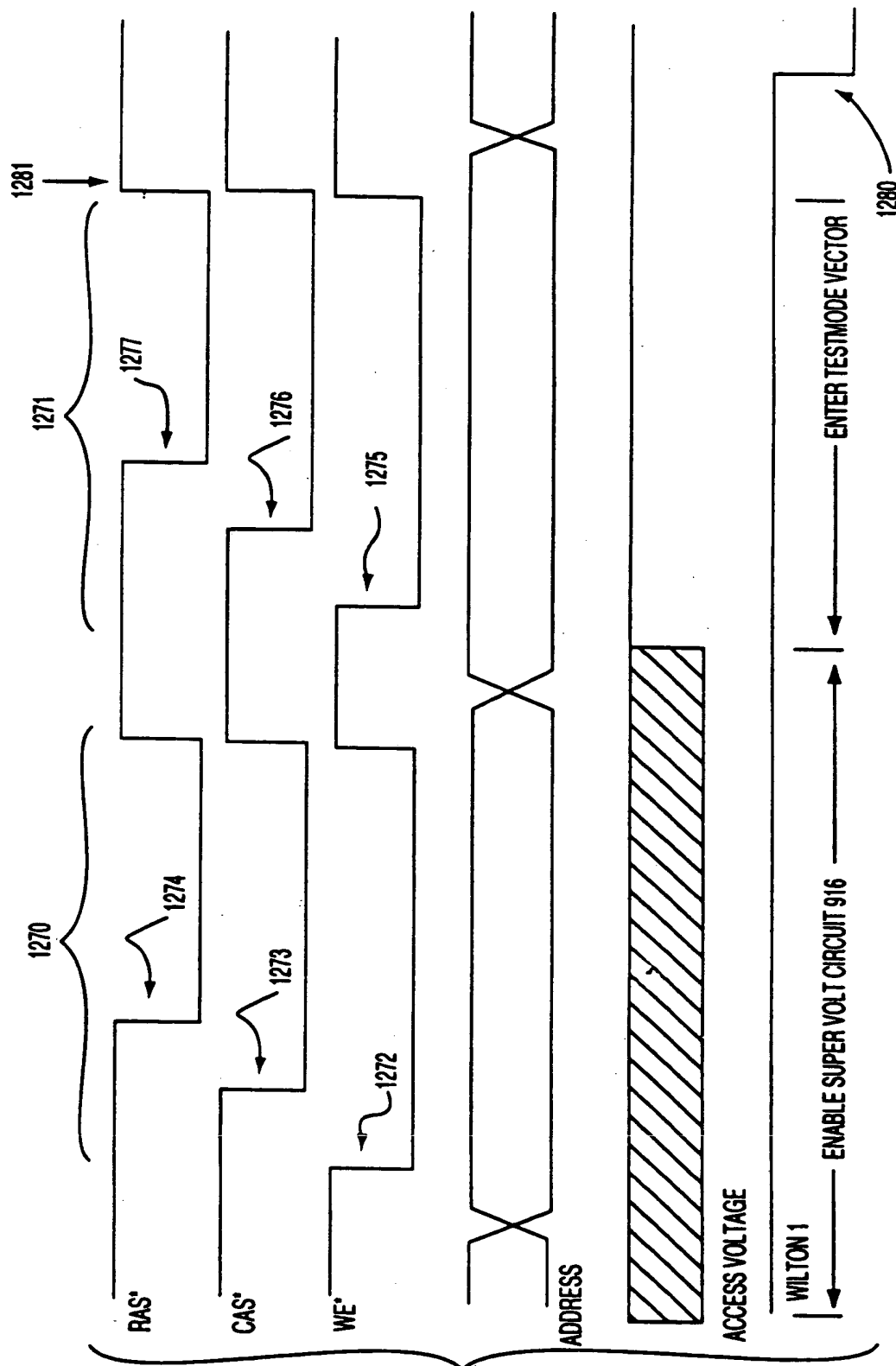
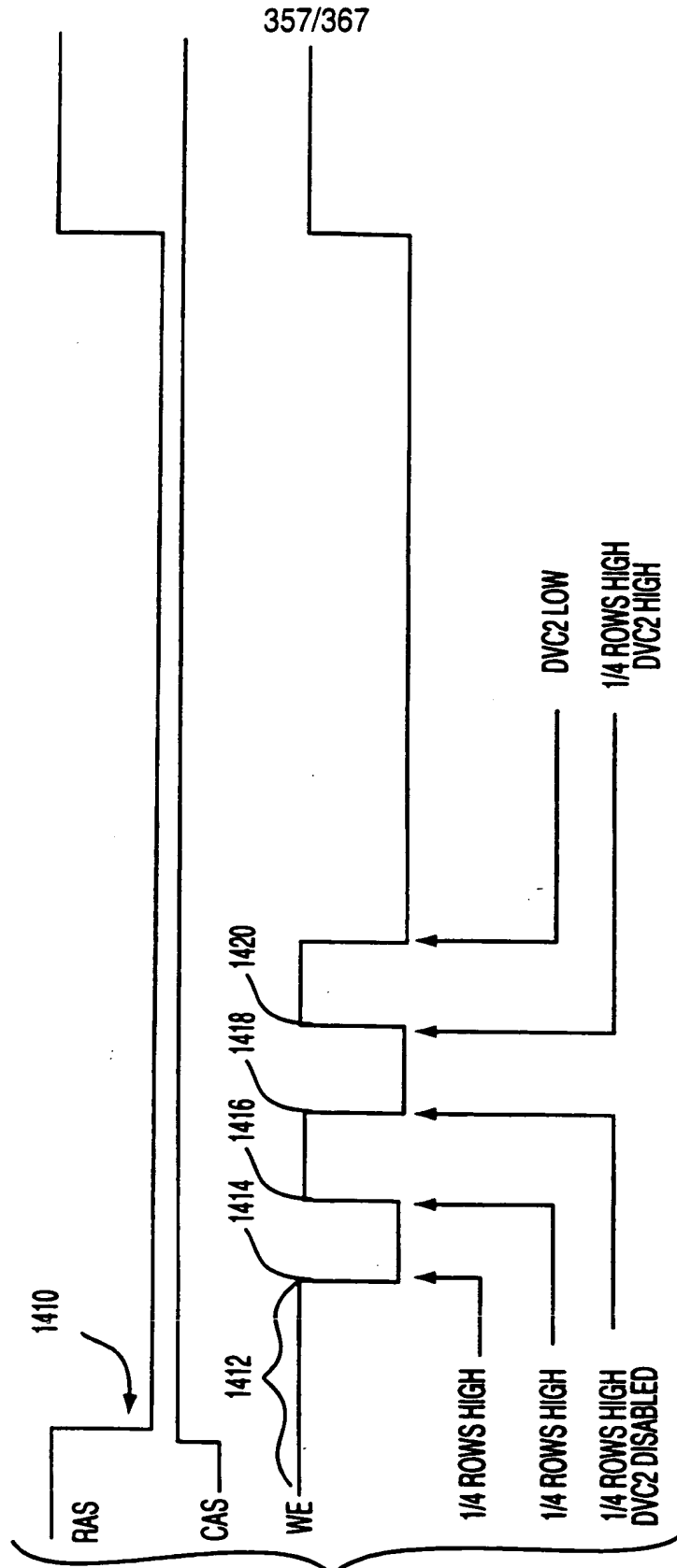


FIG.
103



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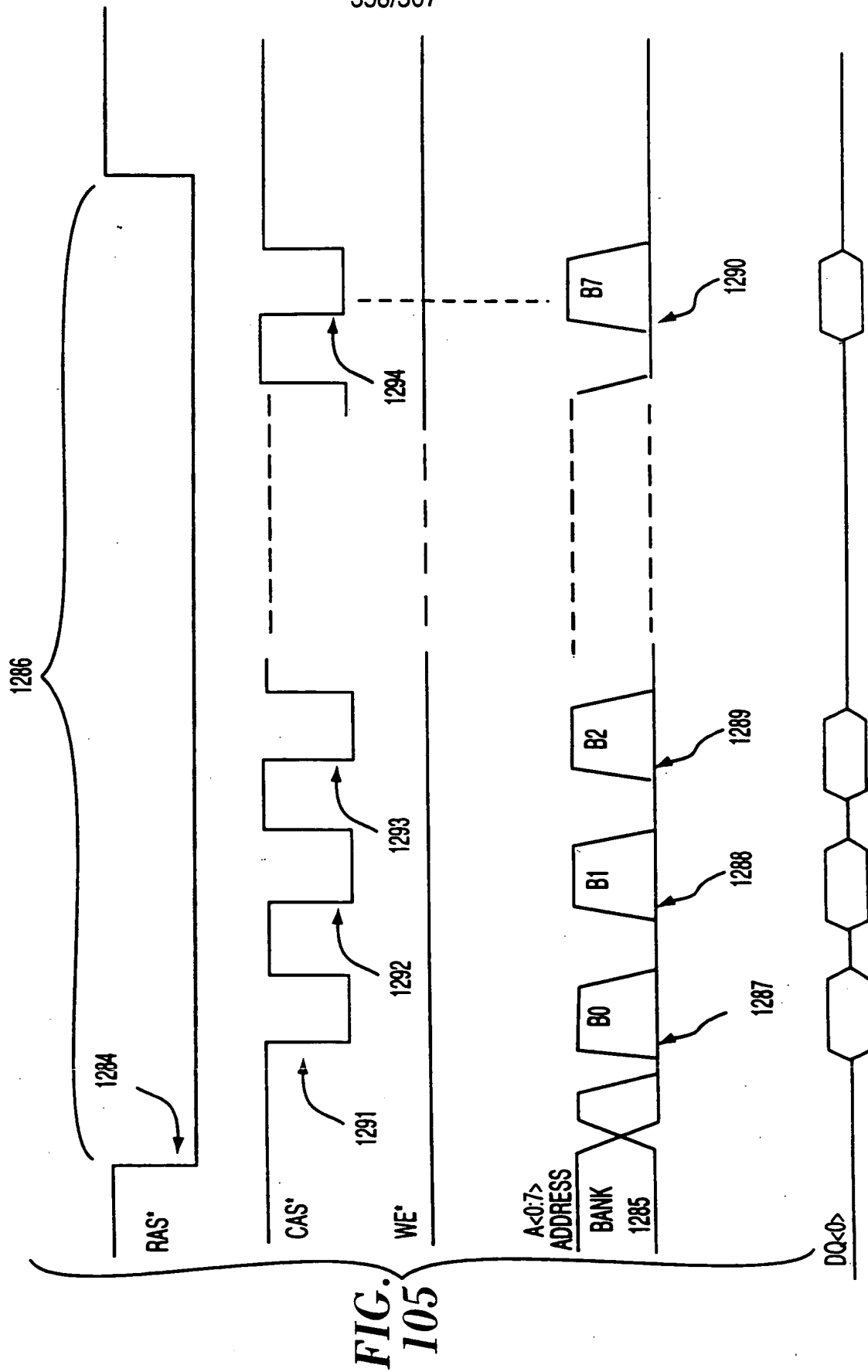


FIG. 106

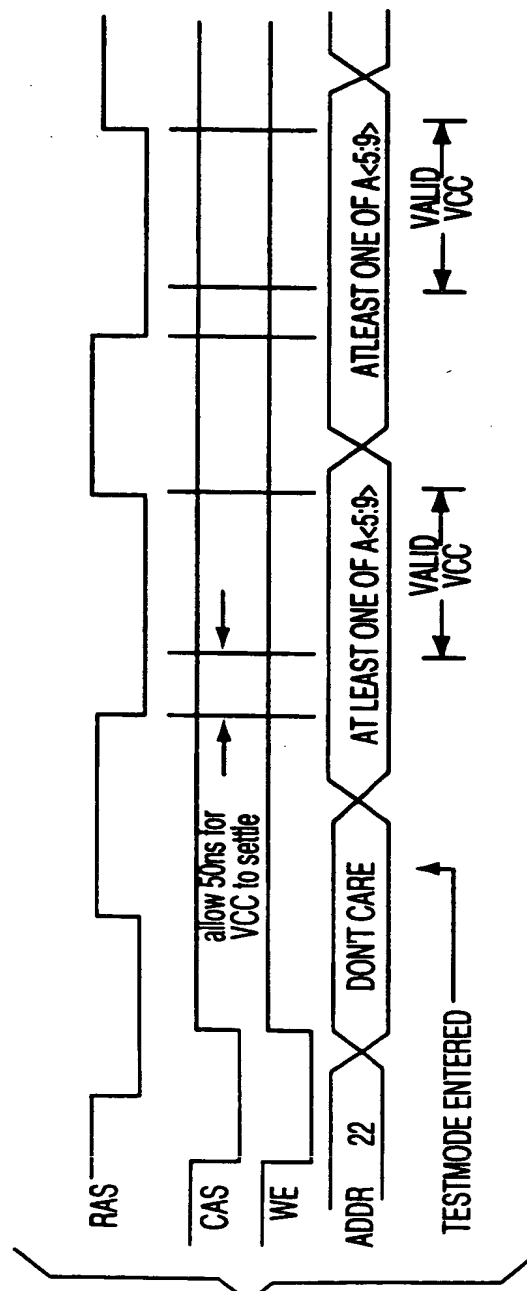
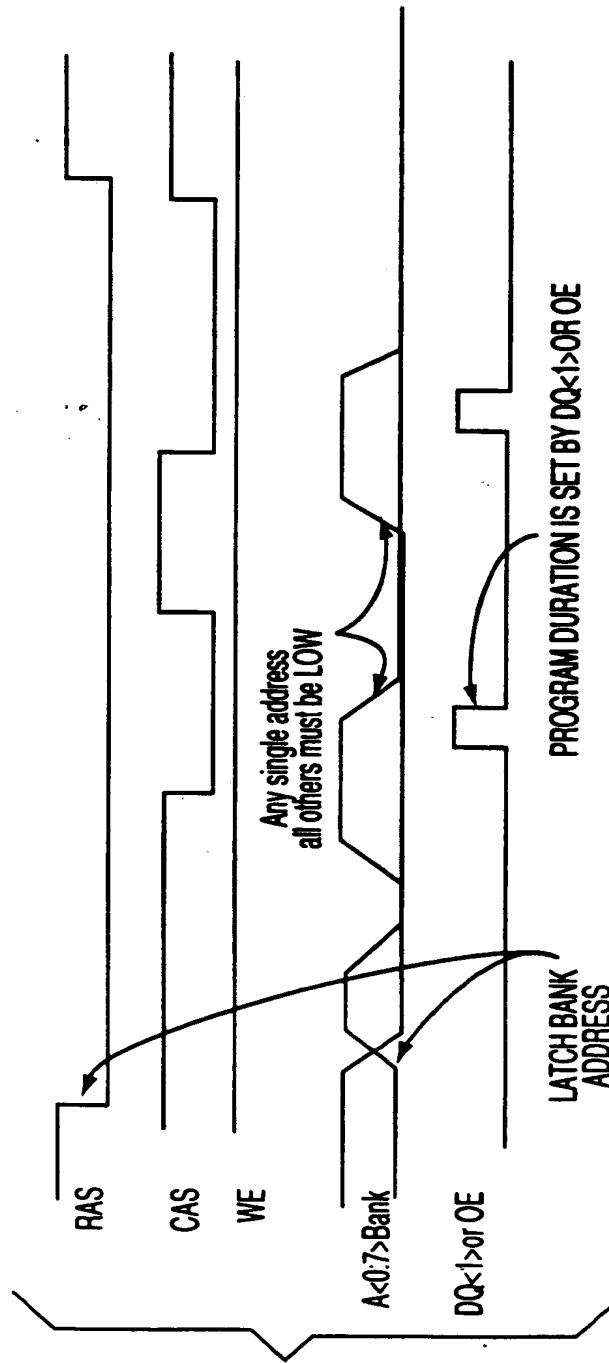


FIG. 106

FIG. 107



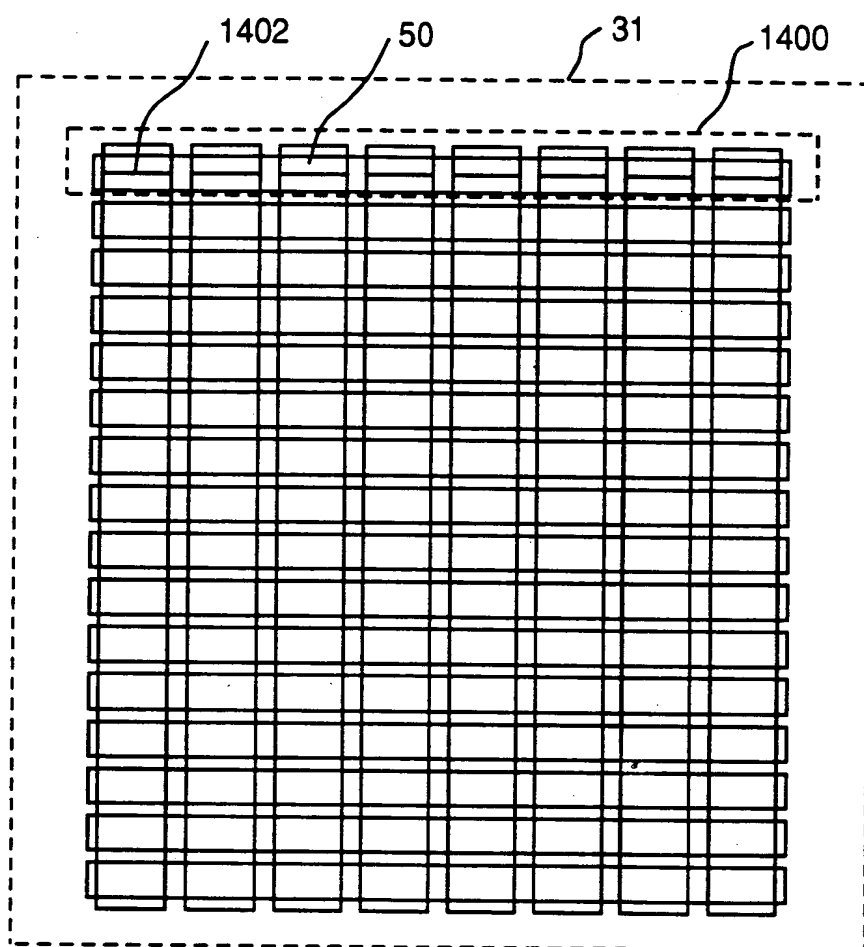
**FIG. 108**

FIG. 109-2

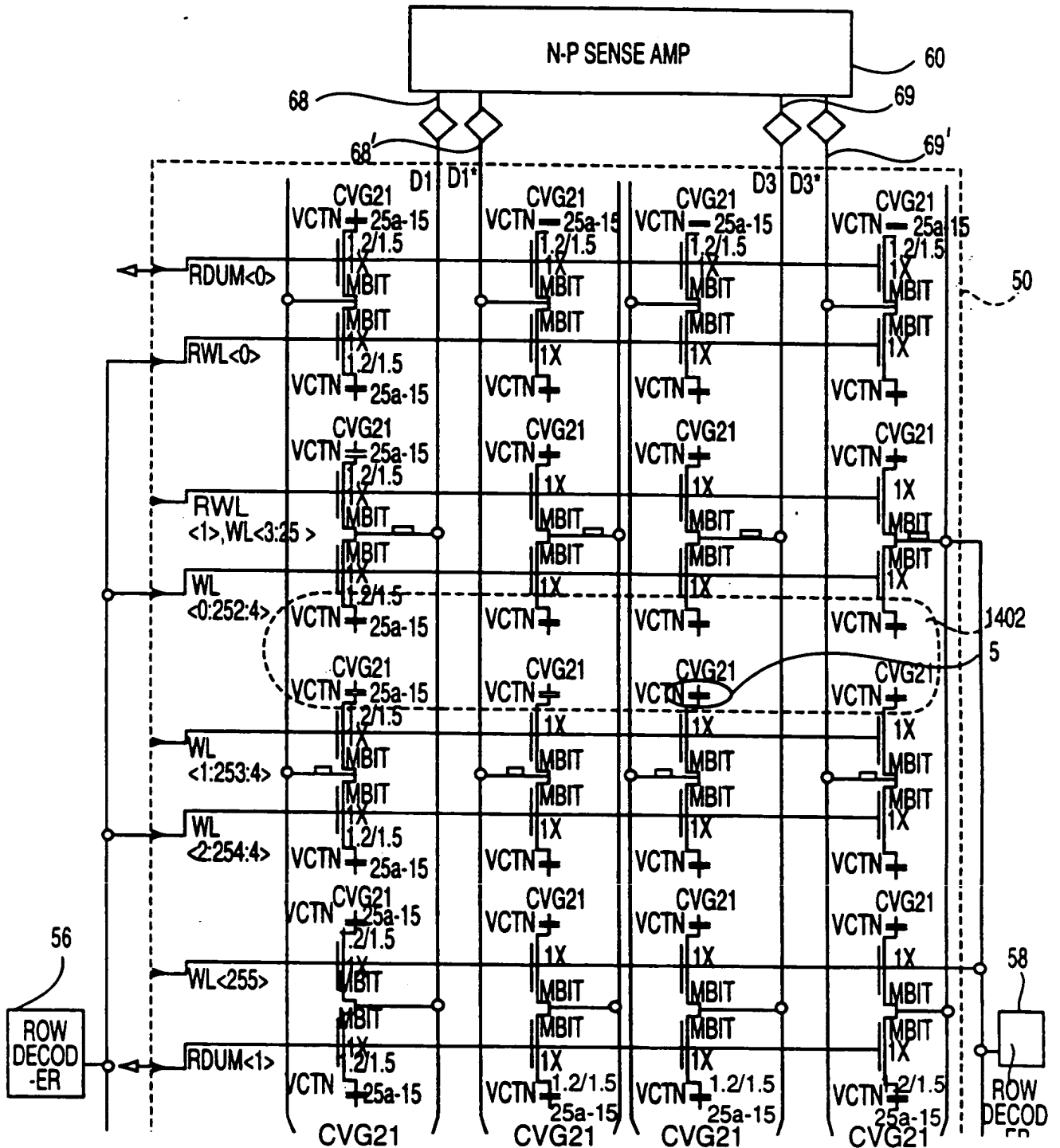


FIG. 109-2

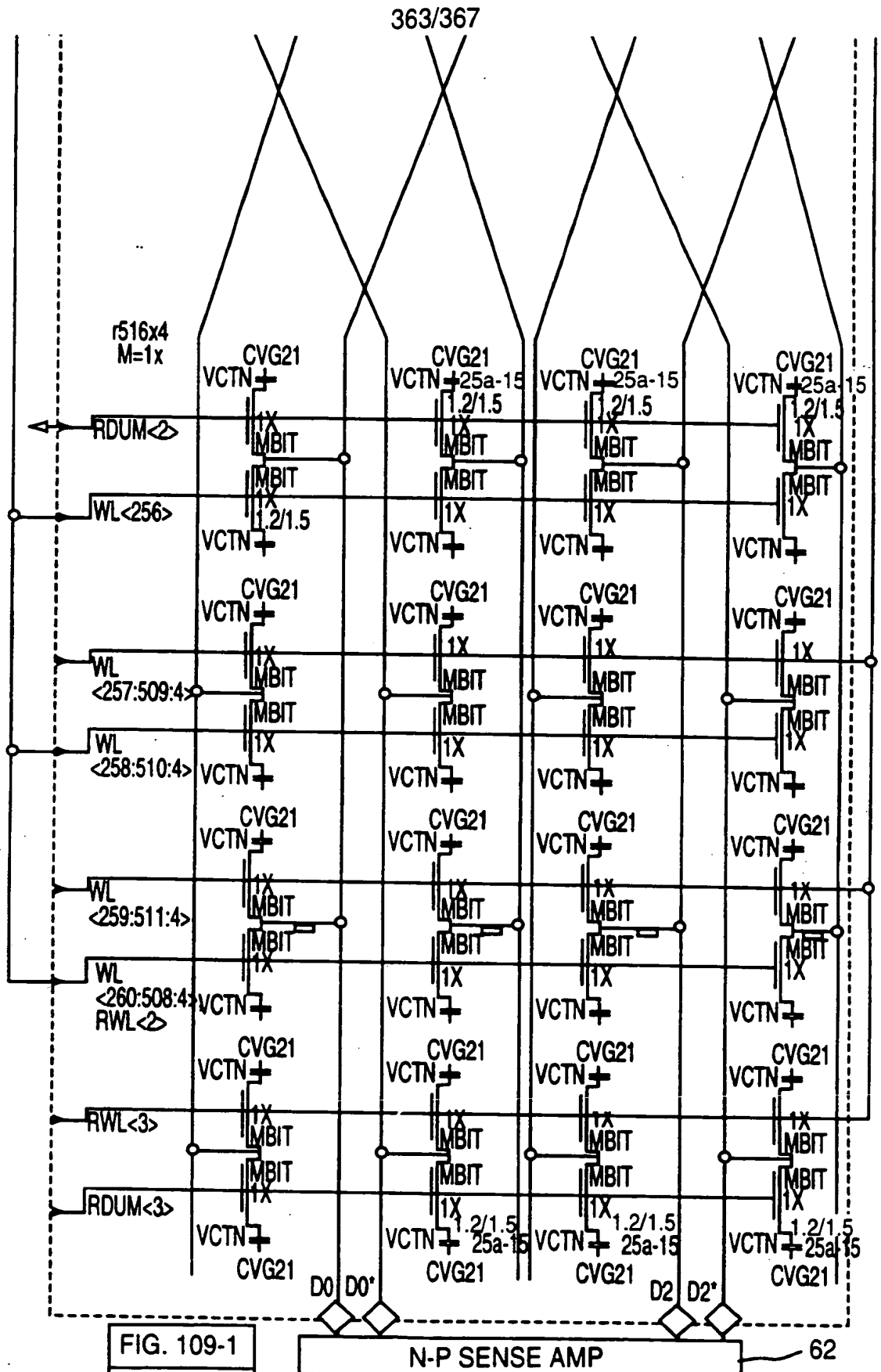


FIG. 109-1

FIG. 109-2

FIG. 109-2

[illegible]

Shrink Factor = 0.24
Mbit = 2.5 x 5.4 um (drawn)
0.600um Column Pitch
0.648 um Row Pitch

63.5um Scribe
24.0um Flat Strip
87.5um Edge

- 14.999 mm w/scribe
590.53 mls w/scribe

1776

520 total
Wordlines
Pitch=
0.648um

Twist
(6.144 μm)

PN Sense
2 Amps
(44.66um)

87.5um

-87.5um

120µm
24.677 mm w/scribe
971.55 mils w/scribe

240µm

Row Decode (93.12 μm)—

Edge Row Decode (84.72 um)-

63.5um Scribe
14.0um Clat Strip
87.5um Edges

1024 Actual Digits
Digitline Pitch=0.600um

FIG. 110

FIG. 111

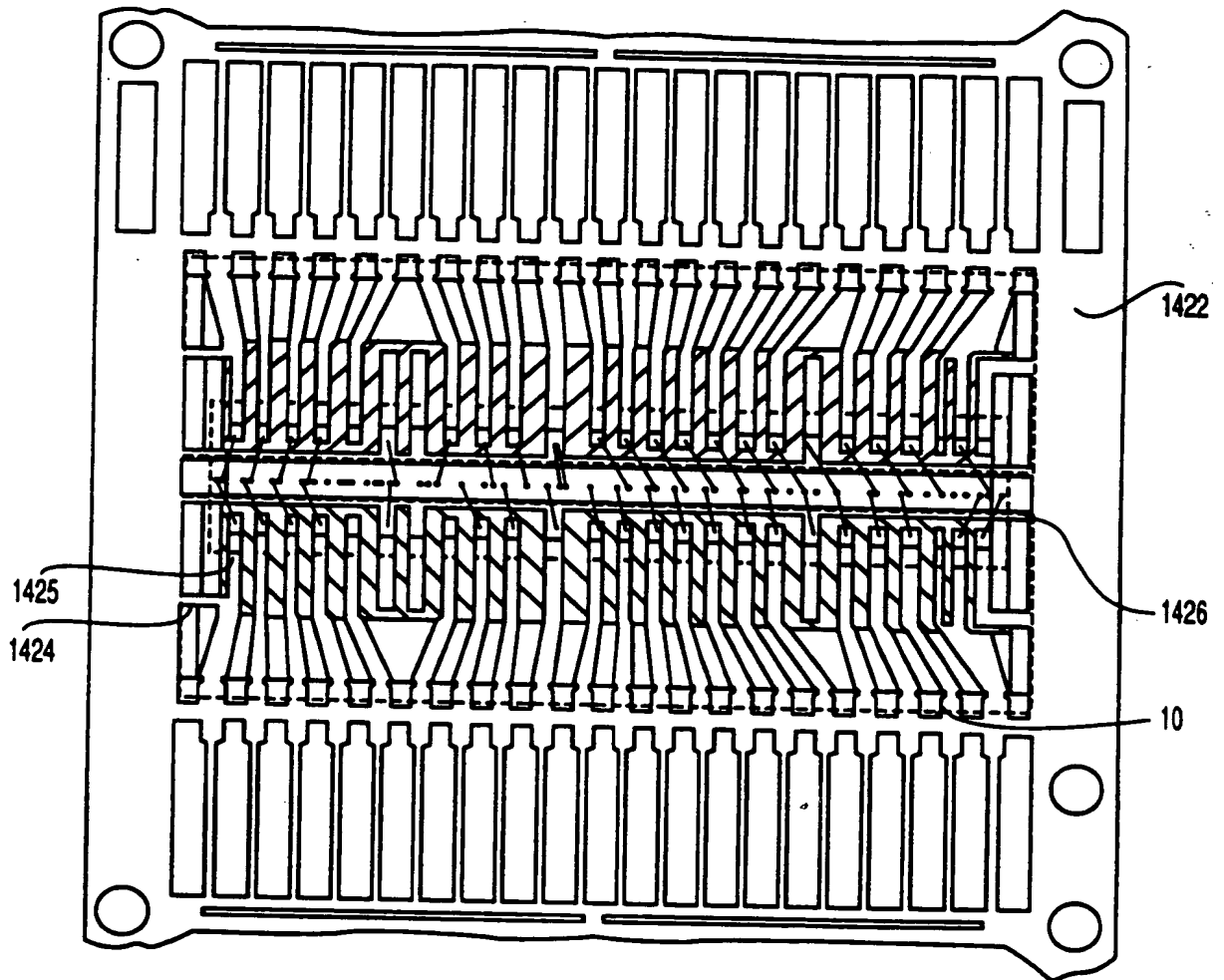
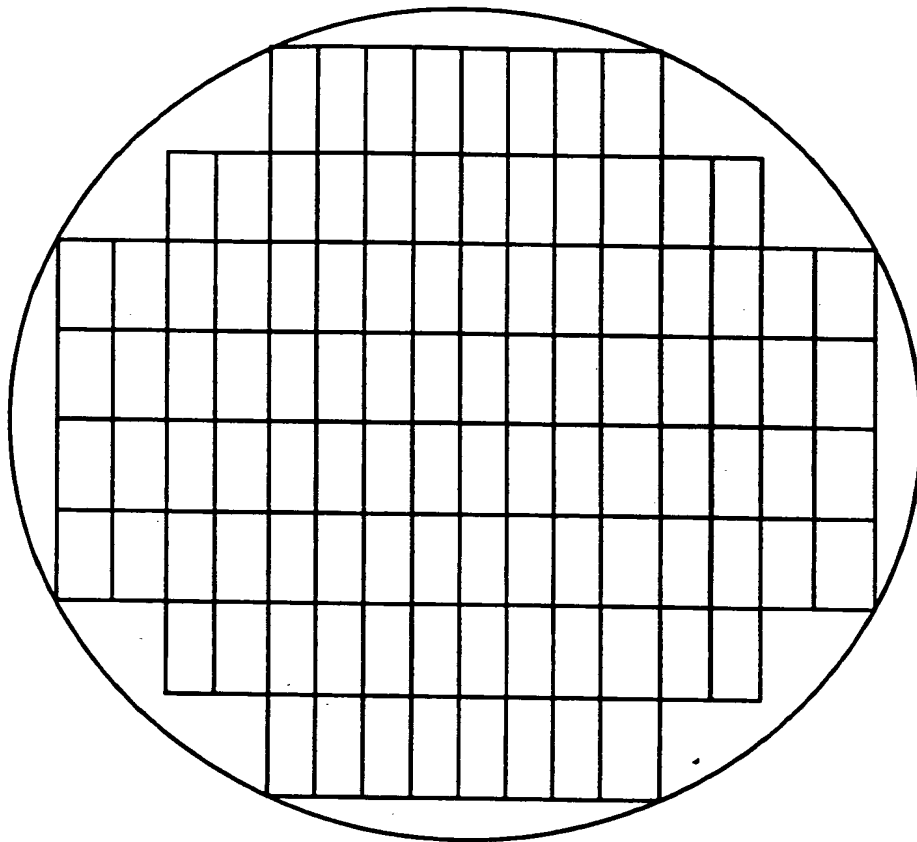


FIG. 111

**FIG. 112**

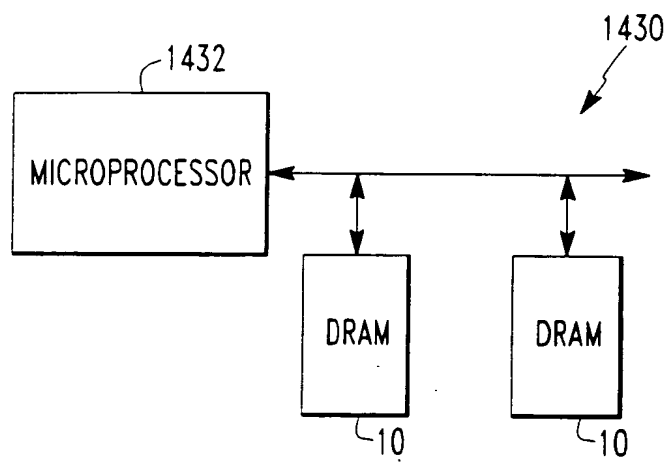


FIG. 113